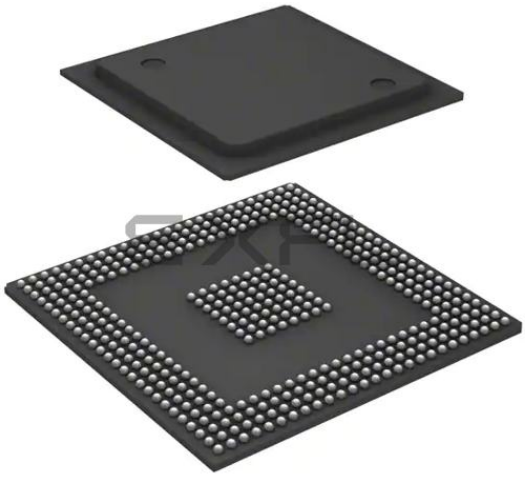
Infineon Technologies - TC1793F512F270EFABKXUMA2 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	270MHz
Connectivity	ASC, CANbus, EBI/EMI, FlexRay, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	221
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	192K x 8
RAM Size	288K x 8
Voltage - Supply (Vcc/Vdd)	1.17V ~ 3.63V
Data Converters	A/D 8x10b, 44x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	PG-BGA-416
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1793f512f270efabkxuma2

Figure 3 shows the block diagram of the **SAK-TC1793S-512F270EF**.

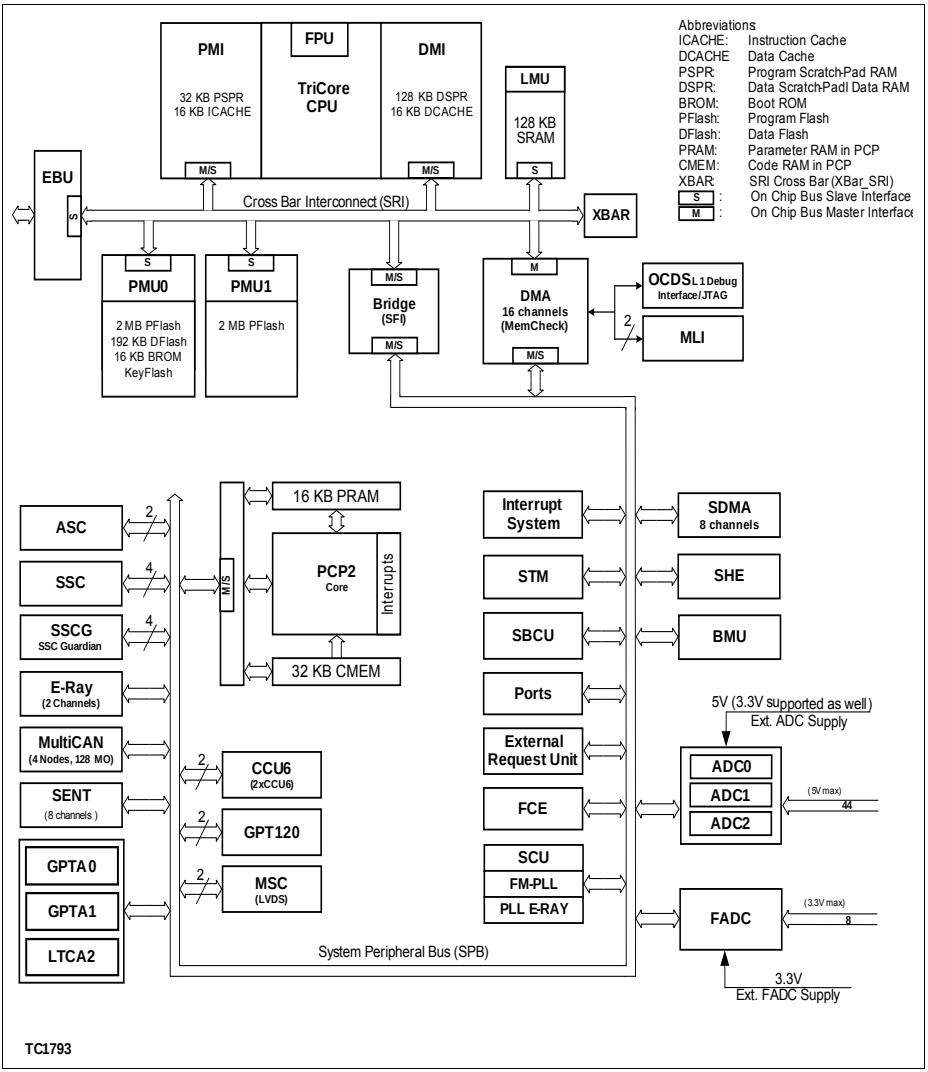


Figure 3 Block Diagram

3 Pinning

Figure 4 is showing the TC1793 Logic Symbol.

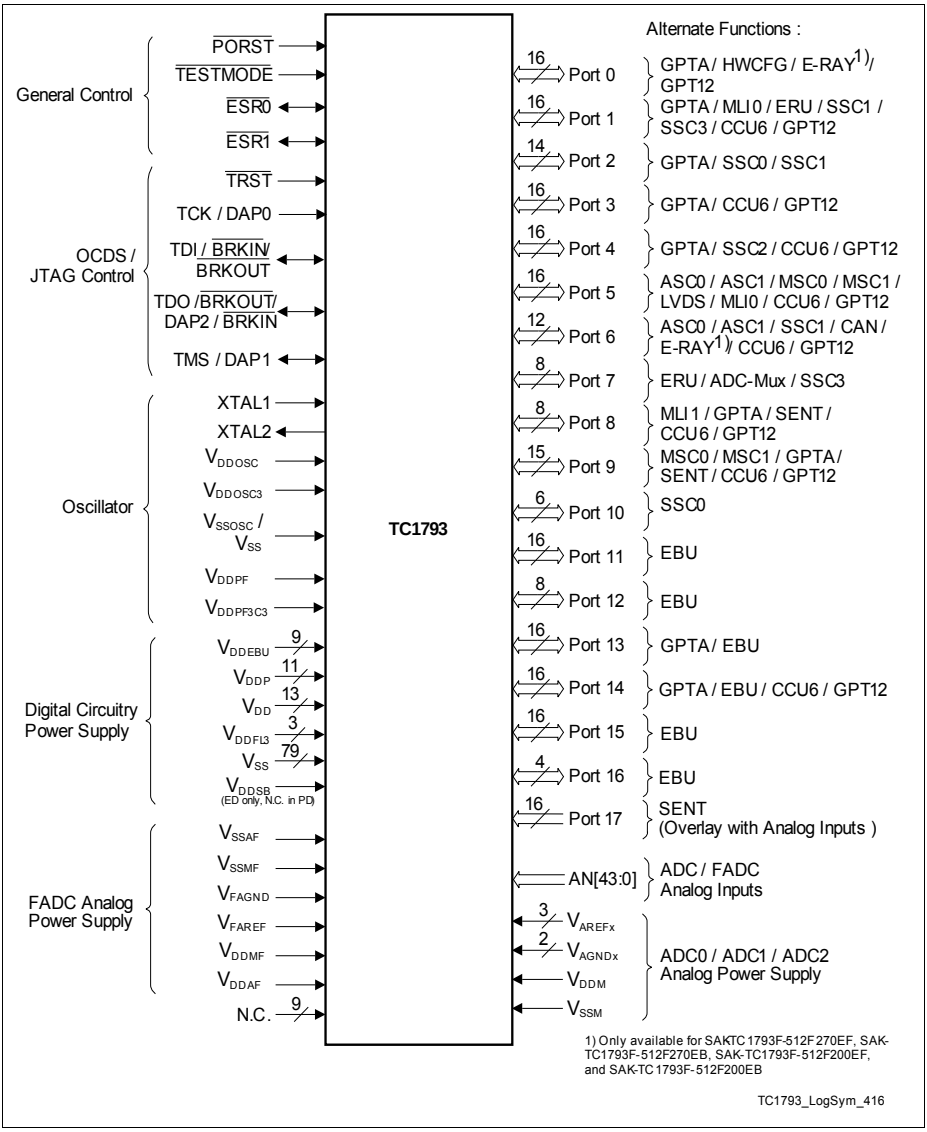


Figure 4 TC1793 Logic Symbol

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
D5	P0.13	I/O	A1/ PU	**Port 0 General Purpose I/O Line 13**
	RXDB0	I		**E-Ray Channel B Receive Data Input 0** [2]
	T5EUDB	I		**GPT120**
	T5EUDA	I		**GPT121**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
A5	P0.14	I/O	A2/ PU	**Port 0 General Purpose I/O Line 14**
	T6INA	I		**GPT120**
	T6INB	I		**GPT121**
	TXDA	O1		**E-Ray Channel A transmit Data Output** [2]
	Reserved	O2		-
	Reserved	O3		-
D4	P0.15	I/O	A1/ PU	**Port 0 General Purpose I/O Line 15**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
Port 1				
P3	P1.0	I/O	A2/ PU	**Port 1 General Purpose I/O Line 0**
	REQ0	I		**External trigger Input 0**
	EXTCLK1	O1		**External Clock Output 1**
	Reserved	O2		-
	Reserved	O3		-

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K1	P8.7	I/O	A1/ PU	**Port 8 General Purpose I/O Line 7**
	IN47	I		**IN47 Line of GPTA0**
	IN47	I		**IN47 Line of GPTA1**
	RDATA1A	I		**MLI1 Receive Channel Data Input A**
	SENT7	I		**SENT Digital Input**
	OUT47	O1		**OUT47 Line of GPTA0**
	COUT61	O2		**CCU61**
	T6OUT	O3		**GPT121**
Port 9				
A19	P9.0	I/O	A2/ PU	**Port 9 General Purpose I/O Line 0**
	IN48	I		**IN48 Line of GPTA0**
	IN48	I		**IN48 Line of GPTA1**
	COUT63	O1		**CCU62**
	OUT48	O2		**OUt48 Line of GPTA1**
	EN12	O3		**MSC1 Device Select Output 2**
B19	P9.1	I/O	A2/ PU	**Port 9 General Purpose I/O Line 1**
	IN49	I		**IN49 Line of GPTA0**
	IN49	I		**IN49 Line of GPTA1**
	CC60INB	I		**CCU62**
	CC60INA	I		**CCU63**
	CC60	O1		**CCU63**
	OUT49	O2		**OUT49 Line of GPTA1**
	EN11	O3		**MSC1 Device Select Output 1**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A21	P9.9	I/O	A1/ PU	**Port 9 General Purpose I/O Line 9**
	SENT0	I		**SENT Digital Input**
	Reserved	O1		**-**
	SENT0	O2		**SENT Digital Output**
	Reserved	O3		**-**
B21	P9.10	I/O	A1/ PU	**Port 9 General Purpose I/O Line 10**
	EMGSTOP	I		**Emergency Stop**
	SENT7	I		**SENT Digital Input**
	COUT63	O1		**CCU63**
	SENT7	O2		**SENT Digital Output**
	Reserved	O3		**-**
C21	P9.11	I/O	A1/ PU	**Port 9 General Purpose I/O Line 11**
	SENT2	I		**SENT Digital Input**
	Reserved	O1		**-**
	SENT2	O2		**SENT Digital Output**
	Reserved	O3		**-**
D21	P9.12	I/O	A1/ PU	**Port 9 General Purpose I/O Line 12**
	SENT5	I		**SENT Digital Input**
	Reserved	O1		**-**
	SENT5	O2		**SENT Digital Output**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AF8	V_{FAREF}	-	-	**FADC Reference Voltage**
AE8	V_{FAGND}	-	-	**FADC Reference Ground**
AE9	V_{DDMF}	-	-	**FADC Analog Part Power Supply (3.3V)**
AC9	V_{DDAF}	-	-	**FADC Analog Part Logic Power Supply (1.3V)**
AF9	V_{SSMF}	-	-	**FADC Analog Part Ground**
	V_{SSAF}	-	-	**FADC Analog Part Logic Ground**
A18, B18, H3	V_{DDFL3}	-	-	**Flash Power Supply (3.3V)**
F25	V_{SSOSC}	-	-	**Main Oscillator Ground**
	V_{SS}	-	-	**Digital Ground**
F26	V_{DDOSC}	-	-	**Main Oscillator Power Supply (1.3V)**
E26	V_{DDOSC3}	-	-	**Main Oscillator Power Supply (3.3V)**
G23	V_{DDPF}	-	-	**E-Ray PLL Power Supply (1.3V)**
G24	V_{DDPF3}	-	-	**E-Ray PLL Power Supply (3.3V)**
AC11, AC20, AB23, V23, P23, E23, D24, C25, B26, D16, D9, H4, R4	V_{DD}	-	-	**Digital Core Power Supply (1.3V)**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AC16, AD16, AE16, AF16, D22, C23, B24, A25, D14, D7, K4	V_{DDP}	-	-	**Port Power Supply (3.3V)**
H23, H24, H25, H26, M23, T23, Y23, AC18, AC22	V_{DDEBU}	-	-	**EBU Port Power Supply (1.8V - 2.5V - 3.3V)**
R1	V_{DDSB}	-	-	**Emulation Stand-by SRAM Power Supply (1.3V) (Emulation device only)** *Note: This pin is N.C. in a productive device.*
AC10, AC17, AC19, AC23, W23, R23, L23, D23, C24, B25, A26, D15, D8, J4, T4	V_{SS}	-	-	**Digital Ground (outer balls)**

5 Electrical Parameters

This specification provides all electrical parameters of the TC1793.

5.1 General Parameters

5.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1793 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1793 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1793 designed in.

1) The port groups are defined in **Table 14**.

Table 14 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
45	P2.[15:11]
46	P2.[10:5]

Table 18 Standard_Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A2 pads [1]	$HYSA2$ CC	0.1 x V_{DDP}	–	–	V	
Input Leakage current Class A2	I_{OZA2} CC	-6000	–	6000	nA	$V_i < V_{DDP}$ / 2 - 1 V; $V_i > V_{DDP}$ / 2 + 1 V; $V_i \geq 0$ V; $V_i \leq V_{DDP}$ V
		-3000	–	3000	nA	$V_i > V_{DDP}$ / 2 - 1 V; $V_i < V_{DDP}$ / 2 + 1 V
Ratio Vil/Vih, A2 pads	V_{ILA2} / V_{IHA2} CC	0.6	–	–		
On-Resistance of the class A2 pad, weak driver	R_{DSONW} CC	–	450	600	Ohm	$I_{OH} > -0.5$ mA; P_MOS
		–	210	340	Ohm	$I_{OL} < 0.5$ mA; N_MOS
On-Resistance of the class A2 pad, medium driver	R_{DSONM} CC	–	–	155	Ohm	$I_{OH} > -2$ mA; P_MOS
		–	–	110	Ohm	$I_{OL} < 2$ mA; N_MOS
On-Resistance of the class A2 pad, strong driver	R_{DSON2} CC	–	–	28	Ohm	$I_{OH} > -2$ mA; P_MOS
		–	–	22	Ohm	$I_{OL} < 2$ mA; N_MOS

Table 18 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak

Table 18 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak
Input high voltage, class A2 pads	V_{IHA2} SR	0.6 x V_{DDP}	–	$min(V_{DDP}+0.3, 3.6)$	V	
Input low voltage Class A2 pads	V_{ILA2} SR	-0.3	–	0.36 x V_{DDP}	V	
Output voltage high class A2 pads	V_{OHA2} CC	V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= medium
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= strong
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= medium
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= strong
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -400 µA; pin out driver= weak
		2.4	–	–	V	I_{OH}≥ -500 µA; pin out driver= weak

2) V_{ILSD} is implemented to ensure J2716 specification. It can't be guaranteed that it suppresses switching due to external noise.

Table 23 LVDS_Pads Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output impedance, pad class F, LVDS mode	R_O CC	40	–	140	Ohm	
Fall time, pad type LVDS	t_{FL} CC	–	–	2	ns	termination 100 Ω ± 1 %
Rise time, pad type LVDS	t_{RL} CC	–	–	2	ns	termination 100 Ω ± 1 %
Pad set-up time	t_{SET_LVDS} CC	–	–	13	µs	termination 100 Ω ± 1 %
Output Differential Voltage	V_{OD} CC	150	–	400	mV	termination 100 Ω ± 1 %
Output voltage high, pad class F, LVDS mode	V_{OH} CC	–	–	1525	mV	termination 100 Ω ± 1 %
Output voltage low, pad class F, LVDS mode	V_{OL} CC	875	–	–	mV	termination 100 Ω ± 1 %
Output Offset Voltage	V_{OS} CC	1075	–	1325	mV	termination 100 Ω ± 1 %

5.2.2 Analog to Digital Converters (ADCx)

ADC parameter are valid for $V_{DD\,/\,DDAF}$ = 1.235 V to 1.365 V; V_{DDM} = 4.5 V to 5.5 V.

Table 24 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at the analog voltage inputs[1]	C_{AINSW} CC	–	9	20	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	20	30	pF	
Switched capacitance at the positive reference voltage input[2][3]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[2]	$C_{AREFTOT}$ CC	–	20	40	pF	
Differential Non-Linearity Error[4][5][6][7]	EA_{DNL} CC	-3	–	3	LSB	ADC resolution= 12-bit [8] [9]
Gain Error[4][5][6][7]	EA_{GAIN} CC	-3.5	–	3.5	LSB	ADC resolution= 12-bit [8] [9]
Integral Non-Linearity[4][5][7][7]	EA_{INL} CC	-3	–	3	LSB	ADC resolution= 12-bit [8] [9]
Offset Error[4][5][6][7]	EA_{OFF} CC	-4	–	4	LSB	ADC resolution= 12-bit [8] [9]
Converter clock	f_{ADC} SR	4	–	100	MHz	f_{ADC}= f_{FPI}
Internal ADC clock	f_{ADCI} CC	1	–	18	MHz	ADC0
		1	–	18	MHz	ADC1
		1	–	20[10]	MHz	ADC2
Charge consumption per conversion	Q_{CONV} CC	70	85[11]	100	pC	charge needs to be provided via V_{AREF0}

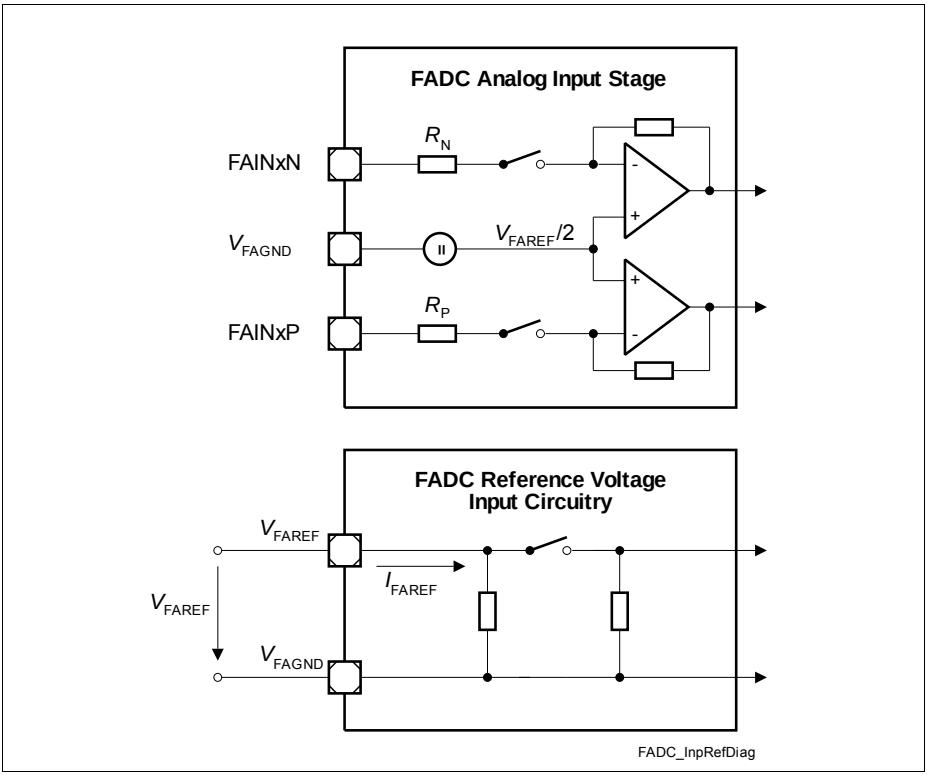


Figure 8 FADC Input Circuits

Table 29 Power Supply Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum power dissipation	PD CC	–	–	1633	mW	power pattern= max; fCPU=270 MHz
		–	–	1488	mW	power pattern= realistic; fCPU=270 MHz
		–	–	1523	mW	power pattern= max; fCPU=200 MHz
		–	–	1403	mW	power pattern= realistic; fCPU=200 MHz

1) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each customer application will most probably be lower than this value, but must be evaluated seperately.
2) This current includes the E-Ray module power consumption, including the PCP operation component.
3) The I_{DD} decreases typically by 97 mA if the f_{CPU} decreases by 50MHz, at constant T_J
4) The I_{DD} decreases typically by 105 mA if the f_{CPU} decreases by 50MHz, at constant T_J
5) D-Flash read, write, or erase opoeration in parallel to P-Flash operations name in Test Condition is covered already in the give current limits.
6) Relevant for the power supply dimensioning, not for thermal considerations.
7) In case of erase of Program Flash PFx, internal flash array loading effects may generate transient current spikes of up to 15 mA for maximum 5 ms per flash module.
8) For power supply dimensioning of V_{DDP} 30 mA have to added for flash programming case.

Note: In general current consumption for operations with data flash are always lower than the defined values for program flash read operation.

5.2.6.1 Calculating the 1.3 V Current Consumption

The current consumption of the 1.3 V rail compose out of two parts:

- Static current consumption
- Dynamic current consumption

The static current consumption is related to the device temperature T_J and the dynamic current consumption depends of the configured clocking frequencies and the software

5.3.2 Power Sequencing

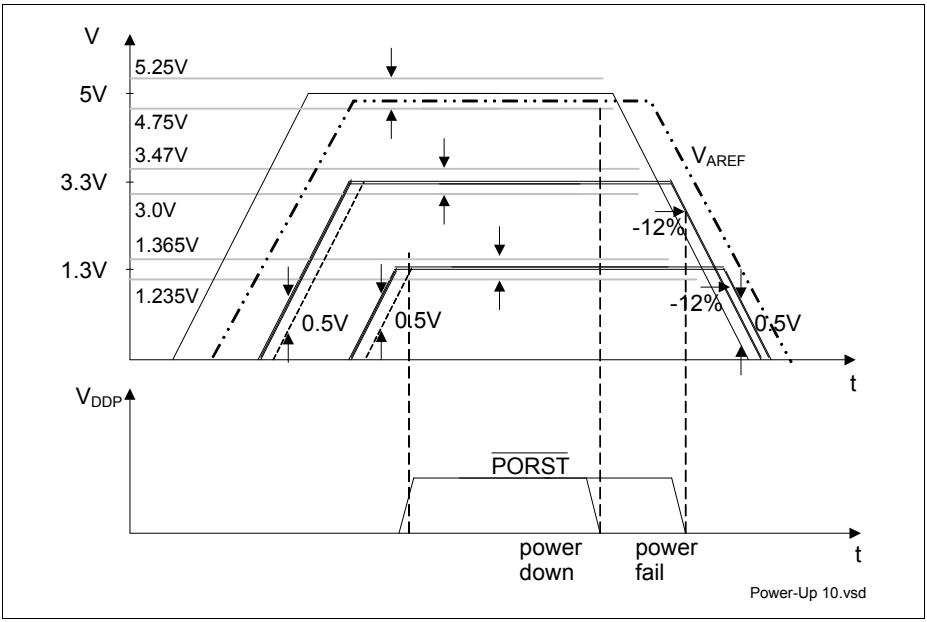


Figure 12 5 V / 3.3 V / 1.3 V Power-Up/Down Sequence

The following list of rules applies to the power-up/down sequence:

- All ground pins V_{SS} must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- At any moment in time to avoid increased latch-up risk,
  each power supply must be higher then any lower_power_supply - 0.5 V, or:
  VDD5 > VDD3.3 - 0.5 V; VDD5 > VDD1.3 - 0.5 V;VDD3.3 > VDD1.3 - 0.5 V, see **Figure 12**.
  – The latch-up risk is minimized if the I/O currents are limited to:
  – 20 mA for one pin group
  – AND 100 mA for the completed device I/Os
  – AND additionally before power-up / after power-down:
  1 mA for one pin in inactive mode (0 V on all power supplies)
- During power-up and power-down, the voltage difference between the power supply pins of the same voltage (3.3 V, 1.3 V, and 5 V) with different names (for example VDDP, VDDFL3 ...), that are internally connected via diodes, must be lower than

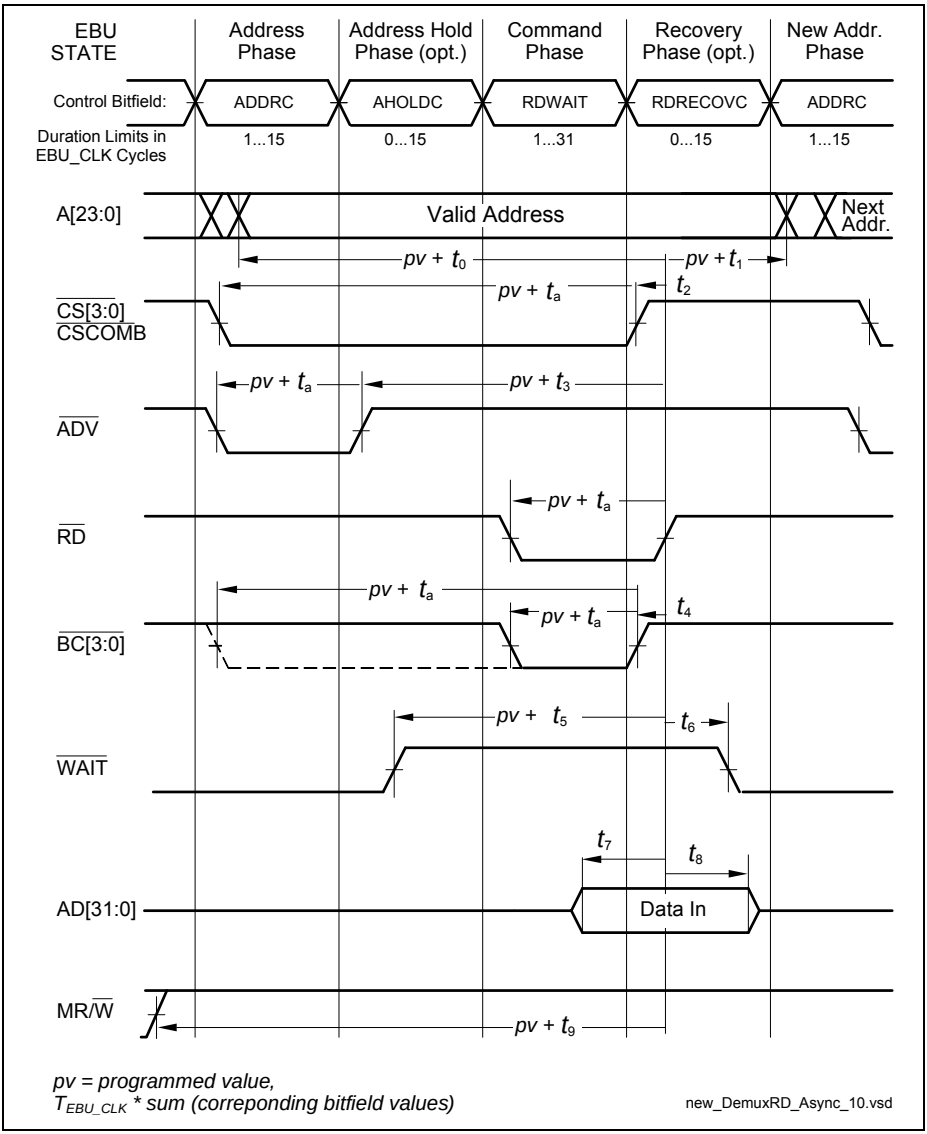


Figure 26 Demultiplexed Read Access

- add note at the end of Pin Reliability in Overload section
- clearify pad supply levels in Pin Reliability in Overload section
- add footnote for D-Flash currents in power section
- clearify wording for valid operating conditions
- add negative limit for class S pad leakage
- increase max values for parameter t_B
- change formula 10
- change MLI parameter t_{17} min value
- change footnote 3 for EBU parameter t_{22}
- change package naming
- add products SAK-TC1793N-512F270EF and SAK-TC1793N-512F270EB
- split FADC DNL parameter into two conditions and change value for gain 4 and 8
- update footnote 10 for the ADC
- update package outline
- update parmeter description for SSC parameters t_{52} and t_{53}
- change SSC parameters from CC to SR Symbol for t_{56}, t_{57}, t_{58} and t_{59}
- increase value range for BFCLKO duty cycle

The following changes where done between Version 1.0 and 1.1 of this document:

- add product option SAK-TC1793S-512F270EF
- update block diagrams to cover new option
- add identification registers for new product option
- rework first sentence for chapter 5.3
- reduce min value for t_L for both PLLs
- split f_{VCO} for system PLL into two conditions
- add for MLI and SSC parameter: valid strong driver medium edge only
- add footnote 5) for SSC parameters
- add parameters t_{15}, t_{16}, t_{17}, and t_{19} to the EBU

The following changes where done between Version 1.1 and 1.1.1 of this document:

- update the incoorect CHIPID values for copper and non copper bond options.
- product SAK-TC-1793N-512F270EB not longer supported and replaced by SAK-TC1793N-512F270EF

The following changes where done between Version 1.1.1 and 1.2 of this document:

- remove the following product options:
  – SAK-TC1793F-512F270EB
- change V_{ILS} from 2.1V to 1.9V in table 23
- change t_{48} from 100ns to 200ns in table 42
- change t_{49} from 100ns to 200ns in table 42
- extend K_{OVAN} conditon from $I_{OV}\leq$ 0 mA; $I_{OV}\geq$ -1 mA to $I_{OV}\leq$ 0 mA; $I_{OV}\geq$ -2 mA
- change t_8 from -4ns to -2ns in table 43
- change t_{18} from -4ns to -2ns in table 43