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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRAY, I²C, LINbus, SPI, PSI, UART/USART
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8.64MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	404K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12b SAR, 16b Sigma-Delta
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	512-FBGA
Supplier Device Package	512-FBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777mk0mva8

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    - Access path via dedicated AXBS slave port
        - Avoids contention with other memory accesses
- Two Dual-channel FlexRay controllers
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- Self-test capability

Table 1. MPC5777M feature (continued)

Feature	MPC5777M
CRC channels	2
Software watchdog timer (Task SWT/Safety SWT)	4 (3/1)
Core Nexus class	3+
Sequence processing unit (SPU)	Yes
Debug and calibration interface (DCI) / run control module	Yes
System SRAM	404 KB
Flash memory	8640 KB
Flash memory fetch accelerator	4 × 256 bit
Data flash memory (EEPROM)	8 × 64 KB + 2 × 16 KB
Flash memory overlay RAM	16 KB
External bus	32 bit
Calibration interface	64-bit IPS Slave
DMA channels	2 × 64
DMA Nexus Class	3+
LINFlex (UART/MSC)	6 (3/3)
MCAN/TTCAN	4/1
DSPI (SPI/MSC/sync SCI)	8 (4/3/1)
Microsecond bus downlink	Yes
SENT bus	15
I^2C	2
PSI5 bus	5
PSI5-S UART-to-PSI5 interface	Yes
FlexRay	2 × dual channel
Ethernet	MII / RMII
Zipwire® (SIPI / LFAST^2) Interprocessor Communication Interface	High speed
System timers	8 PIT channels 3 AUTOSAR® (STM) 64-bit PIT
BOSCH® GTM Timer[3]	Yes
GTM RAM	58 KB
Interrupt controller	727 sources
ADC (SAR)	12

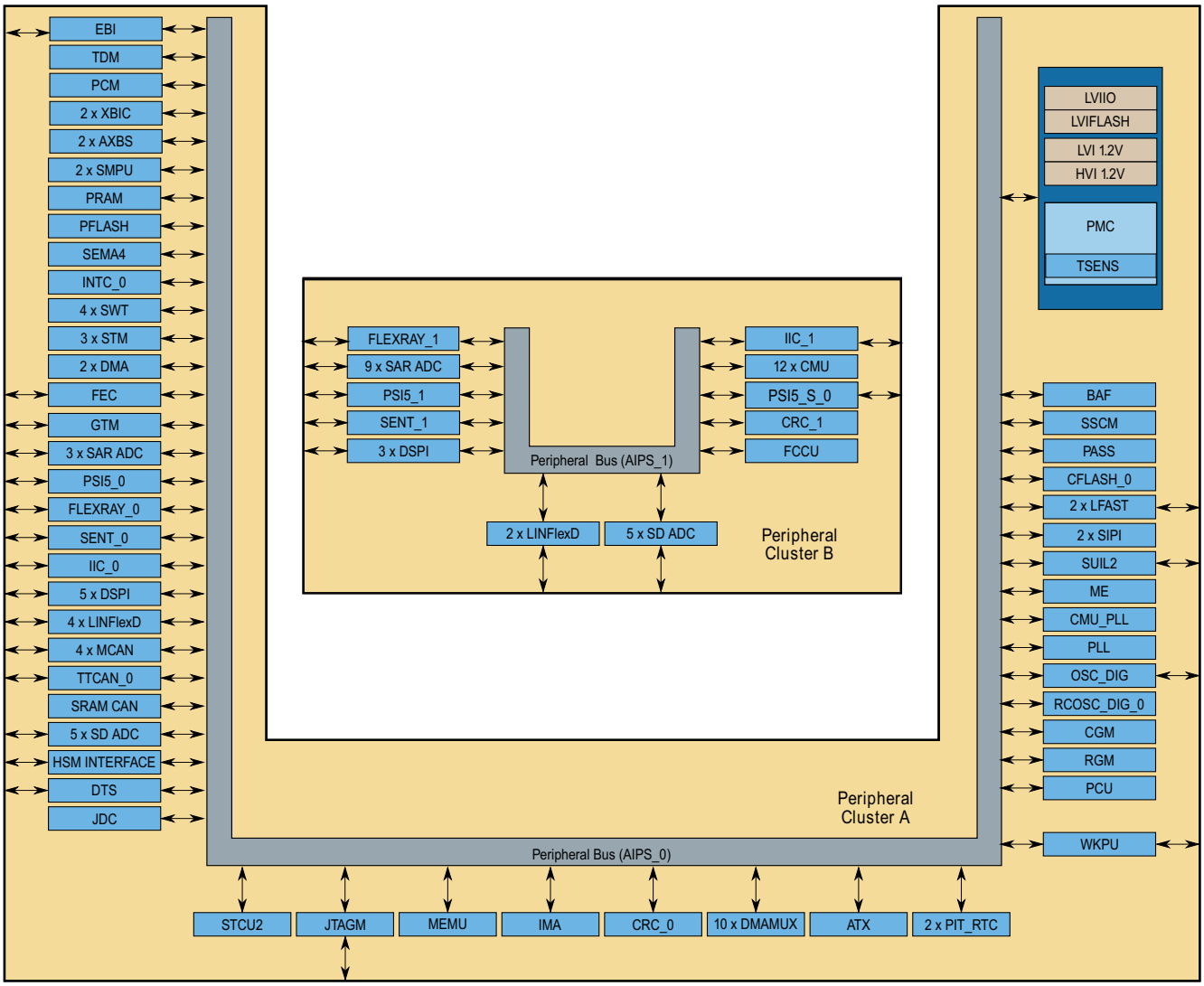

Figure 2. Periphery allocation

2 Package pinouts and signal descriptions

See the *MPC5777M Microcontroller Reference Manual* for signal information.

Table 4. LVDS pin descriptions (continued)

Functional block	Port pin	Signal	Signal description	Direction	BGA ball (416 PD, 416 ED)	BGA ball (512 PD, 512 ED)
Differential DSPI 2	PD[2]	SCK_P	Differential DSPI 2 Clock, LVDS Positive Terminal	O	C18	F17
	PD[3]	SCK_N	Differential DSPI 2 Clock, LVDS Negative Terminal	O	C17	G17
	PD[0]	SOUT_P	Differential DSPI 2 Serial Output, LVDS Positive Terminal	O	C16	F16
	PD[1]	SOUT_N	Differential DSPI 2 Serial Output, LVDS Negative Terminal	O	D17	G16
	PD[7]	SIN_P	Differential DSPI 2 Serial Input, LVDS Positive Terminal	I	G23	P24
	PF[13]	SIN_N	Differential DSPI 2 Serial Input, LVDS Negative Terminal	I	H23	R24
Differential DSPI 5	PF[10]	SCK_P	Differential DSPI 5 Clock, LVDS Positive Terminal	O	J24	W24
	PF[9]	SCK_N	Differential DSPI 5 Clock, LVDS Negative Terminal	O	K23	W25
	PF[12]	SOUT_P	Differential DSPI 5 Serial Output, LVDS Positive Terminal	O	J26	Y24
	PF[11]	SOUT_N	Differential DSPI 5 Serial Output, LVDS Negative Terminal	O	J25	Y25
	PD[7]	SIN_P	Differential DSPI 5 Serial Input, LVDS Positive Terminal	I	G23	P24
	PF[13]	SIN_N	Differential DSPI 5 Serial Input, LVDS Negative Terminal	I	H23	R24
	PI[15]	SIN_P	Differential DSPI 5 Serial Input, LVDS Positive Terminal	I	G24	P22
	PI[14]	SIN_N	Differential DSPI 5 Serial Input, LVDS Negative Terminal	I	J23	R22

1 DRCLK and TCK/DRCLK usage for SIPI LFAST and Debug LFAST are described in the *MPC5777M Microcontroller Reference Manual* SIPI LFAST and Debug LFAST chapters.

2 Pads use special enable signal form DCI block: DCI driven enable for Debug LFAST pads is transparent to user.

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

NOTE

Within this document, $V_{DD\_HV\_IO}$ refers to supply pins $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_IO\_FLEXE}$, $V_{DD\_HV\_IO\_EBI}$, and $V_{DD\_HV\_FLA}$. $V_{DD\_HV\_ADV}$ refers to ADC supply pins $V_{DD\_HV\_ADV\_S}$ and $V_{DD\_HV\_ADV\_D}$. $V_{DD\_HV\_ADR}$ refers to ADC reference pins $V_{DD\_HV\_ADR\_S}$ and $V_{DD\_HV\_ADR\_D}$. $V_{SS\_HV\_ADV}$ refers to ADC ground pins $V_{SS\_HV\_ADV\_S}$ and $V_{SS\_HV\_ADV\_D}$. $V_{SS\_HV\_ADR}$ refers to ADC reference pins $V_{SS\_HV\_ADR\_S}$ and $V_{SS\_HV\_ADR\_D}$.

3.2 Absolute maximum ratings

Table 6 describes the maximum ratings of the device.

Table 6. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
Cycle	SR	Lifetime power cycles	—	—	1000 k	—
V_{DD_LV}	SR	1.2 V core supply voltage[2,3,4]	—	–0.3	1.5	V
$V_{DD\_LV\_BD}$	SR	Emulation module voltage[2,3,4]	—	–0.3	1.5	V
$V_{DD\_HV\_IO}$	SR	I/O supply voltage[5,6]	—	–0.3	6.0	V
$V_{DD\_HV\_PMC}$	SR	Power Management Controller supply voltage[5]	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$	SR	Flash core voltage[7]	—	–0.3	4.5	V
V_{DDSTBY}	SR	RAM standby supply voltage[5]	—	–0.3	6.0	V
$V_{SS\_HV\_ADV}$[8]	SR	SAR and S/D ADC ground voltage	Reference to V_{SS_HV}	–0.3	0.3	V
$V_{DD\_HV\_ADV}$[9]	SR	SAR and S/D ADC supply voltage	Reference to corresponding $V_{SS\_HV\_ADV}$	–0.3	6.0	V
$V_{SS\_HV\_ADR}$[10]	SR	SAR and S/D ADC low reference	Reference to V_{SS_HV}	–0.3	0.3	V
$V_{DD\_HV\_ADR}$[11]	SR	SAR and S/D ADC high reference	Reference to corresponding $V_{SS\_HV\_ADR}$	–0.3	6.0	V
$V_{DD\_HV\_IO\_JTAG}$	SR	Crystal oscillator, FEC MDIO/MDC, LFAST, JTAG[5]	Reference to V_{SS_HV}	–0.3	6.0	V

Table 10. DC electrical specifications[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
I_{SR}[18]	CC	Current variation during power up/down	See footnote[19]	—	—	90	mA
I_{BG}	CC	Bandgap reference current consumption		—	—	600	µA
I_{DDOFF}	CC	Power-off current on high voltage supply rails[20]	V_{DD_HV} = 2.5 V	100	—	—	µA
V_{STBY_BO}	CC	Standby RAM brownout flag trip point voltage	—	—	—	0.9[21]	V
$V_{DD\_LV\_STBY\_SW}$	CC	Standby RAM switch VDD_LV voltage threshold	—	0.93	—	—	V
$V_{REF\_BG\_T}$	CC	Bandgap trimmed reference voltage	T_J = –40 °C to 150 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	1.200	—	1.237	V
$V_{REF\_BG\_TC}$	CC	Bandgap temperature coefficient[22]	T_J = –40 °C to 150 °C $V_{DD\_HV\_ADV}$ = 5 V	—	—	50	ppm/°C
$V_{REF\_BG\_LR}$	CC	Bandgap line regulation[22]	T_J = –40 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	—	—	8000	ppm/V
			T_J = 150 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	—	—	4000	

1 All parameters in this data sheet are valid for operation within an operating range of -40° C ≤ T_J≤ 150 °C except where otherwise noted

2 f_{MAX} as specified per IP. Excludes flash P/E and HSM dynamic current. Measured on an application specific pattern. Calculation of total current for the device, all rails, is done by adding the applicable dynamic currents to the I_{DD_LV} value for the core supply, and summing the currents based on use case for the 5 V blocks, for which current consumption values are defined in later sections of the DC electrical specification.

3 f_{MAX} as specified per IP. Excludes flash P/E and HSM dynamic current. Measured on an application specific pattern.

4 $V_{DD\_HV\_PMC}$ only available in the 416 BGA package. PMC supply is shorted to $V_{DD\_HV\_IO\_MAIN}$ in the 512 BGA, with an external bypass capacitor connected to the $V_{DD\_HV\_PMC\_BYP}$ ball. The flash read and P/E current, and PMC current apply to $V_{DD\_HV\_IO\_MAIN}$ for the 512 BGA.

5 The flash read and flash P/E currents are mutually exclusive, and are not cumulative.

6 This includes PMC consumption, LFAST PLL regulator current, and Nwell bias regulator current. If the V_{DD_LV} auxiliary regulator is enabled, the PMC supply may see short term (10 µs) spikes of up to 150 mA depending on transient current conditions from use case of the device. The auxiliary regulator can be disabled at power-up in the user DCF clients in the flash memory.

7 There is an additional 25 mA when FERS = 1 to enable the fast erase time of the flash memory.

8 Data is retained for full T_J range of -40 °C to 150 °C. RAM supply switch to the standby regulator occurs when the V_{DD_LV} supply falls below 0.95V.

Table 12. I/O input DC electrical characteristics (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
$V_{DRFTTTL}$	—	Input V_{IL}/V_{IH} temperature drift TTL	—	—	—	100	mV
AUTOMOTIVE							
V_{IHAUT}[2]	SR	Input high level AUTOMOTIVE	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	3.8	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ILAUT}[3]	SR	Input low level AUTOMOTIVE	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	–0.3	—	2.2	V
V_{HYSAUT}[4]	—	Input hysteresis AUTOMOTIVE	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.4	—	—	V
$V_{DRFTAUT}$	—	Input V_{IL}/V_{IH} temperature drift	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	100[5]	mV
CMOS/EBI							
V_{IHCMOS_H}[6]	SR	Input high level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.70 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
V_{IHCMOS}[6]	SR	Input high level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.6 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
V_{ILCMOS_H}[6]	SR	Input low level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	–0.3	—	0.35 * $V_{DD\_HV\_IO}$	V
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
V_{ILCMOS}[6]	SR	Input low level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	–0.3	—	0.4 * $V_{DD\_HV\_IO}$	V
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
$V_{HYSCMOS}$	—	Input hysteresis CMOS	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.1 * $V_{DD\_HV\_IO}$	—	—	V
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V[7]				
$V_{DRFTCMOS}$	—	Input V_{IL}/V_{IH} temperature drift CMOS	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	100[5]	mV
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
INPUT CHARACTERISTICS[8]							
I_{LKG}	CC	Digital input leakage	4.5 V < V_{DD_HV} < 5.5 V V_{SS_HV} < V_{IN} < V_{DD_HV} TJ = 150 °C	—	—	750	nA
I_{LKG_EBI}	CC	Digital input leakage for EBI pad	4.5 V < V_{DD_HV} < 5.5 V V_{SS_HV} < V_{IN} < V_{DD_HV} TJ = 150 °	—	—	750	nA
C_{IN}	CC	Digital input capacitance	GPIO input pins	—	—	7	pF
			EBI input pins	—	—	7	

1 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

Table 28. SDn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
$SNR_{DIFF333}$	CC	Signal to noise ratio in differential mode 333 ksps output rate	4.5 < $V_{DD\_HV\_ADV\_D}$ < 5.5[9,10,17] $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ GAIN = 1 T_J < 150 °C	74	—	—	dBFS
			4.5 < $V_{DD\_HV\_ADV\_D}$ < 5.5[9,10,17] $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ GAIN = 2 T_J < 150 °C	71	—	—	
			4.5 < $V_{DD\_HV\_ADV\_D}$ < 5.5[9,10,17] $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ GAIN = 4 T_J < 150 °C	68	—	—	
			4.5 < $V_{DD\_HV\_ADV\_D}$ < 5.5[9,10,17] $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ GAIN = 8 T_J < 150 °C	65	—	—	
			4.5 < $V_{DD\_HV\_ADV\_D}$ < 5.5[9,10,17] $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ GAIN = 16 T_J < 150 °C	62	—	—	
SNR_{SE150}	CC	Signal to noise ratio in single ended mode 150 ksps output rate[11]	4.5 < $V_{DD\_HV\_ADV\_D}$ < 5.5[9,10,17] $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ GAIN = 1 T_J < 150 °C	74	—	—	dBFS
			4.5 < $V_{DD\_HV\_ADV\_D}$ < 5.5[9,10,17] $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ GAIN = 2 T_J < 150 °C	71	—	—	
			4.5 < $V_{DD\_HV\_ADV\_D}$ < 5.5[9,10,17] $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ GAIN = 4 T_J < 150 °C	68	—	—	
			4.5 < $V_{DD\_HV\_ADV\_D}$ < 5.5[9,10,17] $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ GAIN = 8 T_J < 150 °C	65	—	—	
			4.5 < $V_{DD\_HV\_ADV\_D}$ < 5.5[9,10,17] $V_{DD\_HV\_ADR\_D}$=$V_{DD\_HV\_ADV\_D}$ GAIN = 16 T_J < 150 °C	62	—	—	
SFDR	CC	Spurious free dynamic range	GAIN = 1	60	—	—	dBc
			GAIN = 2	60	—	—	
			GAIN = 4	60	—	—	
			GAIN = 8	60	—	—	
			GAIN = 16	60	—	—	

[13] Impedance given at F_{ADCD_M}= 16 MHz. Impedance is inversely proportional to SDADC clock frequency. $Z_{DIFF}(F_{ADCD\_M})$ = (16 MHz / F_{ADCD_M}) * Z_{DIFF}, Z_{CM} (F_{ADCD_M}) = (16MHz / F_{ADCD_M}) * Z_{CM}.

[14] Input impedance in single-ended mode Z_{IN} = (2 * Z_{DIFF} * Z_{CM}) / (Z_{DIFF} + Z_{CM}).

[15] Impedance given at F_{ADCD_M}= 16 MHz. Impedance is inversely proportional to SDADC clock frequency. $Z_{DIFF}(F_{ADCD\_M})$ = (16 MHz / F_{ADCD_M}) * Z_{DIFF}, Z_{CM} (F_{ADCD_M}) = (16MHz / F_{ADCD_M}) * Z_{CM}.

[16] Vintcm is the common mode input reference voltage for the SDADC, and has a nominal value of ($V_{DD\_HV\_ADC}$ - $V_{SS\_HV\_ADC}$) / 2.

[17] SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} - f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency, and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.

[18] The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB.

[19] Propagation of the information from the pin to the register CDR[CDATA] and flags SFR[DFEF], SFR[DFFF] is given by the different modules that need to be crossed: delta/sigma filters, high pass filter, fifo module, clock domain synchronizers. The time elapsed between data availability at pin and internal S/D module registers is given by the below formula:

REGISTER LATENCY = tLATENCY + 0.5/fADCD_S + 2 (~+1)/fADCD_M + 2(~+1)fPBRIDGEx_CLK

where fADCD_S is the frequency of the sampling clock, fADCD_M is the frequency of the modulator, and fPBRIDGEx_CLK is the frequency of the peripheral bridge clock feeds to the ADC S/D module. The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing.
Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the ADC S/D module.

[20] This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.

3.11 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 29. Temperature sensor electrical characteristics

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
—	CC	Temperature monitoring range	—	–40	—	150	°C
T_{SENS}	CC	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	CC	Accuracy	$T_J < 150$ °C	–3	—	3	°C
I_{TEMP_SENS}	CC	$V_{DD\_HV\_ADV\_S}$ power supply current	—	—	—	700	µA

3.12 LVDS Fast Asynchronous Serial Transmission (LFAST) pad electrical characteristics

The LFAST pad electrical characteristics apply to both the SIPI and high-speed debug serial interfaces on the device. The same LVDS pad is used for the Microsecond Channel (MSC) and DSPI LVDS interfaces, with different characteristics given in the following tables.

3.14 Power management: PMC, POR/LVD, sequencing

3.14.1 Power management electrical characteristics

The power management module monitors the different power supplies. It also generates the internal supplies that are required for correct device functionality. The power management is supplied by the $V_{DD\_HV\_PMC}$ supply (see Table 8).

3.14.2 Power management integration

In order to ensure correct functionality of the device, it is recommended to follow below integration scheme.

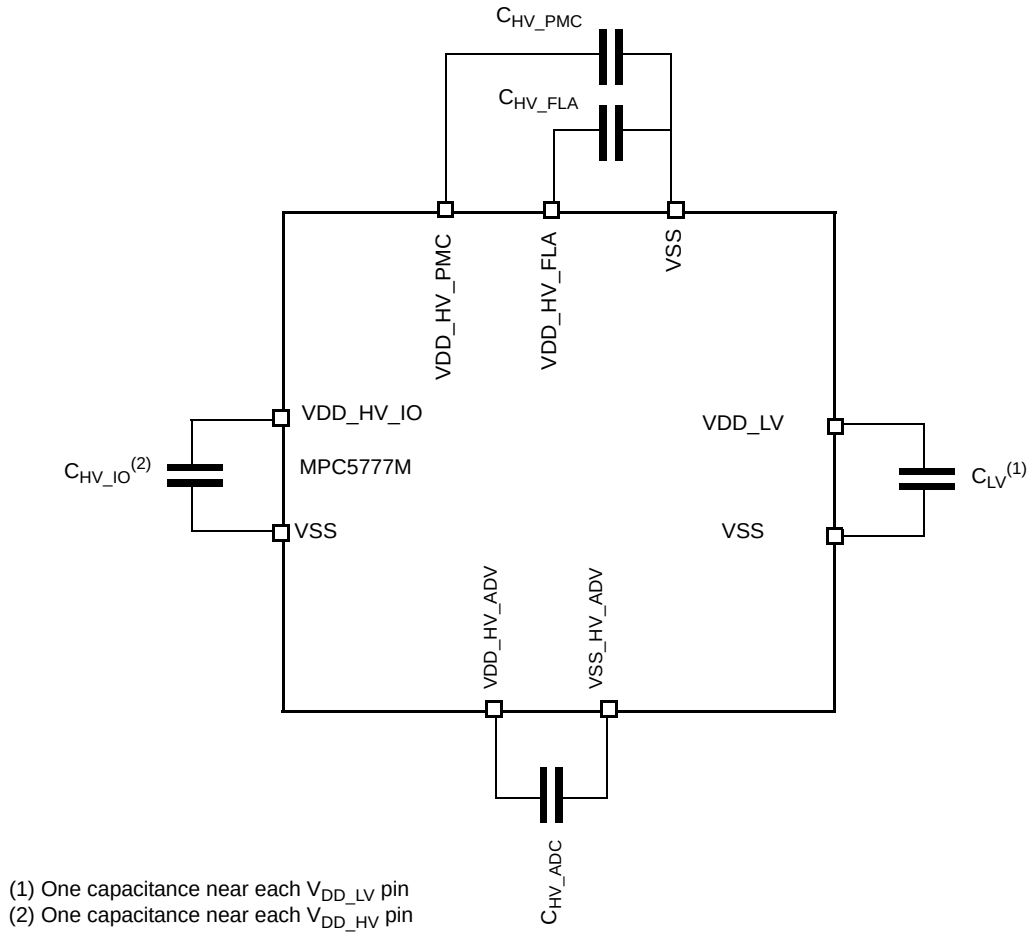

Figure 20. Recommended supply pin circuits

Table 47. Nexus debug port timing[1] (continued)

#	Symbol		Characteristic	Value		Unit
				Min	Max	
12	t_{NTDIH}	CC	TDI/TDIC data hold time	5	—	ns
13[9]	t_{NTMSS}	CC	TMS/TMSC data setup time	5	—	ns
14	t_{NTMSH}	CC	TMS/TMSC data hold time	5	—	ns
15[10]	—	CC	TDO/TDOC propagation delay from falling edge of TCK[11]	—	16	ns
16	—	CC	TDO/TDOC hold time with respect to TCK falling edge (minimum TDO/TDOC propagation delay)	2.25	—	ns

1 Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.

2 t_{CYC} is system clock period.

3 Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.

4 This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.

5 This value is TDO/TDOC propagation time 36ns + 4 ns setup time to sampling edge.

6 This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

7 This value is TDO/TDOC propagation time 16ns + 4 ns setup time to sampling edge.

8 TDIC represents the TDI bit frame of the scan packet in compact JTAG 2-wire mode.

9 TMSC represents the TMS bit frame of the scan packet in compact JTAG 2-wire mode.

10 TDOC represents the TDO bit frame of the scan packet in compact JTAG 2-wire mode.

11 Timing includes TCK pad delay, clock tree delay, logic delay and TDO/TDOC output pad delay.

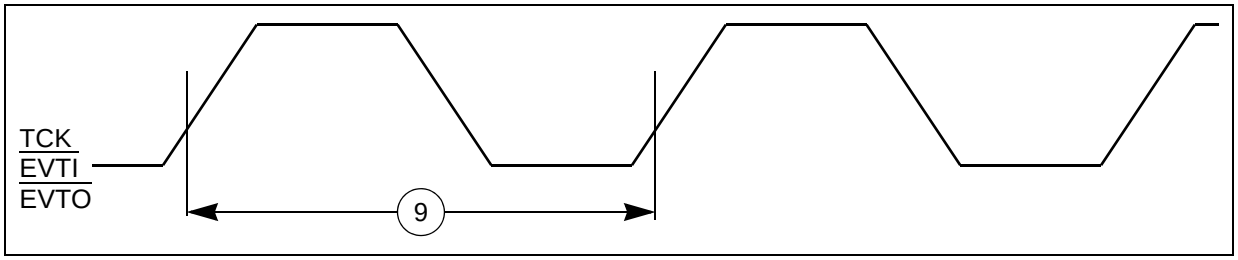

Figure 26. Nexus event trigger and test clock timings

Table 52. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
5	t_{PCSC}	CC	PCSx to $\overline{PCSS}$ time[8]	PCS and PCSS drive strength				
				Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	$\overline{PCSS}$ to PCSx time[8]	PCS and PCSS drive strength				
				Strong	25 pF	16.0	—	ns
SIN setup time								
7	t_{SUI}	CC	SIN setup time to SCK CPHA = 0[9]	SCK drive strength				
				Very strong	25 pF	$25 – (P^{10} \times t_{SYS}^{5})$	—	ns
				Strong	50 pF	$32.75 – (P^{10} \times t_{SYS}^{5})$	—	
				Medium	50 pF	$52 – (P^{10} \times t_{SYS}^{5})$	—	
			SIN setup time to SCK CPHA = 1[9]	SCK drive strength				
				Very strong	25 pF	25.0	—	ns
				Strong	50 pF	32.75	—	
				Medium	50 pF	52.0	—	
SIN hold time								
8	t_{HI}	CC	SIN hold time from SCK CPHA = 0[9]	SCK drive strength				
				Very strong	0 pF	$–1 + (P^{9} \times t_{SYS}^{4})$	—	ns
				Strong	0 pF	$–1 + (P^{9} \times t_{SYS}^{4})$	—	
				Medium	0 pF	$–1 + (P^{9} \times t_{SYS}^{4})$	—	
			SIN hold time from SCK CPHA = 1[9]	SCK drive strength				
				Very strong	0 pF	–1.0	—	ns
				Strong	0 pF	–1.0	—	
				Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	SOUT data valid time from SCK CPHA = 0[10]	SOUT and SCK drive strength				
				Very strong	25 pF	—	$7.0 + t_{SYS}^{5}$	ns
				Strong	50 pF	—	$8.0 + t_{SYS}^{5}$	
				Medium	50 pF	—	$16.0 + t_{SYS}^{5}$	
			SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength				
				Very strong	25 pF	—	7.0	ns
				Strong	50 pF	—	8.0	
				Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)								

Table 53. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol		Characteristic	Condition		Value[1]		Unit
				Pad drive	Load	Min	Max	
8	t_{HI}	CC	SIN Hold Time					
			SIN hold time from SCK CPHA = 0[6]	SCK drive strength				
				LVDS	0 pF differential	$-1 + (P^{7} \times t_{SYS}{}^{3})$	—	ns
			SIN hold time from SCK CPHA = 1[6]	SCK drive strength				
				LVDS	0 pF differential	–1	—	ns
9	t_{SUO}	CC	SOUT data valid time (after SCK edge)					
			SOUT data valid time from SCK CPHA = 0[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	—	$7.0 + t_{SYS}{}^{3}$	ns
			SOUT data valid time from SCK CPHA = 1[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	—	7.0	ns
10	t_{HO}	CC	SOUT data hold time (after SCK edge)					
			SOUT data hold time after SCK CPHA = 0[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	$-7.5 + t_{SYS}{}^{3}$	—	ns
			SOUT data hold time after SCK CPHA = 1[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	–7.5	—	ns

1 All timing values for output signals in this table are measured to 50% of the output voltage.

2 N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

3 t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).

4 M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

5 t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.

6 Input timing assumes an input slew rate of 1 ns (10% – 90%) and LVDS differential voltage = ±100 mV.

7 P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

3.16.2.1.4 DSPI Master Mode – Output Only

Table 55. DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1,2]

#	Symbol		Characteristic	Condition		Value		Unit
				Pad drive	Load	Min	Max	
1	t_{SCK}	CC	SCK cycle time	LVDS	15 pF to 50 pF differential	25.0	—	ns
2	t_{CSV}	CC	PCS valid after SCK[3] (SCK with 50 pF differential load cap.)	Very strong	25 pF	—	6.0	ns
				Strong	50 pF	—	10.5	ns
3	t_{CSH}	CC	PCS hold after SCK[3] (SCK with 50 pF differential load cap.)	Very strong	0 pF	–4.0	—	ns
				Strong	0 pF	–4.0	—	ns
4	t_{SDC}	CC	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$^1/_2t_{SCK}$ – 2	$^1/_2t_{SCK}$ + 2	ns
SOUT data valid time (after SCK edge)								
5	t_{SUO}	CC	SOUT data valid time from SCK[4]	SOUT and SCK drive strength				
				LVDS	15 pF to 50 pF differential	—	3.5	ns
SOUT data hold time (after SCK edge)								
6	t_{HO}	CC	SOUT data hold time after SCK[4]	SOUT and SCK drive strength				
				LVDS	15 pF to 50 pF differential	–3.5	—	ns

1 All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.

2 TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.

3 With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.

4 SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 56. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1,2]

#	Symbol		Characteristic	Condition		Value[3]		Unit
				Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	SCK cycle time	SCK drive strength				
				Very strong	25 pF	33.0	—	ns
				Strong	50 pF	80.0	—	ns
				Medium	50 pF	200.0	—	ns

Table 56. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1,2] (continued)

#	Symbol		Characteristic	Condition		Value[3]		Unit
				Pad drive[4]	Load (C_L)	Min	Max	
2	t_{CSV}	CC	PCS valid after SCK[5]	SCK and PCS drive strength				
				Very strong	25 pF	7	—	ns
				Strong	50 pF	8	—	ns
				Medium	50 pF	16	—	ns
				PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	29	—	ns
3	t_{CSH}	CC	PCS hold after SCK[5]	SCK and PCS drive strength				
				Very strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
				Strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
				Medium	PCS = 0 pF SCK = 50 pF	–33	—	ns
				PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	–35	—	ns
4	t_{SDC}	CC	SCK duty cycle[6]	SCK drive strength				
				Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
				Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
				Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	SOUT data valid time from SCK CPHA = 1[7]	SOUT and SCK drive strength				
				Very strong	25 pF	—	7.0	ns
				Strong	50 pF	—	8.0	ns
				Medium	50 pF	—	16.0	ns
SOUT data hold time (after SCK edge)								
10	t_{HO}	CC	SOUT data hold time after SCK CPHA = 1[7]	SOUT and SCK drive strength				
				Very strong	25 pF	–7.7	—	ns
				Strong	50 pF	–11.0	—	ns
				Medium	50 pF	–15.0	—	ns

1 TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.

2 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

3 All timing values for output signals in this table are measured to 50% of the output voltage.

4 Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.

5 With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.

Table 68. UART frequency support

LINFlexD clock frequency LIN_CLK (MHz)	Oversampling rate	Voting scheme	Max usable frequency (Mbaud)
80	16	3:1 majority voting	5
	8		10
	6	Limited voting on one sample with configurable sampling point	13.33
	5		16
	4		20
100	16	3:1 majority voting	6.25
	8		12.5
	6	Limited voting on one sample with configurable sampling point	16.67
	5		20
	4		25

3.16.7 External Bus Interface (EBI) Timing

Table 69. Bus Operation Timing[1]

Spec	Characteristic	Symbol	66.7 MHz (Ext. Bus Freq)[2 3]		Unit
			Min	Max	
1	CLKOUT Period[4]	t_C	15.15	—	ns
2	CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C
3	CLKOUT Rise Time	t_{CRT}	—	—[5]	ns
4	CLKOUT Fall Time	t_{CFT}	—	—[5]	ns
5	CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time)[6] ADDR[12:31] ADDR[8:11]/WE[0:3]/BE[0:3] BDIP CS[0:3] DATA[0:31] OE RD_WR TS	t_{COH}	1.0	—	ns
6	CLKOUT Posedge to Output Signal Valid (Output Delay)[7,8] ADDR[12:31] ADDR[8:11]/WE[0:3]/BE[0:3] BDIP CS[0:3] DATA[0:31] OE RD_WR TS	t_{COV}	—	8.0	ns

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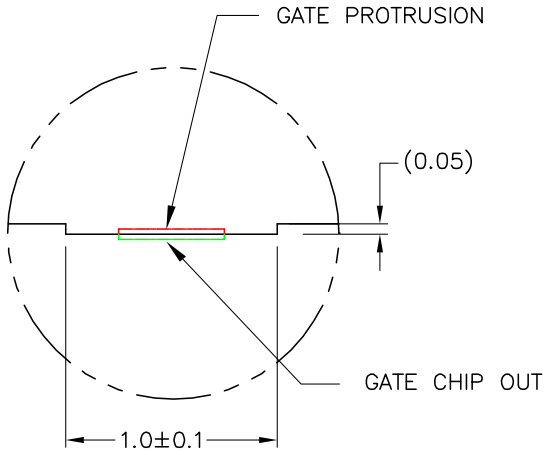

DETAIL A

TITLE: TEPBGA–I 27 X 27 X 2.23 PKG 1 MM PITCH, 416 I/O	CASE NUMBER:	2309–01
	STANDARD:	JEDEC MS–034 AAL–1
	SHEET:	2

Figure 57. 416 TEPBGA (emulation) package mechanical drawing (Sheet 2 of 3)

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Package pinouts and signal descriptions**
		Section 2.1, Package pinouts: • Removed “292” from the first sentence. • Removed figure “292-ball BGA production device pinout (top view)” and figure “292-ball BGA production device pinout (bottom view)”. Table 2 (Power supply and reference pins) and Table 3 (System pins): • Removed the “292PD” and 292ED” BGA ball columns. • V_{SS_LV}: Added K13 and K14 for 416PD/416ED. Added M15 and M16 for 512PD/512ED. • $V_{DD\_LV\_BD}$: R1/R4 now applies only to 416ED (416PD changed to “—”). M13/N12 now applies only to 512ED (512PD changed to “—”). • Removed $V_{DD\_HV\_OSC}$ row. • Changed $V_{DD\_HV\_JTAG}$ Description to "JTAG/Oscillator power supply." • V_{DDSTBY}: removed "Input" from descripion. • Significantly revised $V_{SS\_HV\_ADV\_S}$, $V_{DD\_HV\_ADV\_S}$, $V_{SS\_HV\_ADV\_D}$, and $V_{DD\_HV\_ADV\_D}$ rows. Added rows for $V_{SS\_HV\_ADR\_S}$, $V_{DD\_HV\_ADR\_S}$, $V_{SS\_HV\_ADR\_D}$, $V_{DD\_HV\_ADR\_D}$. Table 4 (LVDS pin descriptions): • Changed title to “LVDS pin descriptions” (was “LVDSM”). • Removed the “292 PD, 292 ED” BGA ball column. • In the BGA ball (416 PD,416 ED) column, added ball locations. • In the BGA ball (512 PD, 512 ED) column, added ball locations. • Changed SIPI_TXP to P25 for 512BGA (was T25). • DSPI 4: Changed SCK_N to G17 for 512BGA (was G18). • DSPI 2: Changed SIN_P to G23 for 416BGA (was D17). • DSPI 5: For SCK_P, changed PI[15] to PF[10], G26 to J24, and P22 to W24. • DSPI 5: For SCK_N, changed PI[15] to PF[9], J23 to K23, and R22 to W25. • Added another pair of SIN_P/SIN_N rows for DSPI_5.
		Electrical characteristics—Absolute maximum ratings
		Section 3.1, Introduction: • Added $V_{DD\_HV\_IO\_FLEXE}$ and $V_{DD\_HV\_IO\_EBI}$ to list in supply pins note. Table 7 (Parameter classifications): • Changed Tag description for C classification to “Parameters are guaranteed. . .” (was “Those parameters are achieved. . .” • Changed Tag description for T classification to “Parameters are guaranteed. . .” (was “Those parameters are achieved. . .” Table 6 (Absolute maximum ratings): • Changed V_{SS} to V_{SS_HV}. • Removed “$V_{SS} – V_{SS\_HV\_ADV}$” parameter row. • Removed V_{FERS} row. • Removed “V_{FERS} is a factory test supply pin . . .” footnote. • $V_{SS\_HV\_ADR}$: Added "Reference to V_{SS_HV}" to Conditions field. • Removed V_{SS}–$V_{SS\_HV\_ADR\_D}$ and V_{SS}–$V_{SS\_HV\_ADR\_S}$ rows. • In $V_{DD\_HV\_IO}$ footnote, added $V_{DD\_HV\_IO\_JTAG}$ to list of power supplies to which $V_{DD\_HV\_IO}$ applies. • In ADC grounds footnote, removed $V_{SS\_HV\_ADV\_D2}$. • In ADC supplies footnote, changed $V_{DD\_HV\_ADV}$ to $V_{DD\_HV\_ADV\_S}$. • In ADC low and high references footnote, removed $V_{SS\_HV\_ADR\_D2}$ and $V_{DD\_HV\_ADR\_D2}$. • In ADC supplies footnote, removed $V_{DD\_HV\_ADV\_D2}$. Table 7 (ESD ratings,): • Changed ESD for Human Body Model (HBM) parameter classification to “T” (was SR)

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—AC specifications—Fast Ethernet Controller (FEC)**
		Table 61 (MII serial management channel timing): • Added footnote to “Value” column: **“**Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.” Table 63 (RMII transmit signal timing,): • Added footnote to “Value” column **“**Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.” • Added footnote to table title: “RMII timing is valid only up to a maximum of 150 ^{o}C junction temperature.”
		Electrical characteristics—AC specifications—FlexRay
		Section 3.16.4, FlexRay timing: • Removed reference to “292 MAPBGA”. • Removed “ . . . and subject to change per the final timing analysis of the device” from FlexRay specification sentence. Table 66 (RxD input characteristics): • Added footnote: “FlexRay RxD timing is valid for all input levels and hysteresis disabled."
		Electrical characteristics—AC specifications—EBI
		Table 69 (Bus Operation Timing): • Changed bus frequency in table heading to “66.7 MHz” (was “66 MHz”). • Footnote 1, added "with DSC = 0b10 for ADDR/CTRL and DSC = 0b11 for CLKOUT/DATA." • Footnote 3, changed “[Clock Register TBD]” TO “CGM_SC_DC4 register”. • Footnote 4, changed "VDDE" to "VDD_HV_IO_EBI or VDD_HV_IO_FLEXE." • Spec 5, Characteristic column, added “ADDR[8:11]/WE[0:3]/BE[0:3],” “BDIP,” and overbar on CS, OE, and TS. Changed "ADDR[8:31]" to "ADDR[12:31]." • Spec 6, Characteristic column, added “ADDR[8:11]/WE[0:3]/BE[0:3]”, “BDIP,” overbar on CS, OE, TS, and footnote “One wait state must be added to the output signal valid delay for external writes.” Changed "ADD[8:31]" to "ADDR[12:31]." • Spec 7, change Min value from “6.0” to “7.0” ns. • Spec 8, Characteristic column, changed to “DATA[0:31]”. • Removed cut 1 footnotes associated with output delay and setup time (total 2). Figure 50 (D_CLKOUT Timing) Figure 51 (Synchronous Output Timing) Figure 52 (Synchronous Input Timing): • Changed “VDDE” to “VDD_HV_IO_EBI” throughout.
		Electrical characteristics—AC specifications—I2C
		Section 3.16.8, “I2C timing: New section.
		Electrical characteristics—AC specifications—GPIO delay
		Section 3.19.10, GPIO delay timing • New section