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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Tri-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRAY, I²C, LINbus, SPI, PSI, UART/USART
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	8.64MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	404K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12b SAR, 16b Sigma-Delta
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	512-FBGA
Supplier Device Package	512-FBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777mk0mva8r

Table 1. MPC5777M feature (continued)

Feature	MPC5777M
ADC (SD)	10
Temperature sensor	Yes
Self test controller	Yes
PLL	Dual PLL with FM
Integrated linear voltage regulator	None
External power supplies	5 V 3.3 V[7] 1.2 V
Low-power modes	Stop mode Slow mode
Packages	• 416 TEPBGA[4] • 512 TEPBGA[5]

1 Includes four user-programmable CPU cores and one safety core. The main computational shell consists of dual e200z7 CPUs operating at 300 MHz with a third identical core running as a safety checker core in delayed lockstep mode with one of the dual e200z7 cores. The I/O subsystem includes a CPU targeted at managing the peripherals. This is an e200z4 CPU running at 200 MHz. The fifth CPU is an e200z0 running at 100 MHz and is embedded in the Hardware Security Module. All CPUs are compatible with the Power Architecture.

2 LVDS Fast Asynchronous Serial Transmission

3 BOSCH® is a registered trademark of Robert Bosch GmbH.

4 416 TEPBGA package supports development and production applications with the same package footprint.

5 512 TEPBGA package supports development and production applications with the same package footprint.

1.4 Block diagram

The figures below show the top-level block diagrams.

Figure 1. Block diagram

Table 17. VERY STRONG configuration output buffer electrical characteristics[1]

Symbol		Parameter	Conditions[2,3]	Value			Unit
				Min	Typ	Max	
R_{OH_V}	CC	PMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1 I_{OH} = 8 mA	20	40	72	Ω
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OH} = 7 mA[4]	30	50	90	
R_{OL_V}	CC	NMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1 I_{OL} = 8 mA	20	40	72	Ω
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OL} = 7 mA[4]	30	50	90	
f_{MAX_V}	CC	Output frequency VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	—	—	50	MHz
			VSIO[VSIO_xx] = 1, C_L = 15 pF[4,5]	—	—	50	
$t_{TPD50\text{-}50}$[6]	CC	50-50 % Output pad propagation delay time	$V_{DD\_HV\_IO}$ = 5 V +/- 10 %, C_L = 25 pF	—	—	5.5	ns
			$V_{DD\_HV\_IO}$ = 5.0 V +/- 10 %, C_L = 50 pF	—	—	6.5	ns
			$V_{DD\_HV\_IO}$ = 3.3 V +/- 10 %, C_L = 15 pF	—	—	7.3/7.6	ns
t_{TR_V}	CC	10–90% threshold transition time output pin VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	1	—	5.3	ns
			$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 50 pF[5]	3	—	12	
			$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 200 pF[5]	14	—	45	
$t_{TR20\text{-}80}$	CC	20–80% threshold transition time[7] output pin VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	0.8	—	4	ns
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 15 pF[5]	1	—	5	
t_{TRTTL}	CC	TTL threshold transition time[8] for output pin in VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 25 pF[5]	1	—	5	ns
$\Sigma t_{TR20\text{-}80}$	CC	Sum of transition time 20–80% output pin VERY STRONG configuration[9]	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF	—	—	9	ns
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 15 pF[5]	—	—	9	
$\lvert t_{SKEW\_V} \rvert$	CC	Difference between rise and fall time at 20–80%	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	0	—	1	ns

[2] During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characterstics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

[3] Stated maximum values represent peak consumption that lasts only a few ns during I/O transition. When possible (timed output) it is recommended to delay transition between pads by few cycles to reduce noise and consumption.

[4] For $I_{DYN\_EBI\_GPIO}$ dynamic current for EBI GPIO mode use the I_{DYN_M} values.

3.8 Reset pad ($\overline{\text{PORST}}$, $\overline{\text{ESR0}}$) electrical characteristics

The device implements a dedicated bidirectional reset pin ($\overline{\text{PORST}}$).

NOTE

$\overline{\text{PORST}}$ pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 kΩ.

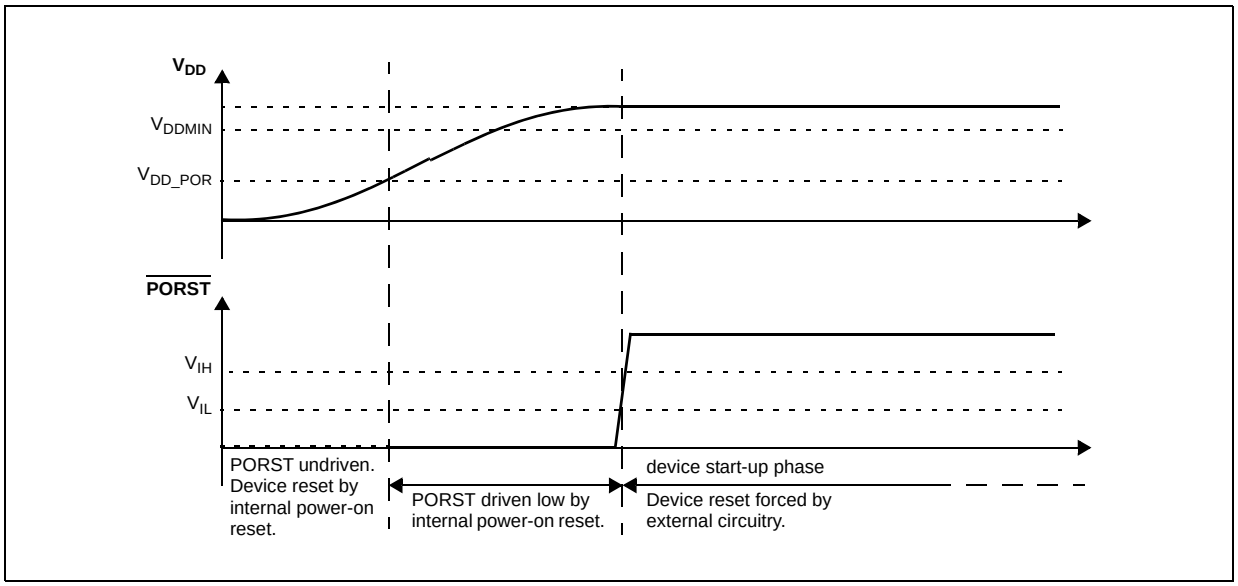


Figure 10. Start-up reset requirements

Figure 11 describes device behavior depending on supply signal on $\overline{\text{PORST}}$:

1. $\overline{\text{PORST}}$ low pulse amplitude is too low—it is filtered by input buffer hysteresis. Device remains in current state.
2. $\overline{\text{PORST}}$ low pulse duration is too short—it is filtered by a low pass filter. Device remains in current state.
3. $\overline{\text{PORST}}$ low pulse generates a reset:
   a) $\overline{\text{PORST}}$ low but initially filtered during at least W_{FRST}. Device remains initially in current state.
   b) $\overline{\text{PORST}}$ potentially filtered until W_{NFRST}. Device state is unknown: it may either be reset or remains in current state depending on other factors (temperature, voltage, device).
   c) $\overline{\text{PORST}}$ asserted for longer than W_{NFRST}. Device is under reset.

Table 23. External Oscillator electrical specifications[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
f_{XTAL}	CC	Crystal Frequency Range[2]	—	4	8	MHz
			—	>8	20	
			—	>20	40	
t_{cst}	CC	Crystal start-up time [3,4]	T_J = 150 °C	—	5	ms
t_{rec}	CC	Crystal recovery time[5]	—	—	0.5	ms
V_{IHEXT}	CC	EXTAL input high voltage[6,7] (External Clock Input)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$	V_{REF} + 0.6	—	V
V_{ILEXT}	CC	EXTAL input low voltage[6,7] (External Clock Input)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$	—	V_{REF} - 0.6	V
C_{S_xtal}	CC	Total on-chip stray capacitance on XTAL/EXTAL pins[8]	BGA416, BGA512	8	8.6	pF
V_{EXTAL}	CC	Oscillation Amplitude on the EXTAL pin after startup[9]	T_J = –40 °C to 150 °C	0.5	1.6	V
V_{HYS}	CC	Comparator Hysteresis	T_J = –40 °C to 150 °C	0.1	1.0	V
I_{XTAL}	CC	XTAL current[13,10]	T_J = –40 °C to 150 °C	—	14	mA

1 All oscillator specifications are valid for VDD_HV_IO_JTAG = 3.0 V – 5.5 V.

2 The range is selectable by UTEST miscellaneous DCF clients XOSC_LF_EN and XOSC_EN_40MHZ.

3 This value is determined by the crystal manufacturer and board design.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.

6 This parameter is guaranteed by design rather than 100% tested.

7 Applies to an external clock input and not to crystal mode.

8 See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.

9 Amplitude on the EXTAL pin after startup is determined by the ALC block, i.e., the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.

10 I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2–3 mA range and is dependent on the load and series resistance of the crystal. Test circuit is shown in Figure 13.

3.10 ADC specifications

3.10.1 ADC input description

Figure 14 shows the input equivalent circuit for fast SARn channels.

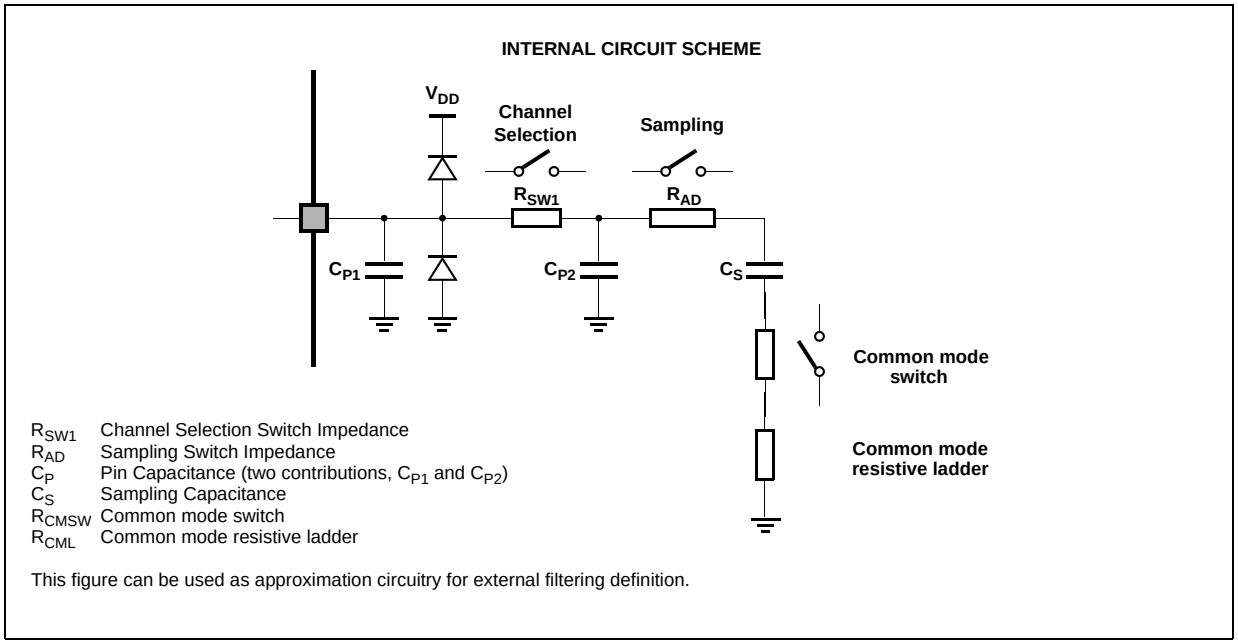


Figure 14. Input equivalent circuit (Fast SARn channels)

Figure 15 shows the input equivalent circuit for SARB channels.

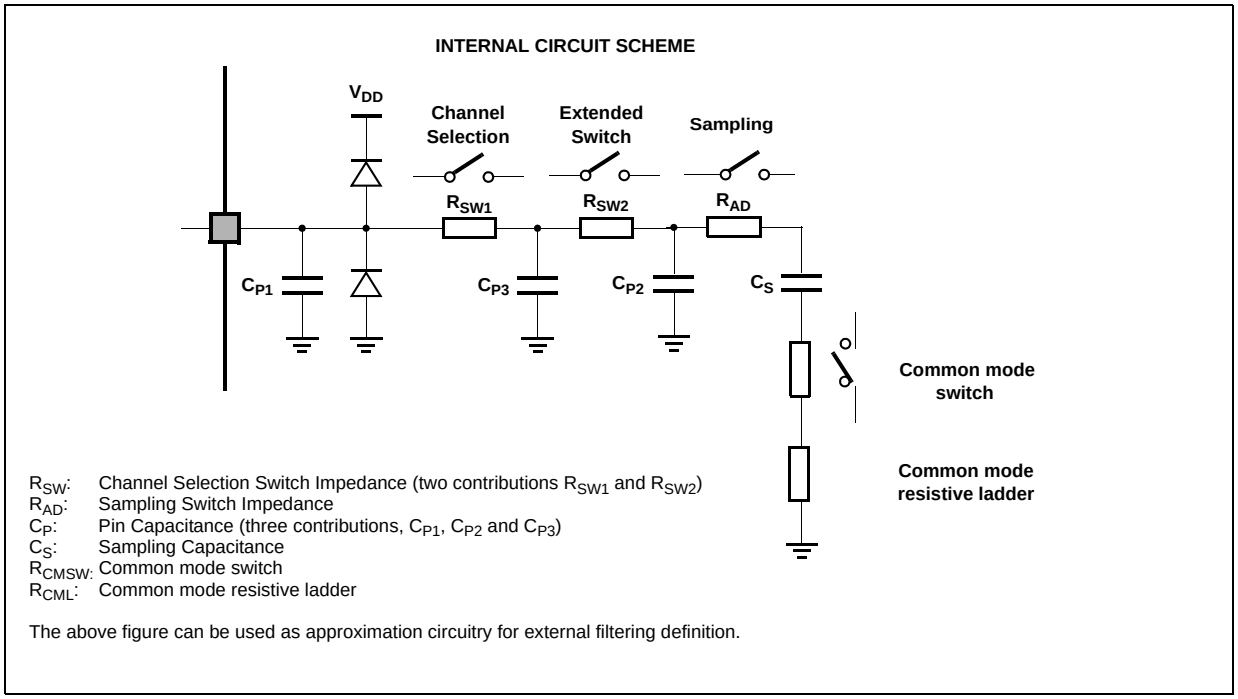


Figure 15. Input equivalent circuit (SARB channels)

Table 27. SARn ADC electrical specification[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{ALTREF}	SR	ADC alternate reference voltage	$V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$	2.0	$V_{DD\_HV\_ADV\_S}$	V
V_{IN}	SR	ADC input signal	$0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$V_{SS\_HV\_ADR\_S}$	$V_{DD\_HV\_ADR\_S}$	V
f_{ADCK}	SR	Clock frequency	$T_J < 150$ °C	7.5	14.6	MHz
$t_{ADCPRECH}$	SR	ADC precharge time	Fast SAR—fast precharge	135	—	ns
			Fast SAR—full precharge	270	—	
			Slow SAR (SARADC_B)—fast precharge	270	—	
			Slow SAR (SARADC_B)—full precharge	540	—	
ΔV_{PRECH}	SR	Precharge voltage precision	Full precharge $V_{PRECH} = V_{DD\_HV\_ADR\_S}/2$ $T_J < 150$ °C	–0.25	0.25	V
			Fast precharge $V_{PRECH} = V_{DD\_HV\_ADR\_S}/2$ $T_J < 150$ °C	–0.5	0.5	V
ΔV_{INTREF}	CC	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR\_S}$, 1/3 * $V_{DD\_HV\_ADR\_S}$, 2/3 * $V_{DD\_HV\_ADR\_S}$, $V_{DD\_HV\_ADR\_S}$)	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	ADC sample time[2]	Fast SAR – 12-bit configuration	0.750	—	µs
			Slow SAR (SARADC_B) – 12-bit configuration	1.500	—	
$t_{ADCEVAL}$	SR	ADC evaluation time	12-bit configuration (25 clock cycles)	1.712	—	µs
$I_{ADCREFH}$[3,4]	CC	ADC high reference current	Run mode $t_{conv} \geq 5$ µs (average across all codes)	—	7	µA
			Run mode $t_{conv} = 2.5$ µs (average across all codes)	—	7	
			Power Down mode	—	6	
			Bias Current[5]	—	+2	
$I_{ADCREFL}$[4]	CC	ADC low reference current	Run mode $t_{conv} \geq 5$ µs $V_{DD\_HV\_ADR\_S}$ <= 5.5 V	—	15	µA
			Run mode $t_{conv} = 2.5$ µs $V_{DD\_HV\_ADR\_S}$ <= 5.5 V	—	30	
			Power Down mode $V_{DD\_HV\_ADR\_S}$ <= 5.5 V	—	1	

Table 28. SDn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Z_{DIFF}	D	Differential Input impedance[12][13]	GAIN=1	1000	1250	1500	kΩ
			GAIN=2	600	800	1000	
			GAIN=4	300	400	500	
			GAIN=8	200	250	300	
			GAIN=16	200	250	300	
Z_{CM}	D	Common Mode Input impedance[14] [15]	GAIN=1	1400	1800	2200	kΩ
			GAIN=2	1000	1300	1600	
			GAIN=4	700	950	1150	
			GAIN=8	500	650	800	
			GAIN=16	500	650	800	
R_{BIAS}	D	Bare Bias resistance	—	110	144	180	kΩ
ΔV_{INTCM}	D	common mode input reference voltage[16]	—	-12	—	+12	%
V_{BIAS}	CC	Bias voltage	—	—	$V_{DD\_HV\_ADR\_D}/2$	—	V
δV_{BIAS}	CC	Bias voltage accuracy	—	–2.5	—	+2.5	%
V_{cmrr}	SR	Common mode rejection ratio	—	54	—	—	dB
R_{Caaf}	SR	Anti-aliasing filter	External series resistance	—	—	20	kΩ
	CC		Filter capacitances	180	—	—	pF
$f_{PASSBAND}$	CC	Pass band[17]	—	0.01	—	0.333 * f_{ADCD_S}	kHz
δ_{RIPPLE}	CC	Pass band ripple[18]	0.333 * f_{ADCD_S}	–1	—	1	%
$F_{rolloff}$	CC	Stop band attenuation	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
			[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	45	—	—	
			[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	50	—	—	
			[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	55	—	—	
			[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	60	—	—	

Table 34. Aurora LVDS electrical characteristics[1,2] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
C_{ac_tx}	SR	Transmit Lane External AC Coupling Capacitance	Values are nominal, valid for +/– 50% tolerance	250	—	2000	pF
Receiver							
F_{RX}	CC	Receive Clock Rate	T_J = 150 °C	—	—	1.25	Gbps
$\|\Delta V_{I\_L}\|$	SR	Differential input voltage (peak to peak)	—	200	—	1000	mV
$R_{V\_L\_Rx}$	CC	Differential Terminating resistance	—	81	100	120	Ω

1 All Aurora electrical characteristics are valid from –40 °C to 150 °C, except where noted.

2 All specifications valid for maximum transmit data rate F_{TX}.

3 The minimum value of 400 mV is only valid for differential terminating resistance (R_{V_L}) = 99 ohm to 101 ohm. The differential output voltage swing tracks with the value of R_{V_L}.

4 Transmission line loss maximum value is specified for the maximum drive level of the Aurora transmit pad.

Table 40 shows the estimated Program/Erase times.

Table 40. Flash memory program and erase specifications (pending characterization)

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3,4]		Field Update			Units
			Initial Max	Initial Max Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C≤ T_a ≤ 30°C	-40°C≤ T_J ≤ 150°C	-40°C≤ T_J ≤ 150 °C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgn}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgn}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1.200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1 Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.

2 Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.

3 Conditions: ≤ 150 cycles, nominal voltage.

4 Plant Programming times provide guidance for timeout limits used in the factory.

5 Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.

6 Conditions: -40°C≤ T_J ≤ 150°C; full spec voltage.

3.15.3 Flash memory Array Integrity and Margin Read specifications

Table 42. Flash memory Array Integrity and Margin Read specifications (characterized but not tested)

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16KB block.	—	—	512 × Tperiod × Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32KB block.	—	—	1024 × Tperiod × Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64KB block.	—	—	2048 × Tperiod × Nread	—
$t_{ai256kseq}$	Array Integrity time for sequential sequence on 256KB block.	—	—	8192 × Tperiod × Nread	—
$t_{aifullseq}$	Array Integrity time for sequential sequence full array.	—	—	3.77e5 × Tperiod × Nread	—
$t_{aifullprop}$	Array Integrity time for proprietary sequence (applies to full array or single block).	—	—	9.96e6 × Tperiod × Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256KB block.	893.01	—	1,339.5	µs
t_{mrfull}	Margin Read time for sequential sequence full array.	45.21	—	60.26	ms

1 Array Integrity times need to be calculated and are dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)

2 The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

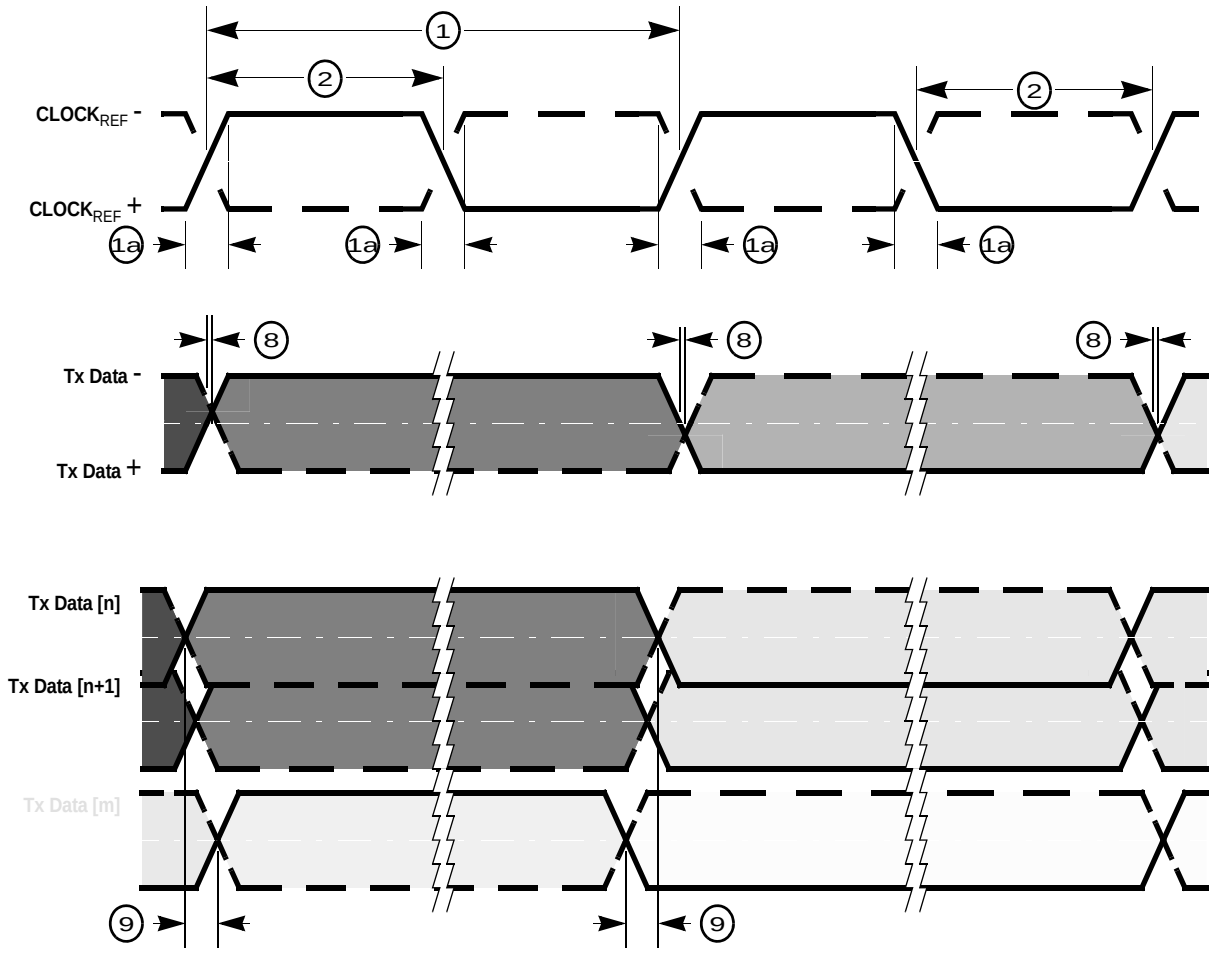


Figure 28. Aurora timings

Table 57. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)[1]

#	Symbol		Characteristic	Condition		Min	Max	Unit
				Pad Drive	Load			
11	t_{SUO}	CC	SOUT Valid Time[2,3,4] (after SCK edge)	Very Strong	25 pF	—	30	ns
				Strong	50 pF	—	30	ns
				Medium	50 pF	—	50	ns
12	t_{HO}	CC	SOUT Hold Time[2,3,4] (after SCK edge)	Very Strong	25 pF	2.5	—	ns
				Strong	50 pF	2.5	—	ns
				Medium	50 pF	2.5	—	ns

1 DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only.

2 Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.

3 All timing values for output signals in this table, are measured to 50% of the output voltage.

4 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

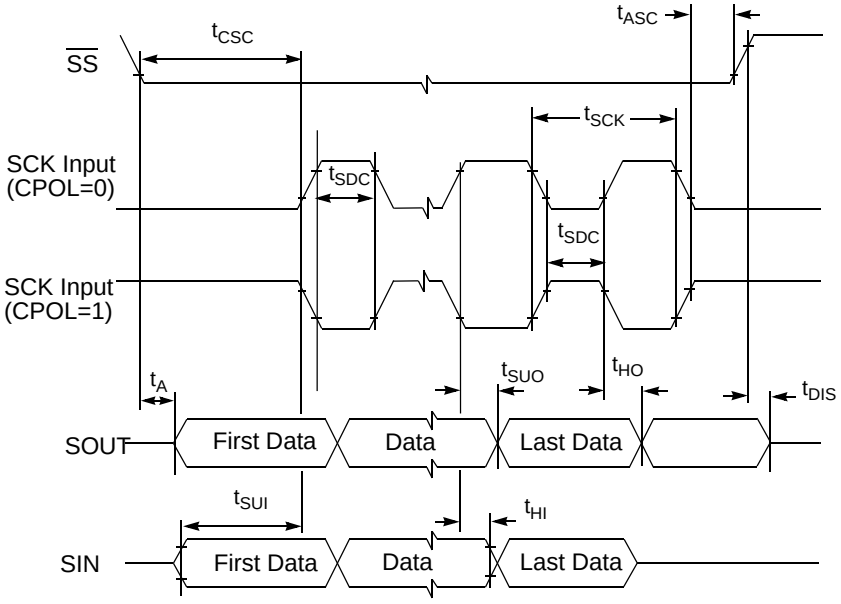


Figure 38. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 0

Table 65. TxD output characteristics[1,2]

Symbol		Characteristic	Value		Unit
			Min	Max	
dCCTxAsym	CC	Asymmetry of sending CC at 25 pF load (= $dCCTxD_{50\%}$ − 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	CC	Sum of Rise and Fall time of TxD signal at the output pin[3,4]	—	9[5]	ns
			—	9[6]	
$dCCTxD_{01}$	CC	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	CC	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1 TxD pin load maximum 25 pF

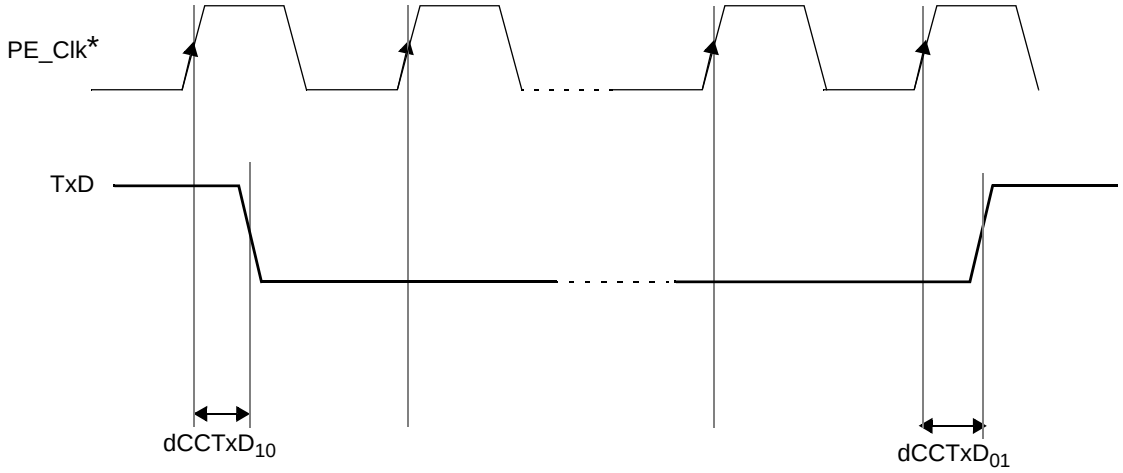
2 Specifications valid according to FlexRay EPL 3.0.1 standard with 20%–80% levels and a 10pF load at the end of a 50 Ohm, 1 ns stripline. Please refer to the Very Strong I/O pad specifications.

3 Pad configured as VERY STRONG

4 Sum of transition time simulation is performed according to Electrical Physical Layer Specification 3.0.1 and the entire temperature range of the device has been taken into account.

5 $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF

6 $V_{DD\_HV\_IO}$ = 3.3 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 0.6 ns, C_L = 10 pF



* FlexRay Protocol Engine Clock

Figure 49. TxD Signal propagation delays

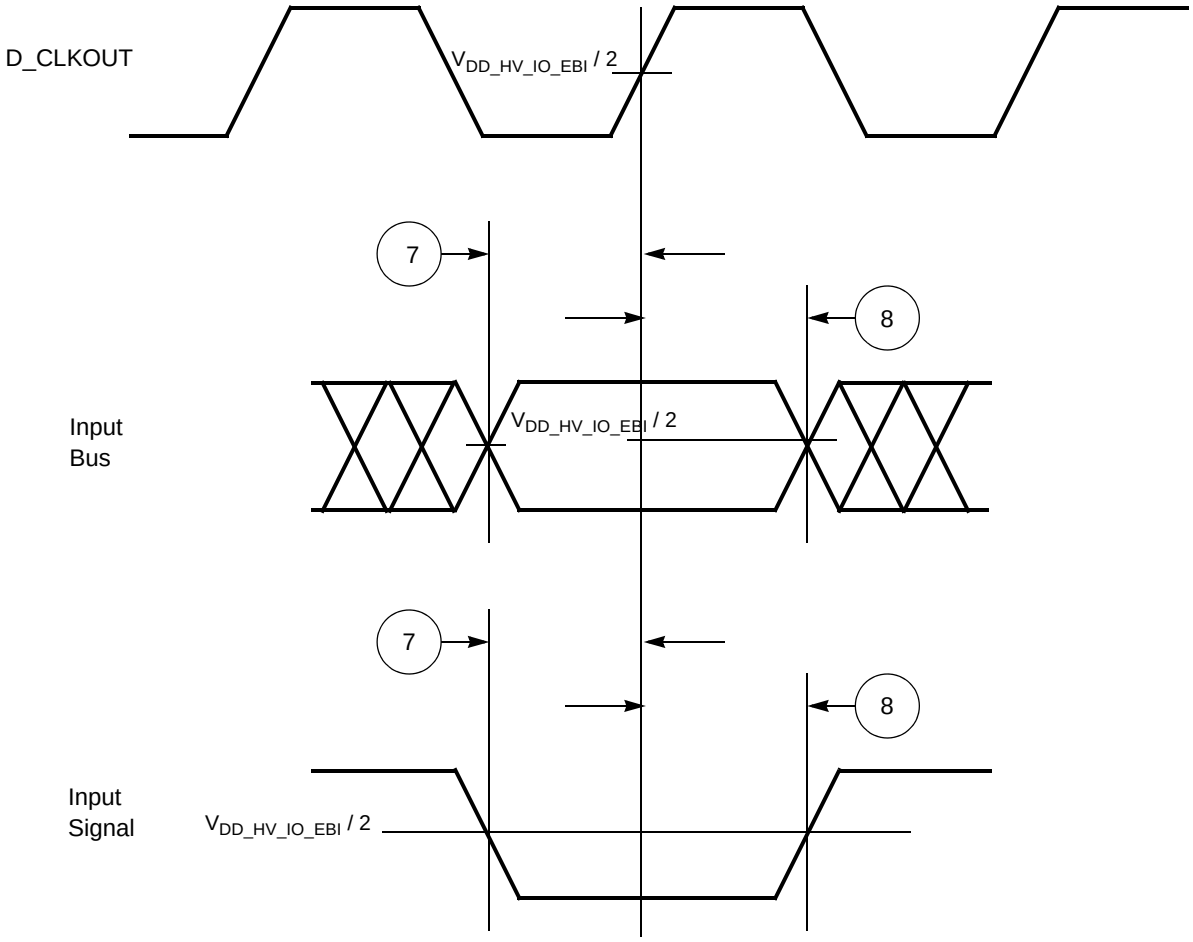


Figure 52. Synchronous Input Timing

3.16.8 I²C timing

The I²C AC timing specifications are provided in the following tables.

Table 70. I²C input timing specifications — SCL and SDA[1]

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1	—	CC	Start condition hold time	2	—	PER_CLK Cycle[2]
2	—	CC	Clock low time	8	—	PER_CLK Cycle
3	—	CC	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	Data hold time	0.0	—	ns

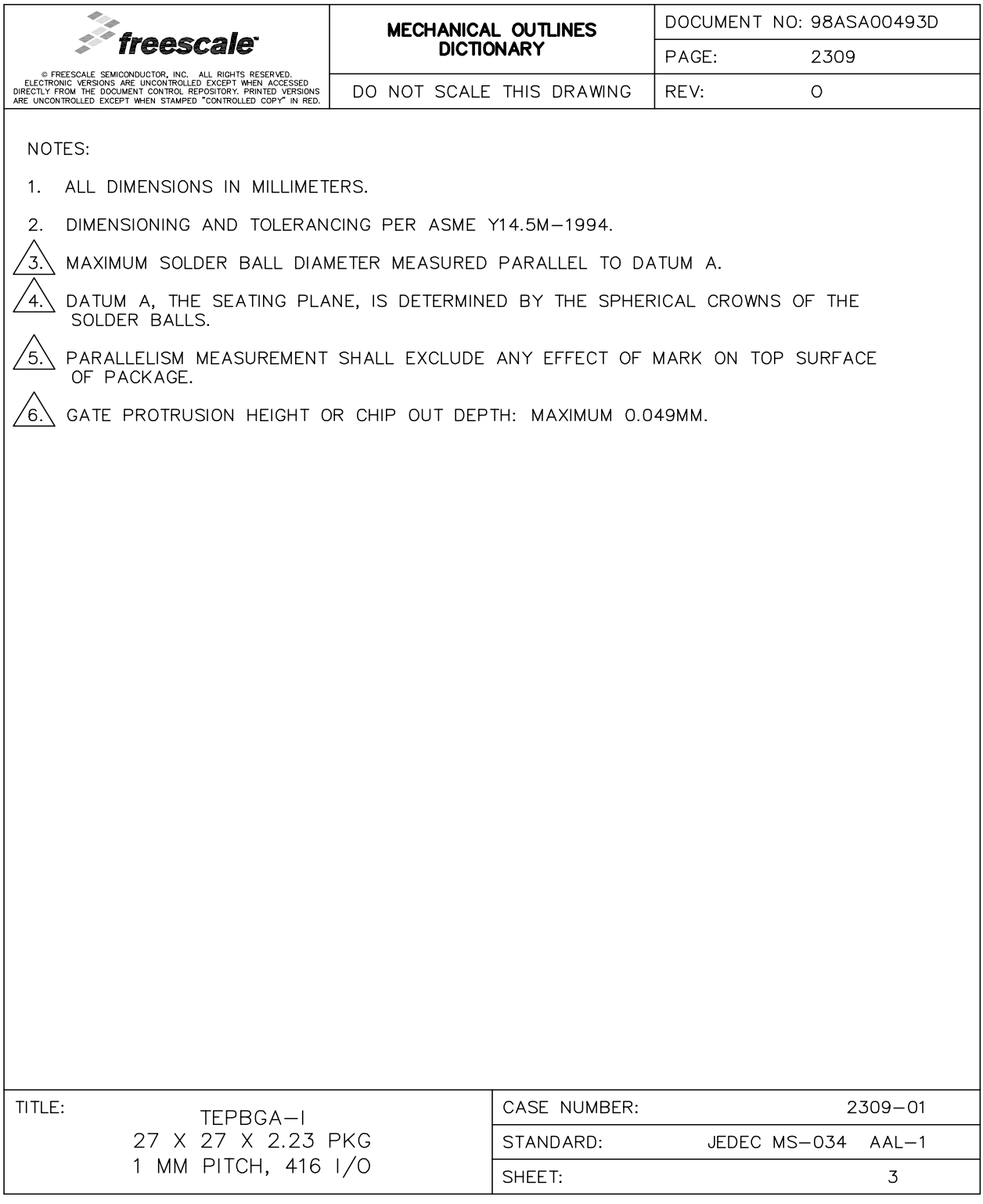


Figure 58. 416 TEPBGA (emulation) package mechanical drawing (Sheet 3 of 3)

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D) \quad \textit{Eqn. 2}$$

where:

T_B = board temperature for the package perimeter (^{o}C)
$R_{\theta JB}$ = junction-to-board thermal resistance (^{o}C/W) per JESD51-8
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (^{o}C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (^{o}C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (^{o}C/W)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—AC specifications—Fast Ethernet Controller (FEC)**
		Section 3.16.3, “FEC timing Table 58 (MII receive signal timing) • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) Table 59 (MII transmit signal timing) • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) • Footnote added to max and min values columns: “Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.” Table 60 (MII async inputs signal timing) • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) Table 61 (MII serial management channel timing): • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) Table 62 (RMII receive signal timing): • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) Table 63 (RMII transmit signal timing,): • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) • Specification change: REF_CLK to TXD[1:0], TX_EN valid max value is 16 ns (was 14) • Added footnote 2 to value column “Output parameters are valid for CL = 25 pF, where CL is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.”
		Electrical characteristics—AC specifications—FlexRay
		Section 3.16.4, FlexRay timing Table 64 (TxEN output characteristics): • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) Table 65 (TxD output characteristics): • $\Sigma t_{TR20\text{-}80}$ specification for $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF, moved from Table 17 (VERY STRONG configuration output buffer electrical characteristics) • $\Sigma t_{TR20\text{-}80}$ specification combined with $dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$ specification. Footnotes added for conditions. 3.3V specification added. • Footnote added: “Specifications valid according to FlexRay EPL 3.0.1 standard with 20%-80% levels and a 10pF load at the end of a 50ohm, 1ns stripline. Please refer to the Very Strong I/O pad specifications.“ • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design)

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—Device voltage monitoring electrical characteristics**
		Table 37 (Voltage monitor electrical characteristics): • V_{PORUP_LV} Rising voltage (power up) condition, changed Min value “1040” to “1111” and Max value “1180” to “1235”. • V_{PORUP_LV} Falling voltage (power down) condition, changed Min value “960” to “1015” and Max value “1100” to “1125”. Added footnote. • V_{LVD096} “960” to “1015” and Max value “1100” to “1145”. • V_{LVD108} changed Min value “1080” to “1125” and Max value “1140” to “1235”. • V_{LVD112} changed Min value “1110” to “1175 and Max value “1180” to “1235”. • V_{HVD140} changed Min value “1320” to “1385” and Max value “1440” to “1475”. • Added new specification V_{HVD145}. • Added “HVD140 does not cause reset” at end of footnote “HVD is released after $t_{VDRELEASE}$ temporization when lower threshold is crossed, HVD is asserted $t_{VDASSERT}$ after detection when upper threshold is crossed.” •]V_{PORUP_HV}, added footnote “the PMC supply also needs to be below 5472 mV (untrimmed HVD600)”. Added new conditions: Rising voltage (power up) on IO JTAG, and Osc supply, Rising voltage (power up) on ADC supply, and Hysteresis on Power-up. • V_{PORUP_HV}: Changed Falling voltage (power down) minimum value to “2850” (was “2680”) and maximum value to 3162 (was “2980”). • Revised Falling voltage footnote to read “Untrimmed LVD300_A will be asserted first on power down” (was “Assume all LVDs except LVD270 on HV supplies disabled”). • V_{LVD295} Rising voltage condition changed Max value “3100” to “3120”. • V_{LVD295} Falling voltage condition changed Min value “2950” to “2920” and Max value “3080” to “3100”. • V_{HVD360} Rising voltage condition changed Min value “3420” to “3435” and Max value “3610” to “3650”. • V_{HVD360} Falling voltage condition changed Min value “3400” to “3415”.
		Electrical characteristics—Flash memory electrical characteristics
		Section 3.15, Flash memory electrical characteristics: • This section completely revised.
		Electrical characteristics—AC specifications—Debug and Calibration
		Table 46 (JTAG pin AC electrical characteristics,): • Added footnote “JTAG timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.” Table 47 (Nexus debug port timing) • Footnote 1 changed to “Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.” • Changed “TDI” to “TDI/TDIC,” “TMS” to “TMS/TMSC,” and “TDO” to “TDO/TDOC.” Figure 27 (Nexus TDI/TDIC, TMS/TMSC, TDO/TDOC timing): • Changed “TDI” to “TDI/TDIC,” “TMS” to “TMS/TMSC,” and “TDO” to “TDO/TDOC.”