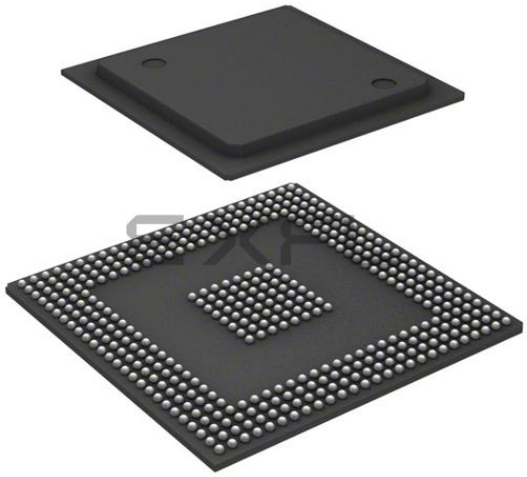

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Program Memory Type	FLASH
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Supplier Device Package	416-PBGA (27x27)
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Table 6. Absolute maximum ratings[1] (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
$V_{DD\_HV\_IO\_EBI}$	SR	External Bus Interface supply voltage	—	–0.3	6.0	V
$V_{DD\_LV\_BD} – V_{DD\_LV}$	SR	Emulation module supply differential to 1.2 V core supply	—	–0.3	1.5	V
V_{IN}	SR	I/O input voltage range[12]	—	–0.3	6.0	V
			Relative to $V_{SS\_HV\_IO}$[13,14]	–0.3	—	
			Relative to $V_{DD\_HV\_IO}$[13,14]	—	0.3	
I_{INJD}	SR	Maximum DC injection current for digital pad	Per pin, applies to all digital pins	–5	5	mA
I_{INJA}	SR	Maximum DC injection current for analog pad	Per pin, applies to all analog pins	–5	5	mA
I_{MAXD}	SR	Maximum output DC current when driven	Medium	–7	8	mA
			Strong	–10	10	
			Very strong	–11	11	
I_{MAXSEG}	SR	Maximum current per power segment[15]	—	–90	90	mA
T_{STG}	SR	Storage temperature range and non-operating times	—	–55	175	°C
STORAGE	SR	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	20	years
T_{SDR}	SR	Maximum solder temperature[16] Pb-free package	—	—	260	°C
MSL	SR	Moisture sensitivity level[17]	—	—	3	—
t_{XRAY}	SR	X-ray screen time[18]	At 160 KeV at max 5 mm	—	3	min

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C, remaining time as defined in note 3 and note 4

3 Allowed 1.38– 1.45 V– for 10 hours cumulative time at maximum T_J = 150 °C, remaining time as defined in note 4

4 1.32 – 1.38 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.326 V at maximum T_J = 150 °C.

5 Allowed 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C, remaining time at or below 5.5 V.

6 $V_{DD\_HV\_IO}$ applies to $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_IO\_FLEXE}$, $V_{DD\_HV\_IO\_JTAG}$, and $V_{DD\_HV\_IO\_EBI}$ I/O power supplies.

7 Allowed 3.6–4.5 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C, remaining time at or below 3.6 V.

8 Includes ADC grounds $V_{SS\_HV\_ADV\_S}$ and $V_{SS\_HV\_ADV\_D}$.

Table 8. Device operating conditions[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Temperature							
T_J	SR	Operating temperature range - junction	—	–40.0	—	150.0	°C
T_A (T_L to T_H)	SR	Ambient operating temperature range	—	–40.0	—	125.0	°C
Voltage							
V_{DD_LV}	SR	External core supply voltage[3,4]	LVD/HVD enabled	1.24	—	1.38[5]	V
			LVD/HVD disabled[6,7,8,9]	1.19	—	1.38[5]	
$V_{DD\_HV\_IO\_MAIN}$[10,11]	SR	I/O supply voltage	LVD400/HVD600 enabled[18]	4.5	—	5.5[12]	V
			LVD400/HVD600 disabled [6,13,14,15,18]	4.2	—	5.5	
			LVD360/HVD600 disabled [6,13,14,16,17,18]	3.0	—	5.5	
$V_{DD\_HV\_IO\_JTAG}$	SR	JTAG I/O supply voltage[6,19]	5 V range	4.5	—	5.5	V
			3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_IO\_FLEX}$	SR	FlexRay I/O supply voltage	5 V range	4.5	—	5.5	V
			3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_IO\_FLEXE}$	SR	FlexRay/EBI I/O supply voltage	5 V range	4.5	—	5.5	V
			3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_IO\_EBI}$	SR	External Bus Interface supply voltage	5 V range	4.5	—	5.5	V
			3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_OSC}$	SR	Oscillator supply voltage[6,20]	5 V range	4.5	—	5.5	V
			3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_PMC}$[21]	SR	Power Management Controller (PMC) supply voltage	Full functionality[22,23]	3.5[24,25]	—	5.5	V
			Reduced internal regulator output capability[26]	3.15	—	3.5	
			Supply monitoring activity only (LVD/HVD)	3.0	—	3.15	
V_{DDSTBY}	SR	RAM standby supply voltage[27,28,29]	—	1.1	—	5.5	V
$V_{DD\_HV\_ADV}$	SR	SARADC, SDADC, Temperature Sensor, and Bandgap Reference supply voltage	LVD400 enabled	4.5	—	5.5	V
			LVD400 disabled[30,31,34]	4.0	—	5.5[32]	
			LVD300 disabled[6,30,31,33,34]	3.7	—	5.5[32]	

[5] Although the maximum V_{DD_LV} operating voltage is 1.38 V, reset is not entered at that voltage. An external voltage monitor is needed or the HVD140_C can be monitored (via an interrupt or by polling the HVD140_C flag bit). Performance above 1.38 V is not guaranteed, and allowed operation above 1.38 V is defined in Absolute maximum ratings.

[6] In the LVD/HVD disabled case, it is necessary for the system to be within a higher voltage range during destructive reset events.

[7] Maximum core voltage is not permitted for entire product life. *See Absolute maximum rating*.

[8] When internal LVD/HVDs are disabled, external monitoring is required to guarantee correct device operation.

[9] Vdd_lv should be above 1.24 V during destructive resets or POR events.

[10] VDD_HV_IO_MAIN range limited to 4.75–5.25 V when FERS = 1 to enable the fast erase time of the flash memory.

[11] During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

[12] When the LVD/HVDs are enabled, the $V_{DD\_HV\_IO\_MAIN}$ must be less than 5.412 V to exit from a destructive reset.

[13] Maximum voltage is not permitted for entire product life. See *Absolute maximum rating*.

[14] When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.

[15] When these LVD/HVDs are disabled, the $V_{DD\_HV\_IO\_MAIN}$ supply must be between 3.182 V and 5.412 V.

[16] Reduced output capabilities below 4.2 V. See performance derating values in *I/O pad electrical characteristics.*

[17] When the LVD/HVDs are disabled, the VDD_HV_IO_MAIN must be between 3.024 V and 5.412 V.

[18] The PMC supply voltage ($V_{DD\_HV\_PMC}$) must be within the correct range (see the $V_{DD\_HV\_PMC}$ specification).

[19] When the LVD/HVDs are disabled, the HV I/O JTAG supply ($V_{DD\_HV\_IO\_JTAG}$) must be above 3.024 V.

[20] When the LVD/HVDs are disabled, the HV OSC supply ($V_{DD\_HV\_OSC}$) must be above 3.024 V.

[21] Flash read operation is supported for a minimum $V_{DD\_HV\_PMC}$ value of 3.15 V. Flash read, program, and erase operations are supported for a minimum $V_{DD\_HV\_PMC}$ value of 3.5 V.

[22] When the LVD/HVDs are disabled, the $V_{DD\_HV\_PMC}$ must be below 5.412 V during destructive reset events.

[23] A minimum of 4.5 V is required to guarantee correct user logic BIST operation.

[24] During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

[25] Above Ta = 25°C, the minimum $V_{DD\_HV\_PMC}$ voltage is 3.6 V.

[26] With the reduced internal regulator output capability, erases and writes to the device flash cannot be guaranteed for a single event and multiple erases and writes may be necessary. User logic BIST is not supported with reduced capability.

[27] RAM data retention is guaranteed at a voltage that is always below the maximum brownout flag trip point voltage (see the DC Electrical Specification table). The minimum V_{DDSTBY} voltage at the pin is larger in order to account for on-chip IR drop and noise. There is no effect on RAM operation when V_{DDSTBY} is below 1.1 V, and V_{DD_LV} is above the minimum operating value.

[28] Non-regulated supplies can be used on the VDDSTBY pin if the absolute maximum and operating condition voltage limits are met. There is no static clamp to a supply rail for the VDDSTBY pin, only dynamic protection for ESD events.

[29] The VDDSTBY pin should be connected to ground in the application when the standby RAM feature is not used.

[30] $V_{DD\_HV\_ADV\_S}$ is required to be between 4.5 V and 5.5 V to read the internal Temperature Sensor and Bandgap Reference.

[31] SAR ADC only. SDADC minimum is 4.5 V.

[32] The ADC is functional up to 5.9V with no reliability issues, but performance is not guaranteed.

[33] When the LVD/HVDs are disabled, the HV ADC supply ($V_{DD\_HV\_ADV}$) must be above 3.182 V.

[34] For supply voltages between 3.0 V and 4.0 V there is no guaranteed precision of ADC (accuracy/linearity). ADCs recover to a fully functional state when the voltage rises above 4.0 V.

[35] $V_{DD\_HV\_ADR\_S}$ must be between 4.5 V and 5.5 V for accurate reading of the device Temperature Sensor.

[36] Full device lifetime without performance degradation

[37] I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the *Absolute maximum ratings* table for maximum input current for reliability requirements.

Table 17. VERY STRONG configuration output buffer electrical characteristics[1]

Symbol		Parameter	Conditions[2,3]	Value			Unit
				Min	Typ	Max	
R_{OH_V}	CC	PMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1 I_{OH} = 8 mA	20	40	72	Ω
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OH} = 7 mA[4]	30	50	90	
R_{OL_V}	CC	NMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1 I_{OL} = 8 mA	20	40	72	Ω
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OL} = 7 mA[4]	30	50	90	
f_{MAX_V}	CC	Output frequency VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	—	—	50	MHz
			VSIO[VSIO_xx] = 1, C_L = 15 pF[4,5]	—	—	50	
$t_{TPD50\text{-}50}$[6]	CC	50-50 % Output pad propagation delay time	$V_{DD\_HV\_IO}$ = 5 V +/- 10 %, C_L = 25 pF	—	—	5.5	ns
			$V_{DD\_HV\_IO}$ = 5.0 V +/- 10 %, C_L = 50 pF	—	—	6.5	ns
			$V_{DD\_HV\_IO}$ = 3.3 V +/- 10 %, C_L = 15 pF	—	—	7.3/7.6	ns
t_{TR_V}	CC	10–90% threshold transition time output pin VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	1	—	5.3	ns
			$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 50 pF[5]	3	—	12	
			$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 200 pF[5]	14	—	45	
$t_{TR20\text{-}80}$	CC	20–80% threshold transition time[7] output pin VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	0.8	—	4	ns
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 15 pF[5]	1	—	5	
t_{TRTTL}	CC	TTL threshold transition time[8] for output pin in VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 25 pF[5]	1	—	5	ns
$\Sigma t_{TR20\text{-}80}$	CC	Sum of transition time 20–80% output pin VERY STRONG configuration[9]	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF	—	—	9	ns
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 15 pF[5]	—	—	9	
$\lvert t_{SKEW\_V} \rvert$	CC	Difference between rise and fall time at 20–80%	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	0	—	1	ns

Table 19. I/O consumption[1]

Symbol		Parameter	Conditions[2]	Value			Unit
				Min	Typ	Max	
I_{RMS_W}	CC	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	mA
			C_L = 50 pF, 1 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	
			C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
			C_L = 50 pF, 1 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
I_{RMS_M}	CC	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz V_{DD} = 5.0 V ± 10%	—	—	4.7	mA
			C_L = 50 pF, 6 MHz V_{DD} = 5.0 V ± 10%	—	—	4.8	
			C_L = 25 pF, 12 MHz V_{DD} = 3.3 V ± 10%	—	—	2.6	
			C_L = 50 pF, 6 MHz V_{DD} = 3.3 V ± 10%	—	—	2.7	
I_{RMS_S}	CC	RMS I/O current for STRONG configuration	C_L = 25 pF, 50 MHz V_{DD} = 5.0 V ± 10%	—	—	19	mA
			C_L = 50 pF, 25 MHz V_{DD} = 5.0 V ± 10%	—	—	19	
			C_L = 25 pF, 50 MHz V_{DD} = 3.3 V ± 10%	—	—	10	
			C_L = 50 pF, 25 MHz V_{DD} = 3.3 V ± 10%	—	—	10	
I_{RMS_V}	CC	RMS I/O current for VERY STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0V +/- 10%	—	—	22	mA
			C_L = 50 pF, 25 MHz, V_{DD} = 5.0V ± 10%	—	—	22	
			C_L = 25 pF, 50 MHz, V_{DD} = 3.3V ± 10%	—	—	11	
			C_L = 25 pF, 25 MHz, V_{DD} = 3.3V ± 10%	—	—	11	
I_{RMS_EBI}	CC	RMS I/O current for External Bus output pins	C_{DRV} = 6 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	9	mA
			C_{DRV} = 12 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	15	
			C_{DRV} = 18 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	27	
			C_{DRV} = 30 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	42	

[2] During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characterstics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

[3] Stated maximum values represent peak consumption that lasts only a few ns during I/O transition. When possible (timed output) it is recommended to delay transition between pads by few cycles to reduce noise and consumption.

[4] For $I_{DYN\_EBI\_GPIO}$ dynamic current for EBI GPIO mode use the I_{DYN_M} values.

3.8 Reset pad ($\overline{\text{PORST}}$, $\overline{\text{ESR0}}$) electrical characteristics

The device implements a dedicated bidirectional reset pin ($\overline{\text{PORST}}$).

NOTE

$\overline{\text{PORST}}$ pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 kΩ.

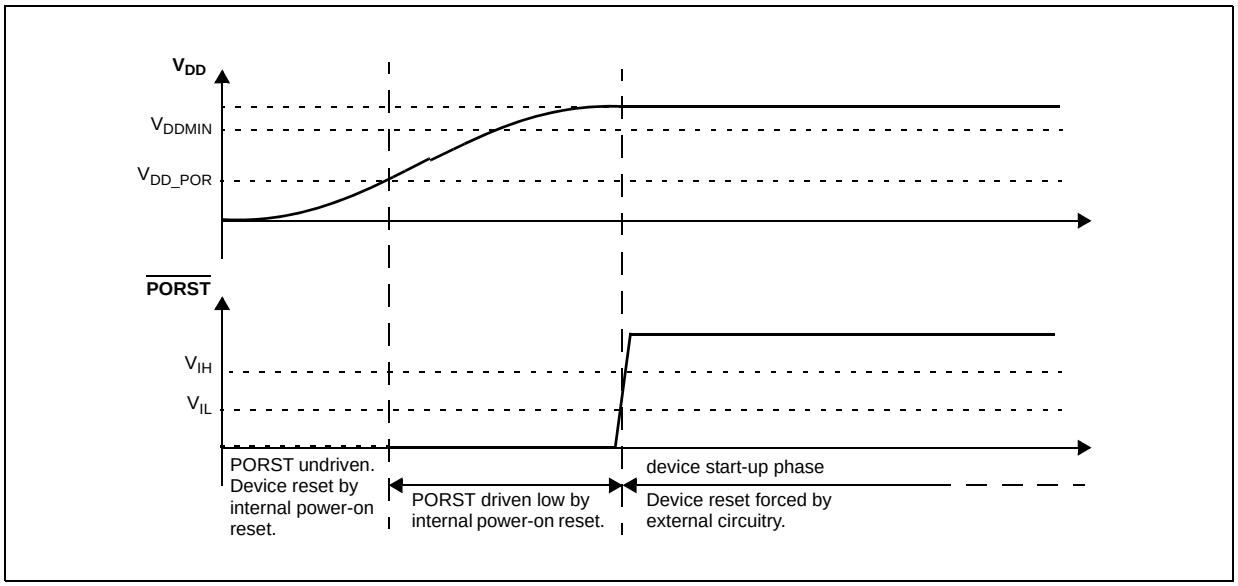


Figure 10. Start-up reset requirements

Figure 11 describes device behavior depending on supply signal on $\overline{\text{PORST}}$:

1. $\overline{\text{PORST}}$ low pulse amplitude is too low—it is filtered by input buffer hysteresis. Device remains in current state.
2. $\overline{\text{PORST}}$ low pulse duration is too short—it is filtered by a low pass filter. Device remains in current state.
3. $\overline{\text{PORST}}$ low pulse generates a reset:
   a) $\overline{\text{PORST}}$ low but initially filtered during at least W_{FRST}. Device remains initially in current state.
   b) $\overline{\text{PORST}}$ potentially filtered until W_{NFRST}. Device state is unknown: it may either be reset or remains in current state depending on other factors (temperature, voltage, device).
   c) $\overline{\text{PORST}}$ asserted for longer than W_{NFRST}. Device is under reset.

Table 23. External Oscillator electrical specifications[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
f_{XTAL}	CC	Crystal Frequency Range[2]	—	4	8	MHz
			—	>8	20	
			—	>20	40	
t_{cst}	CC	Crystal start-up time [3,4]	T_J = 150 °C	—	5	ms
t_{rec}	CC	Crystal recovery time[5]	—	—	0.5	ms
V_{IHEXT}	CC	EXTAL input high voltage[6,7] (External Clock Input)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$	V_{REF} + 0.6	—	V
V_{ILEXT}	CC	EXTAL input low voltage[6,7] (External Clock Input)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$	—	V_{REF} - 0.6	V
C_{S_xtal}	CC	Total on-chip stray capacitance on XTAL/EXTAL pins[8]	BGA416, BGA512	8	8.6	pF
V_{EXTAL}	CC	Oscillation Amplitude on the EXTAL pin after startup[9]	T_J = –40 °C to 150 °C	0.5	1.6	V
V_{HYS}	CC	Comparator Hysteresis	T_J = –40 °C to 150 °C	0.1	1.0	V
I_{XTAL}	CC	XTAL current[13,10]	T_J = –40 °C to 150 °C	—	14	mA

1 All oscillator specifications are valid for VDD_HV_IO_JTAG = 3.0 V – 5.5 V.

2 The range is selectable by UTEST miscellaneous DCF clients XOSC_LF_EN and XOSC_EN_40MHZ.

3 This value is determined by the crystal manufacturer and board design.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.

6 This parameter is guaranteed by design rather than 100% tested.

7 Applies to an external clock input and not to crystal mode.

8 See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.

9 Amplitude on the EXTAL pin after startup is determined by the ALC block, i.e., the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.

10 I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2–3 mA range and is dependent on the load and series resistance of the crystal. Test circuit is shown in Figure 13.

Table 26. ADC pin specification[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
I_{LK_INUD}	CC	Input leakage current, two ADC channels input with weak pull-up and weak pull-down	T_J < 40 °C	—	50	nA
			T_J < 150 °C	—	150	
I_{LK_INUSD}	CC	Input leakage current, two ADC channels input with weak pull-up and strong pull-down	T_J < 40 °C	—	80	nA
			T_J < 150 °C	—	250	
I_{LK_INREF}	CC	Input leakage current, two ADC channels input with weak pull-up and weak pull-down and alternate reference	T_J < 40 °C	—	160	nA
			T_J < 150 °C	—	400	
I_{LK_INOUT}	CC	Input leakage current, two ADC channels input, GPIO output buffer with weak pull-up and weak pull-down	T_J < 40 °C	—	140	nA
			T_J < 150 °C	—	380	
I_{INJ}	CC	Injection current on analog input preserving functionality	Applies to any analog pins	–3	3	mA
C_{HV_ADC}	SR	$V_{DD\_HV\_ADV}$ external capacitance[2]		1	2.2	µF
C_{P1}	CC	Pad capacitance	—	0	10	pF
C_{P2}	CC	Internal routing capacitance	SARn channels	0	0.5	pF
			SARB channels	0	1	
C_{P3}	CC	Internal routing capacitance	Only for SARB channels	0	1	pF
C_S	CC	SAR ADC sampling capacitance	—	6	8.5	pF
R_{SWn}	CC	Analog switches resistance	SARn channels	0	1.1	kΩ
			SARB channels	0	1.7	
R_{AD}	CC	ADC input analog switches resistance	—	0	0.6	kΩ
R_{CMSW}	CC	Common mode switch resistance	—	0	2.6	kΩ
R_{CMRL}	CC	Common mode resistive ladder	—	0	3.5	kΩ
R_{SAFEPD}[3]	CC	Discharge resistance for AN7/AN35 channels (strong pull-down for safety)	—	0	300	Ω

1 All specifications in this table valid for the full input voltage range for the analog inputs.

2 For noise filtering, add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_ADV}$ and $V_{SS\_HV\_ADV}$.

3 Safety pull-down is available for port pin PB[5] and PE[14].

3.10.2 SAR ADC electrical specification

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

[6] This parameter is guaranteed by bench validation with a small sample of typical devices, and tested in production to ± 6 LSB.

3.10.3 S/D ADC electrical specification

The SDn ADCs are Sigma Delta 16-bit analog-to-digital converters with 333 Ksps maximum output rate.

Table 28. SDn ADC electrical specification[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
V_{IN}	SR	ADC input signal	—	0	—	$V_{DD\_HV\_ADV\_D}$	V
V_{IN_PK2PK}[2]	SR	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$[3] – V_{INM}[4]	Single ended $V_{INM} = V_{SS\_HV\_ADR\_D}$	$V_{DD\_HV\_ADR\_D}$/GAIN			V
			Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR\_D}$ GAIN = 1	±0.5*$V_{DD\_HV\_ADR\_D}$			
			Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR\_D}$ GAIN = 2,4,8,16	±$V_{DD\_HV\_ADR\_D}$/GAIN			
			Differential, $0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	±$V_{DD\_HV\_ADR\_D}$/GAIN			
f_{ADCD_M}	SR	S/D modulator Input Clock	—	4	14.4	16	MHz
f_{ADCD_S}	SR	Output conversion rate	—	—	—	333	ksps
—	CC	Oversampling ratio	Internal modulator	24	—	256	—
			External modulator	—	—	256	—
RESOLUTION	CC	S/D register resolution[5]	2’s complement notation	16			bit
GAIN	SR	ADC gain	Defined via ADC_SD[PGA] register. Only integer powers of 2 are valid gain values.	1	—	16	—
$\|\delta_{GAIN}\|$	CC	Absolute value of the ADC gain error[6,7]	Before calibration (applies to gain setting = 1)	—	—	1.5	%
			After calibration, $\Delta V_{DD\_HV\_ADR\_D}$ < 5% $\Delta V_{DD\_HV\_ADV\_D}$ < 10% ΔT_J < 50 °C	—	—	5	mV
			After calibration, $\Delta V_{DD\_HV\_ADR\_D}$ < 5% $\Delta V_{DD\_HV\_ADV\_D}$ < 10% ΔT_J < 100 °C	—	—	7.5	
			After calibration, $\Delta V_{DD\_HV\_ADR\_D}$ < 5% $\Delta V_{DD\_HV\_ADV\_D}$ < 10% ΔT_J < 150 °C	—	—	10	

3.12.1 LFAST interface timing diagrams

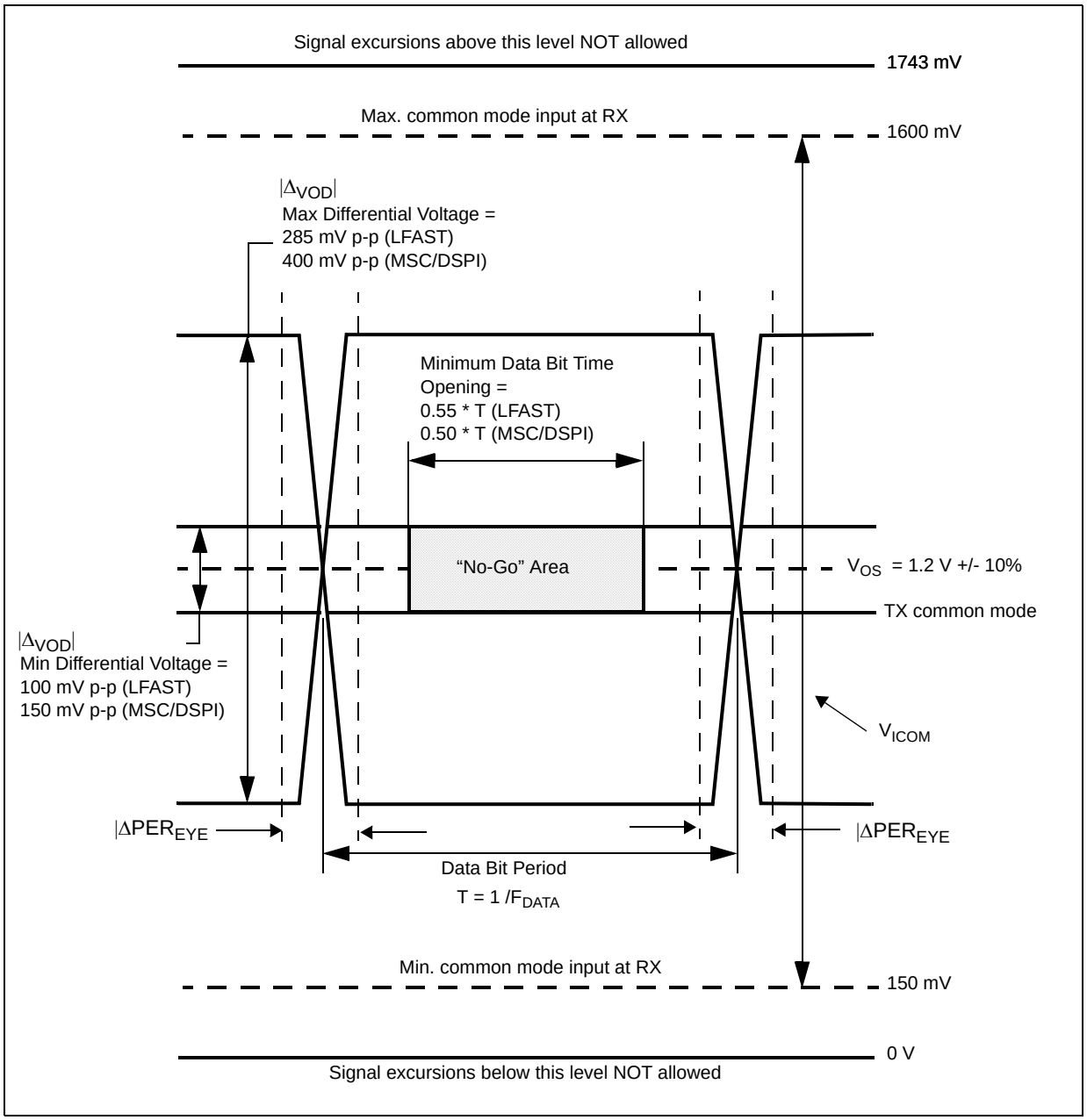


Figure 16. LFAST and MSC/DSPI LVDS timing definition

[12] The LXRXOP[0] bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing.

[13] Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions.

Table 31. LFAST transmitter electrical characteristics[1,2]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{DATA}	SR	Data rate	—	—	—	312/320[3]	Mbps
V_{OS}	CC	Common mode voltage	—	1.08	—	1.32	V
$\lvert V_{OD} \rvert$	CC	Differential output voltage swing (terminated)[4,5]	—	110	171	285	mV
t_{TR}	CC	Rise/Fall time (absolute value of the differential output voltage swing)[4,5]	—	0.26	—	1.5	ns
C_L	SR	External lumped differential load capacitance[3]	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	10.0	pF
			$V_{DD\_HV\_IO}$ = 3.0 V	—	—	8.5	
I_{LVDS_TX}	CC	Transmitter DC current consumption	Enabled	—	—	3.2	mA

[1] The LFAST and High-Speed Debug LFAST pad electrical characteristics are based on worst case internal capacitance values shown in Figure 19.

[2] All LFAST and High-Speed Debug LVDS pad electrical characteristics are valid from –40 °C to 150 °C.

[3] The 312 Mbps data rate is achieved with a 26 MHz reference clock, and 320 Mbps is achieved with a 10 or 20 MHz reference clock.

[4] Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 19.

[5] Valid for maximum external load C_L.

Table 32. MSC/DSPI LVDS transmitter electrical characteristics [1,2]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Data Rate							
f_{DATA}	SR	Data rate	—	—	—	80	Mbps
V_{OS}	CC	Common mode voltage	—	1.08	—	1.32	V
$\lvert V_{OD} \rvert$	CC	Differential output voltage swing (terminated)[3,4]	—	150	214	400	mV
t_{TR}	CC	Rise/Fall time (absolute value of the differential output voltage swing)[3,4]	—	0.8	—	4.0	ns
C_L	SR	External lumped differential load capacitance[3]	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	50	pF
			$V_{DD\_HV\_IO}$ = 3.0 V	—	—	39	
I_{LVDS_TX}	CC	Transmitter DC current consumption	Enabled	—	—	4.0	mA

[1] The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst case internal capacitance values given in Figure 19.

[2] All MSC and DSPI LVDS pad electrical characteristics are valid from –40 °C to 150 °C.

Table 40 shows the estimated Program/Erase times.

Table 40. Flash memory program and erase specifications (pending characterization)

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3,4]		Field Update			Units
			Initial Max	Initial Max Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C≤ T_a ≤ 30°C	-40°C≤ T_J ≤ 150°C	-40°C≤ T_J ≤ 150 °C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgn}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgn}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1.200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1 Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.

2 Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.

3 Conditions: ≤ 150 cycles, nominal voltage.

4 Plant Programming times provide guidance for timeout limits used in the factory.

5 Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.

6 Conditions: -40°C≤ T_J ≤ 150°C; full spec voltage.

3.15.3 Flash memory Array Integrity and Margin Read specifications

Table 42. Flash memory Array Integrity and Margin Read specifications (characterized but not tested)

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16KB block.	—	—	512 × Tperiod × Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32KB block.	—	—	1024 × Tperiod × Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64KB block.	—	—	2048 × Tperiod × Nread	—
$t_{ai256kseq}$	Array Integrity time for sequential sequence on 256KB block.	—	—	8192 × Tperiod × Nread	—
$t_{aifullseq}$	Array Integrity time for sequential sequence full array.	—	—	3.77e5 × Tperiod × Nread	—
$t_{aifullprop}$	Array Integrity time for proprietary sequence (applies to full array or single block).	—	—	9.96e6 × Tperiod × Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256KB block.	893.01	—	1,339.5	µs
t_{mrfull}	Margin Read time for sequential sequence full array.	45.21	—	60.26	ms

1 Array Integrity times need to be calculated and are dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)

2 The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

2 Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

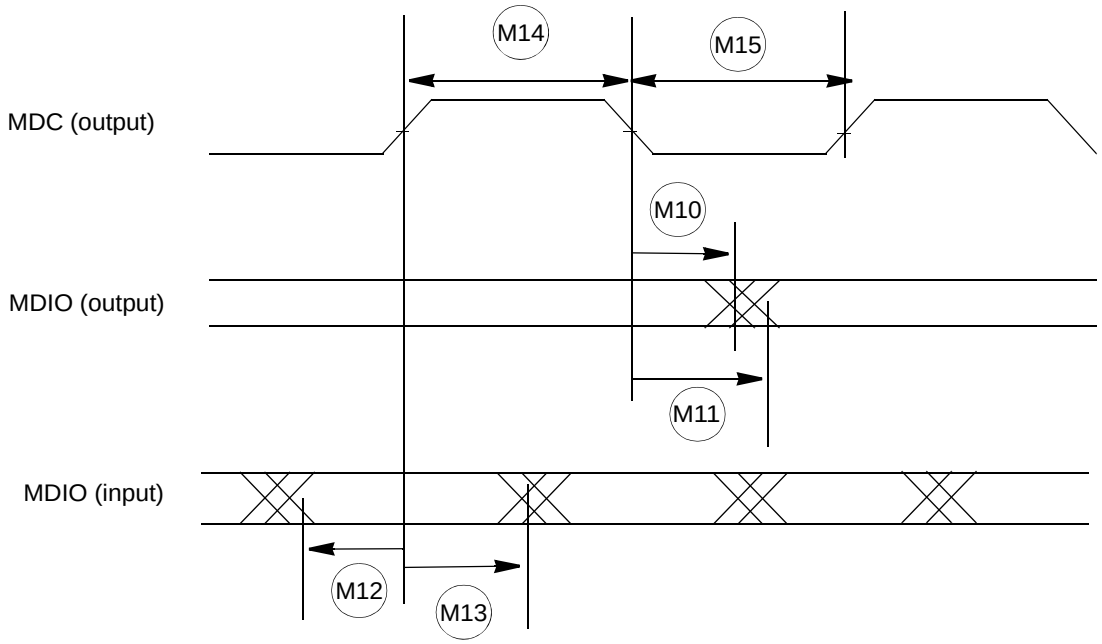


Figure 43. MII serial management channel timing diagram

3.16.3.5 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Table 62. RMII receive signal timing[1]

Symbol		Characteristic	Value		Unit
			Min	Max	
R1	CC	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	CC	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	CC	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	CC	REF_CLK pulse width low	35%	65%	REF_CLK period

1 All timing specifications are referenced from REF_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

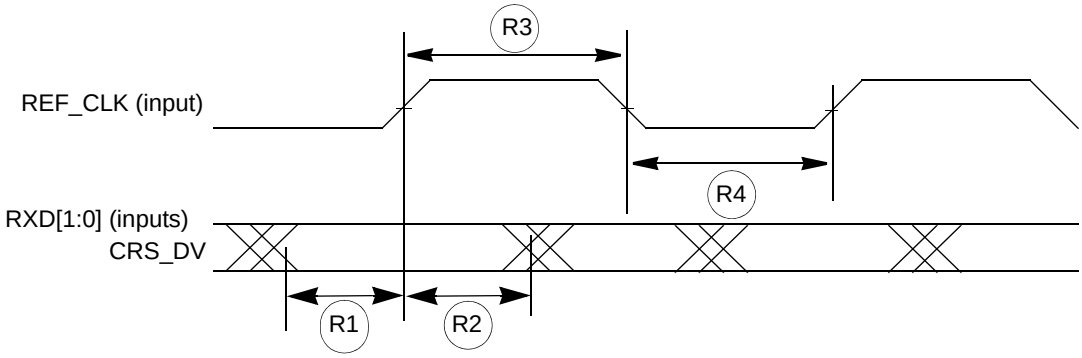


Figure 44. RMII receive signal timing diagram

3.16.3.6 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. These options allows the use of non-compliant RMII PHYs.

Table 63. RMII transmit signal timing[1, 2]

Symbol		Characteristic	Value[3]		Unit
			Min	Max	
R5	CC	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	CC	REF_CLK to TXD[1:0], TX_EN valid	—	16	ns
R7	CC	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	CC	REF_CLK pulse width low	35%	65%	REF_CLK period

1 RMII timing is valid only up to a maximum of 150 ^{o}C junction temperature.

2 All timing specifications are referenced for TTL or CMOS input levels for REF_CLK to the valid output levels, 0.8 V and 2.0 V.

3 Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

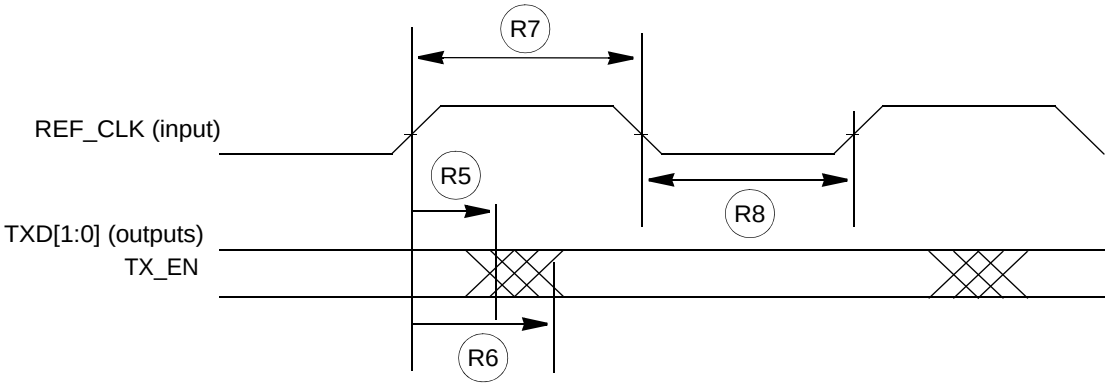


Figure 45. RMII transmit signal timing diagram

Table 65. TxD output characteristics[1,2]

Symbol		Characteristic	Value		Unit
			Min	Max	
dCCTxAsym	CC	Asymmetry of sending CC at 25 pF load (= $dCCTxD_{50\%}$ − 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	CC	Sum of Rise and Fall time of TxD signal at the output pin[3,4]	—	9[5]	ns
			—	9[6]	
$dCCTxD_{01}$	CC	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	CC	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1 TxD pin load maximum 25 pF

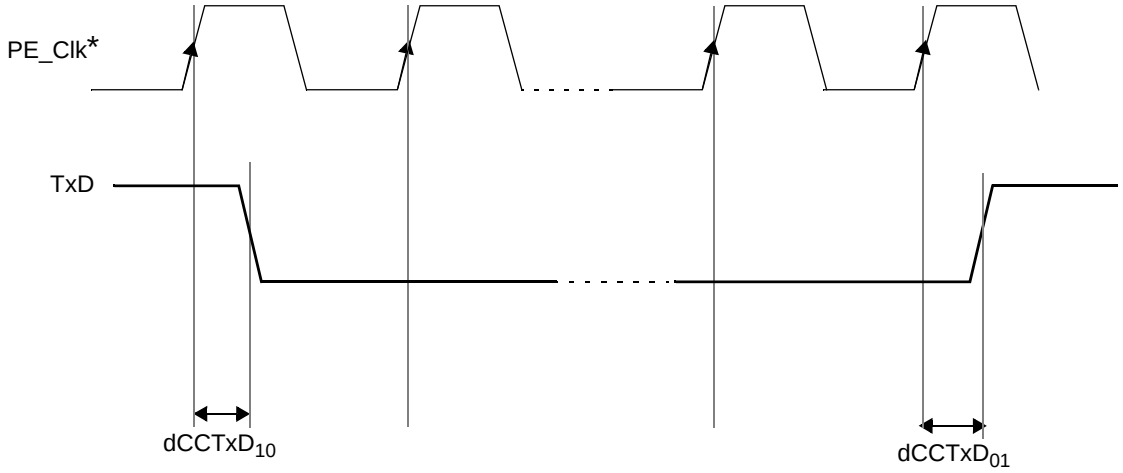
2 Specifications valid according to FlexRay EPL 3.0.1 standard with 20%–80% levels and a 10pF load at the end of a 50 Ohm, 1 ns stripline. Please refer to the Very Strong I/O pad specifications.

3 Pad configured as VERY STRONG

4 Sum of transition time simulation is performed according to Electrical Physical Layer Specification 3.0.1 and the entire temperature range of the device has been taken into account.

5 $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF

6 $V_{DD\_HV\_IO}$ = 3.3 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 0.6 ns, C_L = 10 pF



* FlexRay Protocol Engine Clock

Figure 49. TxD Signal propagation delays

Table 70. I²C input timing specifications — SCL and SDA[1] (continued)

No.	Symbol		Parameter	Value		Unit
				Min	Max	
5	—	CC	Clock high time	4	—	PER_CLK Cycle
6	—	CC	Data setup time	0.0	—	ns
7	—	CC	Start condition setup time (for repeated start condition only)	2	—	PER_CLK Cycle
8	—	CC	Stop condition setup time	2	—	PER_CLK Cycle

1 I^2C input timing is valid for Automotive and TTL inputs levels, hysteresis enabled, and an input edge rate no slower than 1 ns (10% – 90%).

2 PER_CLK is the SoC peripheral clock, which drives the I^2C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Table 71. I²C output timing specifications — SCL and SDA[1,2,3,4]

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1	—	CC	Start condition hold time	6	—	PER_CLK Cycle[5]
2	—	CC	Clock low time	10	—	PER_CLK Cycle
3	—	CC	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	Data hold time	7	—	PER_CLK Cycle
5	—	CC	Clock high time	10	—	PER_CLK Cycle
6	—	CC	Data setup time	2	—	PER_CLK Cycle
7	—	CC	Start condition setup time (for repeated start condition only)	20	—	PER_CLK Cycle
8	—	CC	Stop condition setup time	10	—	PER_CLK Cycle

1 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

2 Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

3 Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.

4 Programming the IBFD register (I^2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I^2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the IBC field of the IBFD register.

5 PER_CLK is the SoC peripheral clock, which drives the I^2C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—Flash memory electrical characteristics**
		Section 3.15, Flash memory electrical characteristics • This section completely revised.
		Electrical characteristics—AC specifications—Debug and Calibration
		Table 46 (JTAG pin AC electrical characteristics,): • Specification change: t_{JCYC} (TCK cycle time) now consists of a single specification—minimum value is 100 ns. Footnotes from previous entries have been removed. • Specification change: t_{TDOHZ} (TCK low to TDO high impedance) is now 15 ns (was 16) • Classification change: All specifications are “D” (were “P” and “C”) Table 47 (Nexus debug port timing) • New specification: t_{EVTIPW} (EVTI pulse width) • New specification: t_{EVTOPW} (EVTO pulse width) • Clarification: footnote added to T_{CYC}, defining it as the system clock period • Specification change: TDO propagation delay from falling edge of TCK max is 16 ns (was 12.5 ns) • Specification change: TCK cycle time is min value is 2 t_{CYC} (was 4) • Specification change: Absolute minimum TCK cycle time min value is 40 ns (was 25) • Specification change: TDI Data Hold Time min value is 5 ns (was 17.5) • Specification change: TMS Data Hold Time min value is 5 ns (was 17.5) • TDO propagation delay from falling edge of TCK max value is 16 ns (was 12.5) • Specification change: t_{TCYC} (absolute minimum TCK cycle time) now consists of two specifications—one with TDO sampled on posedge of TCK and one sampled with TDO sampled on negedge of TCK. Table 48 (Aurora LVDS interface timing specifications) • Specification change: Data rate typ. value is undefined (was 1200 Mbps) • Specification change: Data rate max. value is 1250 Mbps (was “Typ+1%”) Table 49 (Aurora debug port timing) • Specification change: t_{REFCLK} (Reference clock frequency) max value is 1250 MHz (was 1200) • Specification change: OUI (Aurora lane unit interval) is now specified by data rate • Characteristic vs. Requirement change: J_D (Transmit lane deterministic jitter) is “SR” (was “CC”) • Characteristic vs. Requirement change: J_T (Transmit lane total jitter) is “SR” (was “CC”)
		Electrical characteristics—AC specifications—DSPI
		Section 3.19.2, DSPI timing with CMOS and LVDS pads: Substantive changes to entire section, including reclassification of content as: • Table 51 (DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1) • Table 52 (DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1) • Table 54 (DSPI LVDS slave timing – full duplex – modified transfer format (MTFE = 0/1)) • Table 55 (DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock,) • Table 56 (DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock)

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—AC specifications—FlexRay (con't)**
		Table 66 (RxD input characteristics): • New specification: dCCRxAsymAccept15 (Acceptance of asymmetry at receiving CC with 15 pF load) • New specification: dCCRxAsymAccept25 (Acceptance of asymmetry at receiving CC with 25 pF load) • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design)
		Electrical characteristics—AC specifications—PSI5
		Section 3.19.6, PSI5 timing Table 67 (PSI5 timing): • Specification description for t_{MSG_DLY} changed to, "Delay from last bit of frame (CRC0) to assertion of new message received interrupt" (was, "Delay from last bit of frame (end of idle time) ...") • Specification description for t_{MSG_JIT} changed to, "Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt" (was, "Delay from last bit of frame (end of idle time) ...") • Maximum value for t_{SYNC_JIT} changed to ±(1 PSI5_1µs_CLK + 1 PBRIDGEn_CLK); was 1 cycle • Footnote 2 ("Measured in PSI5 1 MHz clock cycles (PSI5_1us_CLK on the device).") on the unit for t_{SYNC_JIT} deleted • Classification change: t_{MSG_DLY} (Delay from last bit of frame (CRC0) to assertion of new message received interrupt) is "D" (was "C") • Classification change: t_{SYNC_DLY} (Delay from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin) is "D" (was "C") • Classification change: t_{MSG_JIT} (Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt) is "D" (was "C") • Classification change: t_{SYNC_JIT} (Delay jitter from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin) is "D" (was "C")
		Electrical characteristics—AC specifications—UART
		Section 3.18.7, UART timing • New
		Electrical characteristics—AC specifications—EBI
		Section 3.16.7, External Bus Interface (EBI) Timing: • New
		Package characteristics
		• 292 MAPBGA case drawing Rev. A included. • 416 TEPBGA case drawing Rev. 0 included.
		Electrical characteristics—Thermal Characteristics
		Table 74 (Thermal characteristics) • This table consolidates what were formerly separate thermal specifications tables for each package. All values have been updated.

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—ADC specifications (con't)**
		Table 28 (SDn ADC electrical specification): • Removed the I_{LK_IN} specification from table. • For $SNR_{DIFF150}$, $SNR_{DIFF333}$, and SNR_{SE150} specifications, added reference to "S/D ADC is functional in the range 3.0 V < VDD_HV_ADR_D , 4.0 V. . ." footnote. • Moved $V_{REF\_BG\_T}$, $V_{REF\_BG\_TC}$ and $V_{REF\_BG\_LR}$ specifications from ADC pin specification table to Device operating table. • Removed I_{BG} specification as it is already provided in the DC electrical table. • Maximum value of parameter "GAIN" changed from "16" to "15"
		Table 28 (SDn ADC electrical specification): • Changed footnote from "The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.87 dB." to "The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB." • Max value of δ_{GROUP} modified for all values of OSR. • $t_{LATENCY}$, $t_{SETTLING}$ and $t_{ODRECOVERY}$: "HPF = ON" and "HPF = OFF" conditions added. New max values. • Added SINAD and THD specifications. • RESOLUTION specification, added footnote "When using a GAIN setting of 16, the conversion result will always have a value of zero in the least significant bit. The gives an effective resolution of 15 bits." • $\lvert\delta_{GAIN}\rvert$ specification, changed Max value from "1" % to "1.5" %, "0.1" % to "5" mV, "0.25" % to "7.5" mV, and "0.5 %" to 10" mV". • V_{OFFSET} specification, added 3 "After calibration" conditions, $\Delta_{VDD\_HV\_ADR\_D}$ < 5% $\Delta_{VDD\_HV\_ADV\_D}$ < 10% ΔT_J < 50 °C, Max value of "5" mV, $\Delta_{VDD\_HV\_ADR\_D}$ < 5% $\Delta_{VDD\_HV\_ADV\_D}$ < 10% ΔT_J < 100 °C, Max value of "7.5" mV and "After calibration" conditions, $\Delta_{VDD\_HV\_ADR\_D}$ < 5% $\Delta_{VDD\_HV\_ADV\_D}$ < 10% ΔT_J < 150 °C, Max value of "10" mV. • Changed all SNR specification "Unit"s from "dB" to "dBFS". • Changed SFDR specification "Unit" from "dB" to "dBc". • Z_{IN} specification, changed footnote to "Input impedance is valid over the full input frequency range.Input impedance is calculated in megaohms by the formula 25.6/(Gain * f_{ADCD_M}). • Common mode rejection ratio parameter changed symbol from "—" to "V_{cmrr}". • Anti-aliasing filter parameter, changed symbol "—" to "R_{Caaf}". • Stop band attenuation parameter, changed symbol "—" to "$F_{rolloff}$". • Changed footnote in 13 "full input range (specified by Vin)" to "full input frequency range." • Changed in footnote 15 "0.873" dB to "0.087" dB. • f_{ADCD_M}, changed "S/D clock 3(4)" to "S/D Modulator Input Clock" and replaced "—" with "4" in Min column. • f_{ADCD_S} changed "conversion rate'" to "output conversion rate".