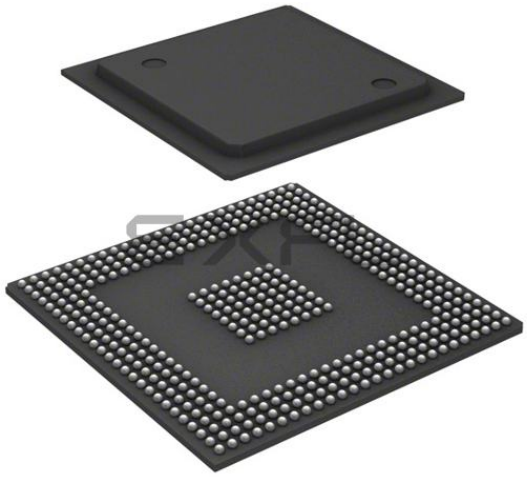

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Details	
Product Status	Active
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Core Size	32-Bit Tri-Core
Speed	300MHz
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Program Memory Size	8.64MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	404K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
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Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5777mk0mvu8r

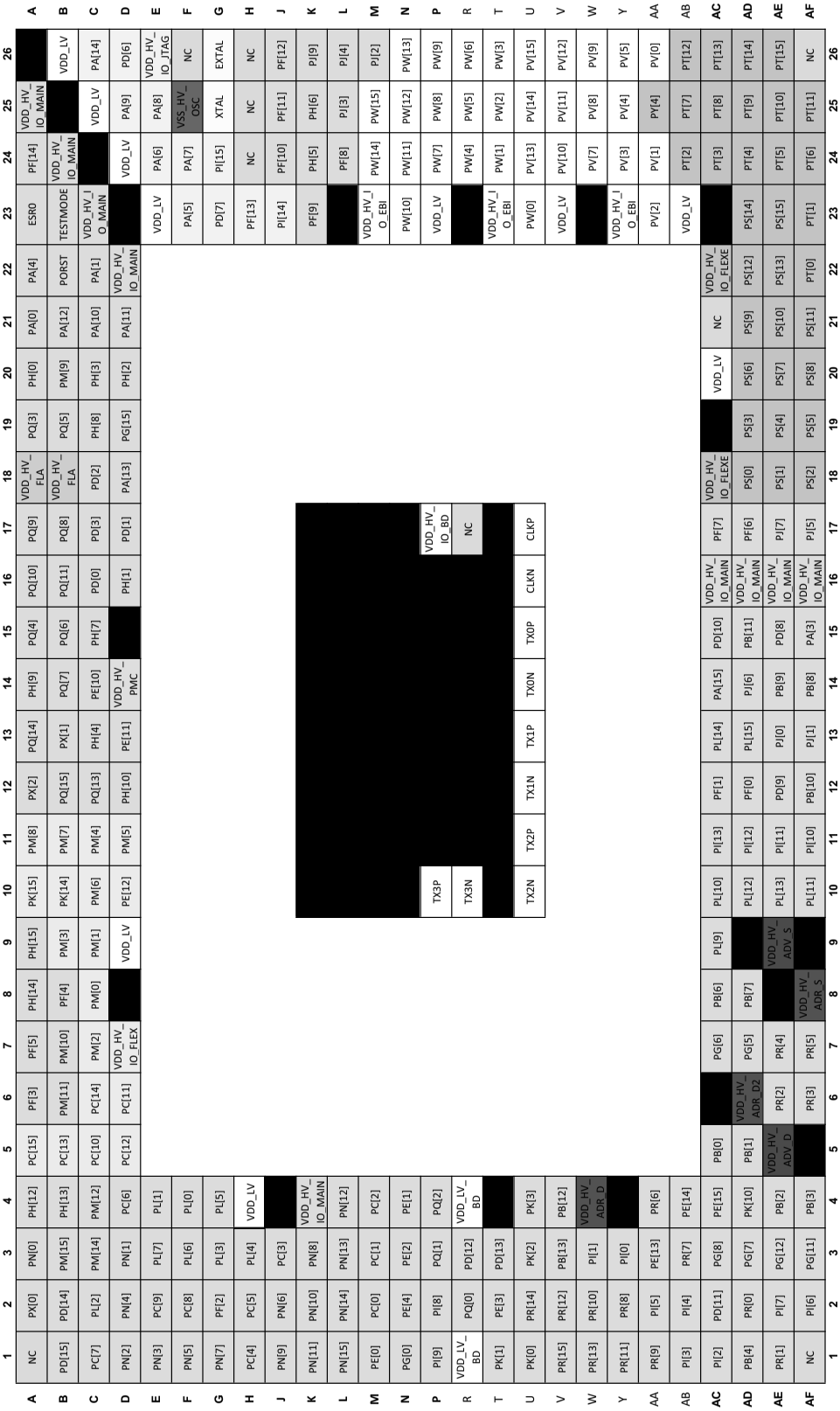

Figure 4. 416-ball BGA emulation device pinout (top view)

Table 4. LVDS pin descriptions (continued)

Functional block	Port pin	Signal	Signal description	Direction	BGA ball (416 PD, 416 ED)	BGA ball (512 PD, 512 ED)
DSPI 4 Microsecond Bus	PD[2]	SCK_P	DSPI 4 Microsecond Bus Serial Clock, LVDS Positive Terminal	O	C18	F17
	PD[3]	SCK_N	DSPI 4 Microsecond Bus Serial Clock, LVDS Negative Terminal	O	C17	G17
	PD[0]	SOUT_P	DSPI 4 Microsecond Bus Serial Data, LVDS Positive Terminal	O	C16	F16
	PD[1]	SOUT_N	DSPI 4 Microsecond Bus Serial Data, LVDS Negative Terminal	O	D17	G16
DSPI 5 Microsecond Bus	PF[10]	SCK_P	DSPI 5 Microsecond Bus Serial Clock, LVDS Positive Terminal	O	J24	W24
	PF[9]	SCK_N	DSPI 5 Microsecond Bus Serial Clock, LVDS Negative Terminal	O	K23	W25
	PF[12]	SOUT_P	DSPI 5 Microsecond Bus Serial Data, LVDS Positive Terminal	O	J26	Y24
	PF[11]	SOUT_N	DSPI 5 Microsecond Bus Serial Data, LVDS Negative Terminal	O	J25	Y25
DSPI 6 Microsecond Bus	PQ[9]	SCK_P	DSPI 6Microsecond Bus Serial Clock, LVDS Positive Terminal	O	A17	A16
	PQ[8]	SCK_N	DSPI 6 Microsecond Bus Serial Clock, LVDS Negative Terminal	O	B17	B16
	PQ[11]	SOUT_P	DSPI 6 Microsecond Bus Serial Data, LVDS Positive Terminal	O	B16	A15
	PQ[10]	SOUT_N	DSPI 6 Microsecond Bus Serial Data, LVDS Negative Terminal	O	A16	B15

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

NOTE

Within this document, $V_{DD\_HV\_IO}$ refers to supply pins $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_IO\_FLEXE}$, $V_{DD\_HV\_IO\_EBI}$, and $V_{DD\_HV\_FLA}$. $V_{DD\_HV\_ADV}$ refers to ADC supply pins $V_{DD\_HV\_ADV\_S}$ and $V_{DD\_HV\_ADV\_D}$. $V_{DD\_HV\_ADR}$ refers to ADC reference pins $V_{DD\_HV\_ADR\_S}$ and $V_{DD\_HV\_ADR\_D}$. $V_{SS\_HV\_ADV}$ refers to ADC ground pins $V_{SS\_HV\_ADV\_S}$ and $V_{SS\_HV\_ADV\_D}$. $V_{SS\_HV\_ADR}$ refers to ADC reference pins $V_{SS\_HV\_ADR\_S}$ and $V_{SS\_HV\_ADR\_D}$.

3.2 Absolute maximum ratings

Table 6 describes the maximum ratings of the device.

Table 6. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
Cycle	SR	Lifetime power cycles	—	—	1000 k	—
V_{DD_LV}	SR	1.2 V core supply voltage[2,3,4]	—	–0.3	1.5	V
$V_{DD\_LV\_BD}$	SR	Emulation module voltage[2,3,4]	—	–0.3	1.5	V
$V_{DD\_HV\_IO}$	SR	I/O supply voltage[5,6]	—	–0.3	6.0	V
$V_{DD\_HV\_PMC}$	SR	Power Management Controller supply voltage[5]	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$	SR	Flash core voltage[7]	—	–0.3	4.5	V
V_{DDSTBY}	SR	RAM standby supply voltage[5]	—	–0.3	6.0	V
$V_{SS\_HV\_ADV}$[8]	SR	SAR and S/D ADC ground voltage	Reference to V_{SS_HV}	–0.3	0.3	V
$V_{DD\_HV\_ADV}$[9]	SR	SAR and S/D ADC supply voltage	Reference to corresponding $V_{SS\_HV\_ADV}$	–0.3	6.0	V
$V_{SS\_HV\_ADR}$[10]	SR	SAR and S/D ADC low reference	Reference to V_{SS_HV}	–0.3	0.3	V
$V_{DD\_HV\_ADR}$[11]	SR	SAR and S/D ADC high reference	Reference to corresponding $V_{SS\_HV\_ADR}$	–0.3	6.0	V
$V_{DD\_HV\_IO\_JTAG}$	SR	Crystal oscillator, FEC MDIO/MDC, LFAST, JTAG[5]	Reference to V_{SS_HV}	–0.3	6.0	V

Table 8. Device operating conditions[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
$V_{DD\_HV\_ADR\_D}$	SR	SD ADC supply reference voltage	Reduced SNR	3.0	$V_{DD\_HV\_ADV\_D}$	4.5	V
			Full SNR	4.5		5.5[32]	
$V_{DD\_HV\_ADR\_D} - V_{DD\_HV\_ADV\_D}$	SR	SD ADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR\_D}$	SR	SD ADC ground reference voltage	—	$V_{SS\_HV\_ADV\_D}$			V
$V_{SS\_HV\_ADR\_D} - V_{SS\_HV\_ADV\_D}$	SR	$V_{SS\_HV\_ADR\_D}$ differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_S}$[35]	SR	SARADC reference	—	2.0	$V_{DD\_HV\_ADV\_S}$	4.0	V
				4.0		5.5[32]	
$V_{SS\_HV\_ADR\_S}$	SR	SAR ADC ground reference voltage	—	$V_{SS\_HV\_ADV\_S}$			V
$V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S}$	SR	SARADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR\_S} - V_{SS\_HV\_ADV\_S}$	SR	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–25	—	25	mV
$V_{SS\_HV\_ADV} - V_{SS}$	SR	$V_{SS\_HV\_ADV}$ differential voltage	—	–25	—	25	mV
V_{RAMP_LV}	SR	Slew rate on core power supply pins	—	—	—	100	V/ms
V_{RAMP_HV}	SR	Slew rate on HV power supply pins	—	—	—	100	V/ms
V_{por_rel}	CC	POR release trip point	-40 °C < Tj < 150 °C	3.10	—	4.26	V
V_{por_hys}	CC	POR hysteresis	-40 °C < Tj < 150 °C	150	—	300	mV
V_{IN}	SR	I/O input voltage range	—	0	—	5.5	V
Injection current							
I_{IC}	SR	DC injection current (per pin)[36,37,38]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	SR	Maximum current per power segment[39]	—	–80	—	80	mA

1 The ranges in this table are design targets and actual data may vary in the given range.

2 Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the *MPC5777M Microcontroller Reference Manual* for more information on the clock limitations for the various IP blocks on the device.

3 Core voltage as measured on device pin to guarantee published silicon performance.

4 During power ramp, voltage measured on silicon might be lower. maximum performance is not guaranteed, but correct silicon operation is guaranteed. Refer to the Power Management and Reset Generation Module chapters in the *MPC5777M Microcontroller Reference Manual* for further information.

[38] The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current is injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.

[39] Sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.

Table 9. Emulation (buddy) device operating conditions[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Frequency							
—	SR	Standard JTAG 1149.1/1149.7 frequency	—	—	—	50	MHz
—	SR	High-speed debug frequency	—	—	—	320	MHz
—	SR	Data trace frequency	—	—	—	1250	MHz
Temperature							
T_{J_BD}	SR	Device junction operating temperature range	—	–40.0	—	150.0	°C
T_{A_BD}	SR	Ambient operating temperature range	—	–40.0	—	125.0	°C
Voltage							
$V_{DD\_LV\_BD}$	SR	Buddy core supply voltage	—	1.2	—	1.365	V
$V_{DD\_HV\_IO\_BD}$	SR	Buddy I/O supply voltage	—	3.0	—	5.5	V
$V_{RAMP\_LV\_BD}$	SR	Buddy slew rate on core power supply pins	—	—	—	100	V/ms
$V_{RAMP\_HV\_BD}$	SR	Buddy slew rate on HV power supply pins	—	—	—	100	V/ms

[1] The ranges in this table are design targets and actual data may vary in the given range.

3.5 DC electrical specifications

The following table describes the DC electrical specifications.

Table 10. DC electrical specifications[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
I_{DD_LV}	CC	Maximum operating current on the V_{DD_LV} supply[2]	T_J = 150 °C V_{DD_LV} = 1.325 V f_{MAX}	—	—	1140	mA
I_{DDAPP_LV}	CC	Application use case operating current on the V_{DD_LV} supply[3]	T_J = 150 °C V_{DD_LV} = 1.325 V f_{MAX}	—	—	950	mA
$I_{DD\_LV\_PE}$	CC	Operating current on the V_{DD_LV} supply for flash program/erase	T_J = 150 °C	—	—	40	mA

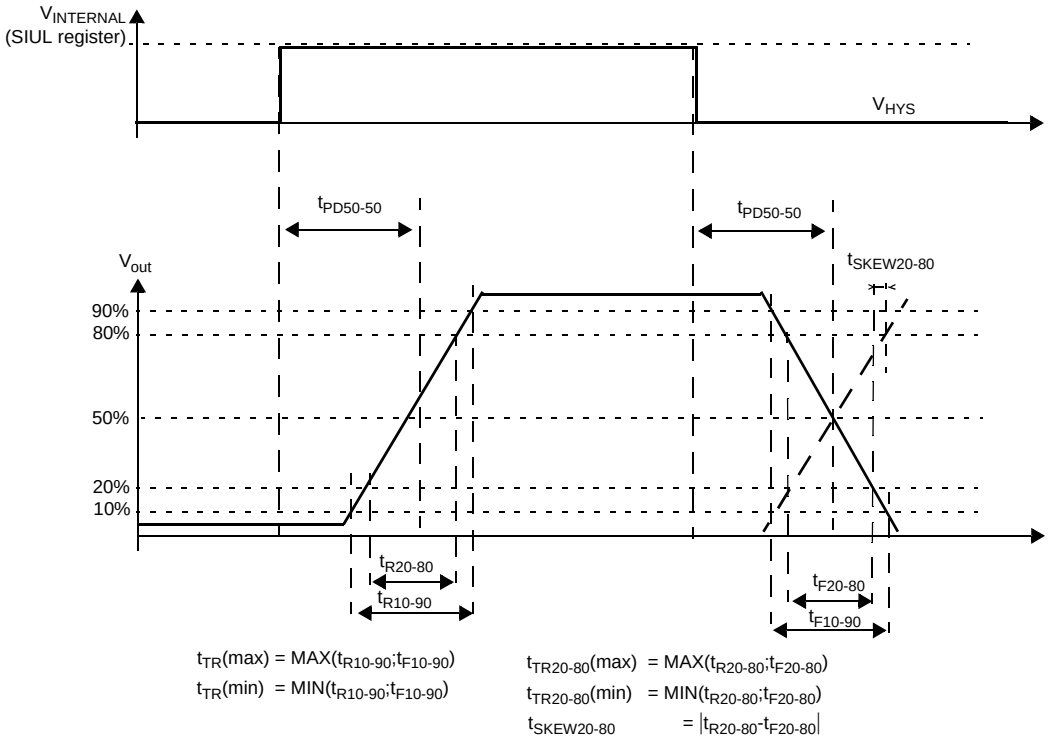

Figure 9. I/O output DC electrical characteristics definition

The following tables provide DC characteristics for bidirectional pads:

- Table 14 provides output driver characteristics for I/O pads when in WEAK configuration.
- Table 15 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 16 provides output driver characteristics for I/O pads when in STRONG configuration.
- Table 17 provides output driver characteristics for I/O pads when in VERY STRONG configuration.
- Table 18 provides output driver characteristics for the EBI pads.

NOTE

Driver configuration is controlled by SIUL2_MSCR*n* registers. It is available within two PBRIDGEA_CLK clock cycles after the associated SIUL2_MSCR*n* bits have been written.

Table 14 shows the WEAK configuration output buffer electrical characteristics.

Table 14. WEAK configuration output buffer electrical characteristics

Symbol		Parameter	Conditions[1,2]	Value			Unit
				Min	Typ	Max	
R_{OH_W}	CC	PMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 0.5 mA	520	800	1052	Ω
R_{OL_W}	CC	NMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 0.5 mA	520	800	1052	Ω

Table 15. MEDIUM configuration output buffer electrical characteristics (continued)

Symbol		Parameter	Conditions[1,2]	Value			Unit
				Min	Typ	Max	
f_{MAX_M}	CC	Output frequency MEDIUM configuration	C_L = 25 pF[3]	—	—	12	MHz
			C_L = 50 pF[3]	—	—	6	
			C_L = 200 pF[3]	—	—	1.5	
$t_{TPD50-50}$[4]	CC	50-50 % Output pad propagation delay time	$V_{DD\_HV\_IO}$ = 5 V +/- 10 %, C_L = 25 pF	—	—	21/17	ns
			$V_{DD\_HV\_IO}$ = 5.0 V +/- 10 %, C_L = 50 pF	—	—	35/27	ns
t_{TR_M}	CC	Transition time output pin MEDIUM configuration[5]	C_L = 25 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	10	—	30	ns
			C_L = 50 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	20	—	60	
			C_L = 200 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	60	—	200	
			C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[6]	12	—	42	
			C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[6]	24	—	86	
			C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[6]	70	—	300	
$\lvert t_{SKEW\_M} \rvert$	CC	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_M}	CC	Maximum DC current	—	—	—	4	mA

1 All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0

2 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

3 C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in Table 12) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).

4 If two values are given for propagation delay, the first value is for rising edge signals and the second for falling edge signals.

5 Transition time maximum value is approximated by the following formula:

0 pF < C_L < 50 pF t_{TR_M}(ns) = 5.6 ns + C_L(pF) × 1.11 ns/pF

50 pF < C_L < 200 pF t_{TR_M}(ns) = 13 ns + C_L(pF) × 0.96 ns/pF

6 Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_FLEX}$ segment when VSIO[VSIO_IF] = 0

Table 16 shows the STRONG configuration output buffer electrical characteristics.

Table 19. I/O consumption[1]

Symbol		Parameter	Conditions[2]	Value			Unit
				Min	Typ	Max	
I_{RMS_W}	CC	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	mA
			C_L = 50 pF, 1 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	
			C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
			C_L = 50 pF, 1 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
I_{RMS_M}	CC	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz V_{DD} = 5.0 V ± 10%	—	—	4.7	mA
			C_L = 50 pF, 6 MHz V_{DD} = 5.0 V ± 10%	—	—	4.8	
			C_L = 25 pF, 12 MHz V_{DD} = 3.3 V ± 10%	—	—	2.6	
			C_L = 50 pF, 6 MHz V_{DD} = 3.3 V ± 10%	—	—	2.7	
I_{RMS_S}	CC	RMS I/O current for STRONG configuration	C_L = 25 pF, 50 MHz V_{DD} = 5.0 V ± 10%	—	—	19	mA
			C_L = 50 pF, 25 MHz V_{DD} = 5.0 V ± 10%	—	—	19	
			C_L = 25 pF, 50 MHz V_{DD} = 3.3 V ± 10%	—	—	10	
			C_L = 50 pF, 25 MHz V_{DD} = 3.3 V ± 10%	—	—	10	
I_{RMS_V}	CC	RMS I/O current for VERY STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0V +/- 10%	—	—	22	mA
			C_L = 50 pF, 25 MHz, V_{DD} = 5.0V ± 10%	—	—	22	
			C_L = 25 pF, 50 MHz, V_{DD} = 3.3V ± 10%	—	—	11	
			C_L = 25 pF, 25 MHz, V_{DD} = 3.3V ± 10%	—	—	11	
I_{RMS_EBI}	CC	RMS I/O current for External Bus output pins	C_{DRV} = 6 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	9	mA
			C_{DRV} = 12 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	15	
			C_{DRV} = 18 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	27	
			C_{DRV} = 30 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	42	

3.9 Oscillator and FMPLL

The Reference PLL (PLL0) and the System PLL (PLL1) generate the system and auxiliary clocks from the main oscillator driver.

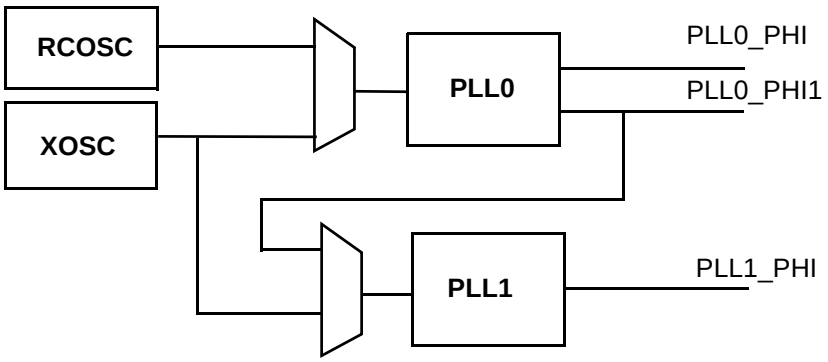

Figure 12. PLL integration

Table 21. PLL0 electrical characteristics

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{PLL0IN}	SR	PLL0 input clock[1,2]	—	8	—	44	MHz
Δ_{PLL0IN}	SR	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	CC	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0VCOFR}$	CC	PLL0 VCO free running frequency	—	35	—	400	MHz
$f_{PLL0PHI}$	CC	PLL0 output frequency	—	4.762	—	400	MHz
$t_{PLL0LOCK}$	CC	PLL0 lock time	—	—	—	110	µs
$\lvert\Delta_{PLL0PHISPJ}\rvert$	CC	PLL0_PHI single period jitter[3] f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI}$ = 400 MHz, 6-sigma	—	—	200	ps
$\lvert\Delta_{PLL0PHI1SPJ}\rvert$	CC	PLL0_PHI1 single period jitter[3] f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma	—	—	300[4]	ps

Table 24. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Load capacitance[1,2] (pF)
00000	1.032
00001	1.976
00010	2.898
00011	3.823
00100	4.751
00101	5.679
00110	6.605
00111	7.536
01000	8.460
01001	9.390
01010	10.317
01011	11.245
01100	12.173
01101	13.101
01110	14.029
01111	14.957

1 Values are determined from simulation across process corners and voltage and temperature variation. Capacitance values vary ±12% across process, 0.25% across voltage, and no variation across temperature.

2 Values in this table do not include the die and package capacitances given by Cs_xtal/Cs_extal in Table 23 (External Oscillator electrical specifications).

Table 27. SARn ADC electrical specification[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{ALTREF}	SR	ADC alternate reference voltage	$V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$	2.0	$V_{DD\_HV\_ADV\_S}$	V
V_{IN}	SR	ADC input signal	$0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$V_{SS\_HV\_ADR\_S}$	$V_{DD\_HV\_ADR\_S}$	V
f_{ADCK}	SR	Clock frequency	$T_J < 150$ °C	7.5	14.6	MHz
$t_{ADCPRECH}$	SR	ADC precharge time	Fast SAR—fast precharge	135	—	ns
			Fast SAR—full precharge	270	—	
			Slow SAR (SARADC_B)—fast precharge	270	—	
			Slow SAR (SARADC_B)—full precharge	540	—	
ΔV_{PRECH}	SR	Precharge voltage precision	Full precharge $V_{PRECH} = V_{DD\_HV\_ADR\_S}/2$ $T_J < 150$ °C	–0.25	0.25	V
			Fast precharge $V_{PRECH} = V_{DD\_HV\_ADR\_S}/2$ $T_J < 150$ °C	–0.5	0.5	V
ΔV_{INTREF}	CC	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR\_S}$, 1/3 * $V_{DD\_HV\_ADR\_S}$, 2/3 * $V_{DD\_HV\_ADR\_S}$, $V_{DD\_HV\_ADR\_S}$)	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	ADC sample time[2]	Fast SAR – 12-bit configuration	0.750	—	µs
			Slow SAR (SARADC_B) – 12-bit configuration	1.500	—	
$t_{ADCEVAL}$	SR	ADC evaluation time	12-bit configuration (25 clock cycles)	1.712	—	µs
$I_{ADCREFH}$[3,4]	CC	ADC high reference current	Run mode $t_{conv} \geq 5$ µs (average across all codes)	—	7	µA
			Run mode $t_{conv} = 2.5$ µs (average across all codes)	—	7	
			Power Down mode	—	6	
			Bias Current[5]	—	+2	
$I_{ADCREFL}$[4]	CC	ADC low reference current	Run mode $t_{conv} \geq 5$ µs $V_{DD\_HV\_ADR\_S}$ <= 5.5 V	—	15	µA
			Run mode $t_{conv} = 2.5$ µs $V_{DD\_HV\_ADR\_S}$ <= 5.5 V	—	30	
			Power Down mode $V_{DD\_HV\_ADR\_S}$ <= 5.5 V	—	1	

Table 27. SARn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
ΔTUE_{12}	CC	TUE degradation due to $V_{DD\_HV\_ADR\_S}$ offset with respect to $V_{DD\_HV\_ADV\_S}$	$V_{IN} < V_{DD\_HV\_ADV\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in$ [0:25 mV]	0	0	LSB (12b)
			$V_{IN} < V_{DD\_HV\_ADV\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in$ [25:50 mV]	–2	2	
			$V_{IN} < V_{DD\_HV\_ADV\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in$ [50:75 mV]	–4	4	
			$V_{IN} < V_{DD\_HV\_ADV\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in$ [75:100 mV]	–6	6	
			$V_{DD\_HV\_ADV\_S} < V_{IN} < V_{DD\_HV\_ADR\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in$ [0:25 mV]	–2.5	2.5	
			$V_{DD\_HV\_ADV\_S} < V_{IN} < V_{DD\_HV\_ADR\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in$ [25:50 mV]	–4	4	
			$V_{DD\_HV\_ADV\_S} < V_{IN} < V_{DD\_HV\_ADR\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in$ [50:75 mV]	–7	7	
			$V_{DD\_HV\_ADV\_S} < V_{IN} < V_{DD\_HV\_ADR\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in$ [75:100 mV]	–12	12	
DNL	CC	Differential non-linearity	$V_{DD\_HV\_ADV\_S} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	LSB (12b)
INL	CC	Integral non-linearity	4.0 V < $V_{DD\_HV\_ADV\_S}$ < 5.5 V 4.0 V < $V_{DD\_HV\_ADR\_S}$ < 5.5 V	–3	3	LSB (12b)
			$V_{DD_HV_ADV_S} = 2$V $V_{DD\_HV\_ADR\_S} = 2$ V	–5	5	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Please refer to Figure 14 and Figure 15 for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.

3 $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.

4 Current parameter values are for a single ADC.

5 Extra bias current is present only when BIAS is selected.

Table 47. Nexus debug port timing[1] (continued)

#	Symbol		Characteristic	Value		Unit
				Min	Max	
12	t_{NTDIH}	CC	TDI/TDIC data hold time	5	—	ns
13[9]	t_{NTMSS}	CC	TMS/TMSC data setup time	5	—	ns
14	t_{NTMSH}	CC	TMS/TMSC data hold time	5	—	ns
15[10]	—	CC	TDO/TDOC propagation delay from falling edge of TCK[11]	—	16	ns
16	—	CC	TDO/TDOC hold time with respect to TCK falling edge (minimum TDO/TDOC propagation delay)	2.25	—	ns

1 Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.

2 t_{CYC} is system clock period.

3 Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.

4 This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.

5 This value is TDO/TDOC propagation time 36ns + 4 ns setup time to sampling edge.

6 This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

7 This value is TDO/TDOC propagation time 16ns + 4 ns setup time to sampling edge.

8 TDIC represents the TDI bit frame of the scan packet in compact JTAG 2-wire mode.

9 TMSC represents the TMS bit frame of the scan packet in compact JTAG 2-wire mode.

10 TDOC represents the TDO bit frame of the scan packet in compact JTAG 2-wire mode.

11 Timing includes TCK pad delay, clock tree delay, logic delay and TDO/TDOC output pad delay.

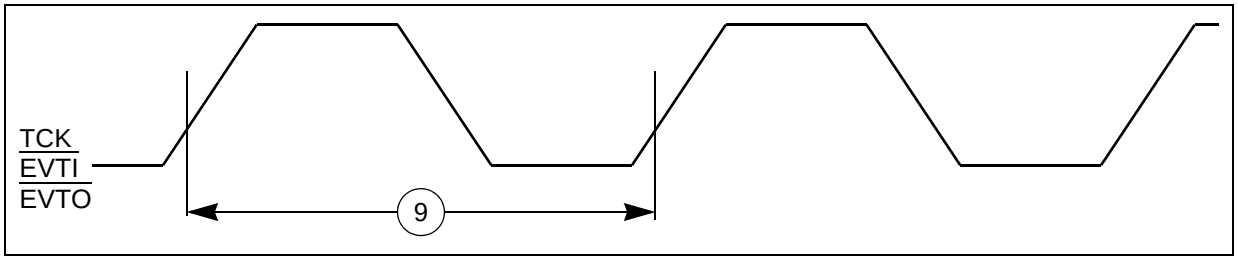

Figure 26. Nexus event trigger and test clock timings

Table 51. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
10	t_{HO}	CC	SOUT data hold time after SCK[10]	SOUT and SCK drive strength				
				Very strong	25 pF	–7.7	—	ns
				Strong	50 pF	–11.0	—	
				Medium	50 pF	–15.0	—	

1 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

2 All timing values for output signals in this table are measured to 50% of the output voltage.

3 Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.

4 N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

5 t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).

6 M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

7 t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.

8 PCSx and PCSS using same pad configuration.

9 Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.

10 SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 52. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
5	t_{PCSC}	CC	PCSx to $\overline{PCSS}$ time[8]	PCS and PCSS drive strength				
				Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	$\overline{PCSS}$ to PCSx time[8]	PCS and PCSS drive strength				
				Strong	25 pF	16.0	—	ns
SIN setup time								
7	t_{SUI}	CC	SIN setup time to SCK CPHA = 0[9]	SCK drive strength				
				Very strong	25 pF	$25 – (P^{10} \times t_{SYS}^{5})$	—	ns
				Strong	50 pF	$32.75 – (P^{10} \times t_{SYS}^{5})$	—	
				Medium	50 pF	$52 – (P^{10} \times t_{SYS}^{5})$	—	
			SIN setup time to SCK CPHA = 1[9]	SCK drive strength				
				Very strong	25 pF	25.0	—	ns
				Strong	50 pF	32.75	—	
				Medium	50 pF	52.0	—	
SIN hold time								
8	t_{HI}	CC	SIN hold time from SCK CPHA = 0[9]	SCK drive strength				
				Very strong	0 pF	$–1 + (P^{9} \times t_{SYS}^{4})$	—	ns
				Strong	0 pF	$–1 + (P^{9} \times t_{SYS}^{4})$	—	
				Medium	0 pF	$–1 + (P^{9} \times t_{SYS}^{4})$	—	
			SIN hold time from SCK CPHA = 1[9]	SCK drive strength				
				Very strong	0 pF	–1.0	—	ns
				Strong	0 pF	–1.0	—	
				Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	SOUT data valid time from SCK CPHA = 0[10]	SOUT and SCK drive strength				
				Very strong	25 pF	—	$7.0 + t_{SYS}^{5}$	ns
				Strong	50 pF	—	$8.0 + t_{SYS}^{5}$	
				Medium	50 pF	—	$16.0 + t_{SYS}^{5}$	
			SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength				
				Very strong	25 pF	—	7.0	ns
				Strong	50 pF	—	8.0	
				Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)								

3.16.4 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals.

These are recommended numbers as per the FlexRay EPL v3.0 specification.

3.16.4.1 TxEN

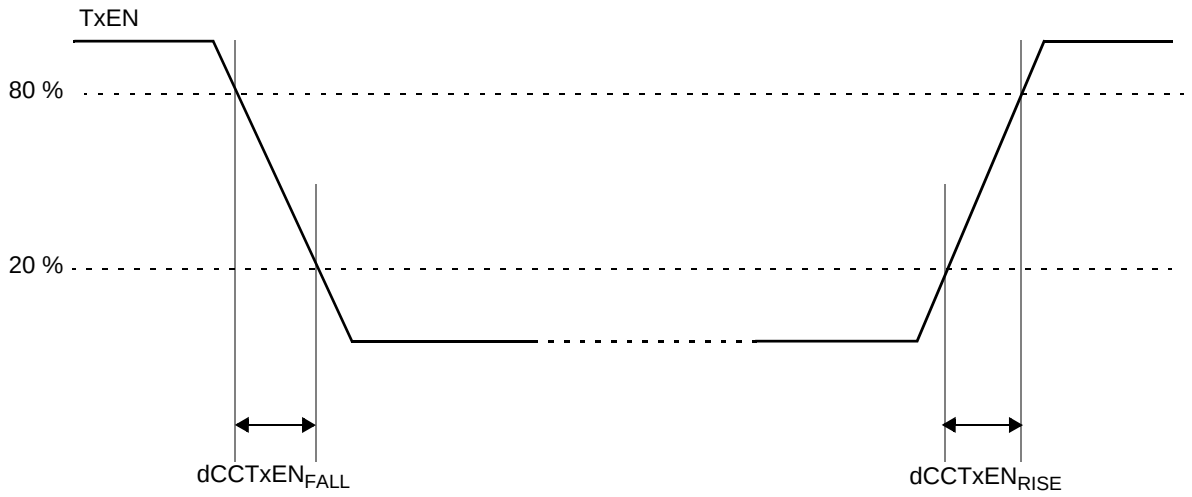

Figure 46. TxEN signal

Table 64. TxEN output characteristics[1]

Symbol		Characteristic	Value		Unit
			Min	Max	
dCCTxEN$_{RISE25}$	CC	Rise time of TxEN signal at CC	—	9	ns
dCCTxEN$_{FALL25}$	CC	Fall time of TxEN signal at CC	—	9	ns
dCCTxEN$_{01}$	CC	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
dCCTxEN$_{10}$	CC	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1 TxEN pin load maximum 25 pF

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Package pinouts and signal descriptions (con't)**
		Table 4 (LVDS pin descriptions): • In SIPI/LFAST, Differential DSPI2, and Differential DSPI 5 groups, changed port pin "PF[7]" to "PD[7]" • Changed the polarity of the signal assigned to several port pins. For example, the signal for port pin PD[7] has been changed to "SIPI_RXP" (was SIPI_RXN) and "Interprocessor Bus LFAST, LVDS Receive Positive Terminal" (was "Interprocessor Bus LFAST, LVDS Receive Negative Terminal"). This change affects port pins PD[7], PF[13], PA[14], PD[6], PA[7], PA[8], PD[2], PD[3], PD[0], PD[1], PF[10], PF[9], PF[11], PF[12], PQ[8], PQ[9], PQ[10], PQ[11], PI[14], and PI[15]. • Added package ball locations
		Electrical characteristics—Miscellaneous
		Section 3, Electrical characteristics: • Thermal characteristics section has been moved to Package characteristics section. • Following note removed: "All parameter values in this document are tested with nominal supply voltage values (VDD_LV = 1.25 V, VDD_HV = 5.0 V ± 10%, VDD_HV_IO = 5.0 V ± 10% or 3.3 V ± 10%) and TA = –40 to 125 °C unless otherwise specified.". Operating conditions will appear elsewhere in the data sheet. • Added VDD_HV_IO_FLEX before VDD_HV_FLA in the second note on the page
		Electrical characteristics—Absolute maximum ratings
		Table 6 (Absolute maximum ratings): • I_{MAXD} specification now given by pad type (Medium, Strong, and Very Strong) • I_{MAXA} specification deleted. • New specification: I_{INJD} (Maximum DC injection current for digital pad) • New specification: I_{INJA} (Maximum DC injection current for analog pad) • New specification: I_{MAXSEG} (Maximum current per power segment) • New specification: V_{FERS} (Flash erase acceleration supply) • New specification: $V_{DD\_HV\_IO\_EBI}$ (External Bus Interface supply) • Changed "Emulation module supply" to "BD supply" in the VDD_LV_BD – BDD_LV row • Maximum junction temperature changed from 125 °C to 165 °C in cumulative time limits on voltage levels for V_{DD_LV} and $V_{DD\_LV\_BD}$ • Footnote added to V_{FERS}: V_{FERS} is a factory test supply pin that is used to reduce the erase time of the flash. It is only available in bare die devices. There is no V_{FERS} pin in the packaged devices. The V_{FERS} supply pad can be bonded to ground (V_{SS_HV}) to disable, or connected to 5.0 V ± 5% to use the flash erase acceleration feature. Pad can be left at 5 V ± 5% in normal operation. • Footnote added to V_{IN}: "The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations." • Footnote V_{DD_LV} changed: "1.32 – 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.288 V at maximum T_J = 165 °C" (was 1.275)

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—Oscillator and FMPLL (con't)**
		Table 23 (External Oscillator electrical specifications): • New specification: V_{HYS} (Comparator Hysteresis) • New specification: V_{EXTAL} (Oscillation Amplitude on the EXTAL pin after startup) • Specification change: f_{XTAL} range values changed: f_{XTAL} ranges are 4–8 MHz, >8–20 MHz, and >20–40 MHz (previously stated as 4–8 MHz, 8–16 MHz, and 20–40 MHz • Specification change t_{cst} (Crystal start-up time) is now specified by temperature range • Specification change: V_{IHEXT} specified at V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$ (previously specified at V_{DDOSC} = 3.0 V and V_{DDOSC} = 5.5 V) • Specification change: V_{ILEXT} specified at V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$ (previously specified at V_{DDOSC} = 3.0 V and V_{DDOSC} = 5.5 V) • Specification change: C_{S_EXTAL} values specified by package (was previously based on selected load capacitance value) • Specification change: C_{S_XTAL} values specified by package (was previously based on selected load capacitance value) • Specification change: g_m (Oscillator Transconductance) is now specified by temperature and frequency range conditions (was previously specified without conditions) • Footnote added: "All oscillator specifications are valid for $V_{DD\_HV\_IO\_JTAG}$ = 3.0 V – 5.5 V." • Footnote added to C_{S_EXTAL}, C_{S_XTAL} to refer to crystal manufacturer's specifications for load capacitance values. • Footnote added: "Amplitude on the EXTAL pin after startup is determined by the ALC block, i.e., the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions." • Footnote added: "I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2–3 mA range and is dependent on the load and series resistance of the crystal." • V_{ILEXT} parameter, changed "External Reference" to "External Clock Input" • V_{ILEXT} parameter, added footnote: This parameter is guaranteed by design rather than 100% tested. Table 24 (Selectable load capacitance): • Changed footnote 2 from "Values in this table do not include 8 pF routing and ESD structure on die and package trace capacitance." to "Values in this table do not include the die and package capacitances given by Cs_xtal/Cs_extal in Table 23 (External Oscillator electrical specifications)."
		Electrical characteristics—ADC specifications
		Section 3.10.1, ADC input description Table 26 (ADC pin specification) • I_{LK_IN} specification change: removed T_A = 125 °C row from (T_A = 125 °C) • I_{LK_INUD}, I_{LK_INUSD}, I_{LK_INREF}, and I_{LK_INOUT} specification changes to parameters, conditions, and values. • Specification change: I_{INJ} min value is –3 mA (was –1) • Specification change: C_S max value is 8.5 pF (was 7) • Specification change: R_{SWn} max value for SARn channels is 1.1 kΩ (was 0.6)

Table 76. Revision history (continued)

Revision	Date	Description of changes
4	9/2014	**Electrical characteristics—DC electrical specification**
		• In Section 3.1, Introduction, added the following to note text: "$V_{DD\_HV\_ADV}$ refers to ADC supply pins $V_{DD\_HV\_ADV\_S}$ and $V_{DD\_HV\_ADV\_D}$. $V_{DD\_HV\_ADR}$ refers to ADC reference pins $V_{DD\_HV\_ADR\_S}$ and $V_{DD\_HV\_ADR\_D}$. $V_{SS\_HV\_ADV}$ refers to ADC ground pins $V_{SS\_HV\_ADV\_S}$ and $V_{SS\_HV\_ADV\_D}$. $V_{SS\_HV\_ADR}$ refers to ADC reference pins $V_{SS\_HV\_ADR\_S}$ and $V_{SS\_HV\_ADR\_D}$." • In Table 10 (DC electrical specifications), changed $I_{DD\_HV\_PMC}$ maximum for PMC only condition (was 5 mA, is 25 mA). Added “This includes PMC consumption, LFAST PLL regulator current, and Nwell bias regulator current” to footnote associated with this value. • In Table 10 (DC electrical specifications), changed I_{DD_LV} maximum to 1140 mA (was 600 mA) and added “V_{DD_LV} = 1.325 V” to conditions. • In Table 10 (DC electrical specifications), added I_{DDAPP_LV} specification. • In Table 10 (DC electrical specifications), changed the conditions for I_{DDSTBY_RAM} and I_{DDSTBY_REG} (were “...to 6 V...”, are “...to 5.5 V...”). • In Table 10 (DC electrical specifications), I_{DDSTBY_RAM} specification: changed max value for 40°C condition to 60 µA (was 40). Changed max value for 85°C condition to 100 µA (was 60). • In Table 10 (DC electrical specifications), V_{STBY_BO} specification: changed min value to 0.9 V (was 0.8).
		Electrical characteristics—I/O pad current specification
		• Table 12 (I/O input DC electrical characteristics), Table 13 (I/O pull-up/pull-down DC electrical characteristics), Table 14 (WEAK configuration output buffer electrical characteristics), Table 15 (MEDIUM configuration output buffer electrical characteristics), Table 16 (STRONG configuration output buffer electrical characteristics), Table 17 (VERY STRONG configuration output buffer electrical characteristics), Table 19 (I/O consumption) added the following footnote to Conditions heading: “During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characterstics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.” • Table 12 (I/O input DC electrical characteristics): V_{HYSTTL} specification: changed min value to 0.275 (was 0.3). V_{HYSAUT} specification: changed min value to 0.4 (was 0.5). • Table 12 (I/O input DC electrical characteristics), changed V_{IHCMOS_H} min value to “0.70 * $V_{DD\_HV\_IO}$” (was 0.65 * $V_{DD\_HV\_IO}$). • In Table 12 (I/O input DC electrical characteristics), changed V_{IHAUT} min value to 3.9 V (was 3.8). • Table 12 (I/O input DC electrical characteristics), revised I_{LKG} and I_{LKG_EBI} rows.

Table 76. Revision history (continued)

Revision	Date	Description of changes
4	9/2014	**Electrical characteristics—I/O pad current specification**
		• Table 14 (WEAK configuration output buffer electrical characteristics), R_{OH_W} and R_{OL_W}: changed min value to 517 (was 560) and max value to 1052 (was 1040). • Table 15 (MEDIUM configuration output buffer electrical characteristics), R_{OH_M} and R_{OL_M}: changed min value to 135 (was 140). • Table 16 (STRONG configuration output buffer electrical characteristics), R_{OH_S} and R_{OL_S}: changed min value to 30 (was 35) and max value to 77 (was 65). • Table 17 (VERY STRONG configuration output buffer electrical characteristics), revised R_{OH_V} and R_{OL_V} conditions. • Table 17 (VERY STRONG configuration output buffer electrical characteristics), R_{OH_V} and R_{OL_V}: changed max values to 72 (was 60) and 90 (was 75). • Table 18 (EBI pad output electrical specification), $R_{OH\_EBI\_GPIO}$ and $R_{OL\_EBI\_GPIO}$: changed max value to 400 (was 260). • In Table 18 (EBI pad output electrical specification): $V_{IHCMOS\_H\_EBI}$ specification: changed max value to "$V_{DD\_HV\_IO\_EBI}$ + 0.3" (was "$V_{DD\_HV\_IO}$ + 0.3"). $R_{OH\_EBI\_GPIO}$ specification: changed condition to "4.5 V < $V_{DD\_HV\_IO\_EBI}$ < 5.5 V" (was "3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V"). $R_{OL\_EBI\_GPIO}$ specification: changed condition to "4.5 V < $V_{DD\_HV\_IO\_EBI}$ < 5.5 V" (was "3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V").
		Electrical characteristics—Oscillator and FMPLL
		• In Table 23 (External Oscillator electrical specifications), deleted the transconductance specification (g_m).
		Electrical characteristics—ADC specifications
		• Table 26 (ADC pin specification), I_{LK_INUD} specification: changed T_J < 40 °C condition max value to 50 nA (was 70). Changed T_J< 150 °C condition max value to 150 nA (was 220). • In Table 27 (SARn ADC electrical specification): added condition rows for full and fast precharge to $t_{ADCPRECH}$, revised condition entries for ΔV_{PRECH}. • In Table 28 (SDn ADC electrical specification), changed the max value for $t_{LATENCY}$ at HPF = OFF (was 2*δ_{GROUP}, is δ_{GROUP}). • In Table 28 (SDn ADC electrical specification), changed the max value for GAIN (was 15, is 16). • Table 28 (SDn ADC electrical specification), SNR_{SE150}: changed GAIN=1 min value to 72 (was 74), GAIN=2 min value to 69 (was 71), GAIN=4 min value to 66 (was 68), GAIN=8 min value to 63 (was 65), and GAIN=16 min value to 60 (was 62). • Table 28 (SDn ADC electrical specification), δ_{GROUP} specification: changed OSR = 75 max value to 696 Tclk (was 746), changed OSR = 96 max value to 946.5 Tclk (was 946.4). • In Table 28 (SDn ADC electrical specification), added footnote to parameter column for $t_{LATENCY}$.
		Electrical characteristics—Power management: PMC, POR/LVD, sequencing
		• In Section 3.16, Power management: PMC, POR/LVD, sequencing, replaced PMC operating conditions and external regulators supply voltage table with a cross reference to Table 8 (Device operating conditions). • In Table 35 (Device power supply integration), changed minimum VDD_LV external capacitance footnote to "variation over voltage, temperature, and aging" (was "variation over process, voltage, temperature, and aging.") • In Table 36 (Flash power supply), revised table footnotes and added new "After trimming; 25°C < TJ ≤ 150°C" condition to $V_{DD\_HV\_FLA}$.