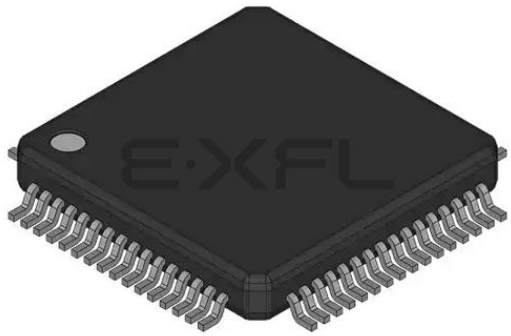

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8027vlh

Table 2-2 56F8037/56F8027 Pins (Continued)

			Peripherals:												
Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**QSCI**	**QSPI**	**ADC**	**PWM**	**Quad Timer**	**DAC**	**Comp**	**MSCAN**	**Power & Ground**	**JTAG**	**Misc.**
28	**VCAP**	V_{CAP}											**V_{CAP}**		
29	**TCK**	TCK, GPIOD2	D2											**TCK**	
30	**GPIOB10**	GPIOB10, CMPAO, TB0	**B10**						TB0		CMPAO				
31	**RESET**	$\overline{\text{RESET}}$, GPIOA7	A7												**$\overline{\text{RESET}}$**
32	**GPIOB3**	GPIOB3, MOSI0, TA3, PSRC1	**B3**			MOSI0		PSRC1	TA3						
33	**GPIOB2**	GPIOB2, MISO0, TA2, PSRC0	**B2**			MISO0		PSRC0	TA2						
34	**GPIOA6**	GPIOA6, FAULT0, TA0	**A6**					FAULT0	TA0						
35	**GPIOA10**	GPIOA10, TB2, CMPAI2	**A10**						TB2		CMPAI2				
36	**GPIOA8**	GPIOA8, FAULT1, TA2, CMPAI1	**A8**					FAULT1	TA2		CMPAI1				
37	**GPIOA12**	GPIOA12, TB1, SCLK1, TA1	**A12**			SCLK1			TB1 TA1						
38	**GPIOB4**	GPIOB4, $\overline{\text{SS1}}$, TB0, TA0, PSRC2, CLKO	**B4**			$\overline{\text{SS1}}$		PSRC2	TA0 TB0						CLKO
39	**GPIOA5**	GPIOA5, PWM5, TA3, FAULT2	**A5**					PWM5 FAULT2	TA3						
40	**VSS**	V_{SS}											**V_{SS}**		
41	**VDD**	V_{DD}											**V_{DD}**		
42	**GPIOB0**	GPIOB0, SCLK0, SCL	**B0**	SCL		SCLK0									
43	**GPIOA4**	GPIOA4, PWM4, TA2, FAULT1	**A4**					PWM4 FAULT1	TA2						
44	**GPIOA13**	GPIOA13, TB2, MISO1, TA2	**A13**			MISO1			TB2 TA2						
45	**GPIOA14**	GPIOA14, TB3, MOSI1, TA3	**A14**			MOSI1			TB3 TA3						
46	**GPIOB9**	GPIOB9, SDA, CANRX	**B9**	SDA								CANRX			
47	**GPIOA2**	GPIOA2, PWM2	**A2**					PWM2							
48	**GPIOA3**	GPIOA3, PWM3	**A3**					PWM3							
49	**VCAP**	V_{CAP}											**V_{CAP}**		
50	**VDD**	V_{DD}											**V_{DD}**		
51	**VSS**	V_{SS}											**V_{SS}**		
52	**GPIOD5**	GPIOD5, XTAL, CLKIN	**D5**												XTAL CLKIN
53	**GPIOD4**	GPIOD4, EXTAL	**D4**												EXTAL
54	**GPIOB8**	GPIOB8, SCL, CANTX	**B8**	SCL								CANTX			
55	**GPIOA1**	GPIOA1, PWM1	**A1**					PWM1							

Table 2-3 56F8037/56F8027 Signal and Package Information for the 64-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB9 **(SDA[25])** **(CANRX[26])**	46	Input/ Output Input/ Output Input	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **Serial Data 1** — This pin serves as the I^2C serial data line. **CAN Receive Data** — This is the MSCAN interface input. After reset, the default state is GPIOB9. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[25]The SDA signal is also brought out on the GPIOB1 and GPIOB6 pins. [26]The CANRX signal is also brought out on the GPIOB13 pin.				
GPIOB10 **(TB0[27])** **(CMPAO)**	30	Input/ Output Input/ Output Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **TB0**— Timer B, Channel 0. **Comparator A Output**— This is the output of comparator A. After reset, the default state is GPIOB10. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[27]The TB0 signal is also brought out on the GPIOB4 pin.				
GPIOB11 **(TB1[28])** **(CMPBO)**	60	Input/ Output Input/ Output Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **TB1**— Timer B, Channel 1. **Comparator B Output**— This is the output of comparator B. After reset, the default state is GPIOB11. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[28]The TB1 signal is also brought out on the GPIOA12 pin.				

Return to Table 2-2

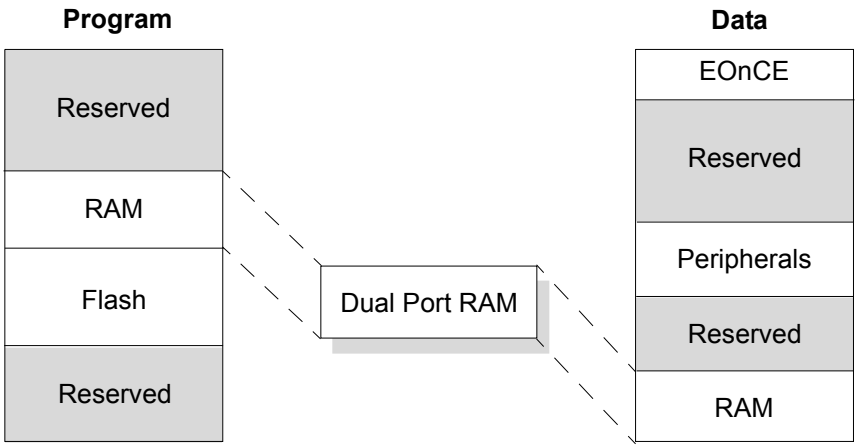

Figure 4-2 Dual Port RAM for 56F8027

4.5 EOnCE Memory Map

Figure 4-7 lists all EOnCE registers necessary to access or control the EOnCE.

Table 4-7 EOnCE Memory Map

Address	Register Acronym	Register Name
X:$FF FFFF	OTX1 / ORX1	Transmit Register Upper Word Receive Register Upper Word
X:$FF FFFE	OTX / ORX (32 bits)	Transmit Register Receive Register
X:$FF FFFD	OTXRXSR	Transmit and Receive Status and Control Register
X:$FF FFFC	OCLSR	Core Lock / Unlock Status Register
X:$FF FFFB - X:$FF FFA1		Reserved
X:$FF FFA0	OCR	Control Register
X:$FF FF9F		Instruction Step Counter
X:$FF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:$FF FF9D	OSR	Status Register
X:$FF FF9C	OBASE	Peripheral Base Address Register
X:$FF FF9B	OTBCR	Trace Buffer Control Register
X:$FF FF9A	OTBPR	Trace Buffer Pointer Register
X:$FF FF99		Trace Buffer Register Stages
X:$FF FF98	OTB (21 - 24 bits/stage)	Trace Buffer Register Stages
X:$FF FF97		Breakpoint Unit Control Register
X:$FF FF96	OBCR (24 bits)	Breakpoint Unit Control Register
X:$FF FF95		Breakpoint Unit Address Register 1
X:$FF FF94	OBAR1 (24 bits)	Breakpoint Unit Address Register 1
X:$FF FF93		Breakpoint Unit Address Register 2

Table 4-11 Analog-to-Digital Converter Registers Address Map (ADC_BASE = $00 F080)

Register Acronym	Address Offset	Register Description
ADC_CTRL1	$0	Control Register 1
ADC_CTRL2	$1	Control Register 2
ADC_ZXCTRL	$2	Zero Crossing Control Register
ADC_CLIST 1	$3	Channel List Register 1
ADC_CLIST 2	$4	Channel List Register 2
ADC_CLIST 3	$5	Channel List Register 3
ADC_CLIST 4	$6	Channel List Register 4
ADC_SDIS	$7	Sample Disable Register
ADC_STAT	$8	Status Register
ADC_RDY	$9	Conversion Ready Register
ADC_LIMSTAT	$A	Limit Status Register
ADC_ZXSTAT	$B	Zero Crossing Status Register
ADC_RSLT0	$C	Result Register 0
ADC_RSLT1	$D	Result Register 1
ADC_RSLT2	$E	Result Register 2
ADC_RSLT3	$F	Result Register 3
ADC_RSLT4	$10	Result Register 4
ADC_RSLT5	$11	Result Register 5
ADC_RSLT6	$12	Result Register 6
ADC_RSLT7	$13	Result Register 7
ADC_RSLT8	$14	Result Register 8
ADC_RSLT9	$15	Result Register 9
ADC_RSLT10	$16	Result Register 10
ADC_RSLT11	$17	Result Register 11
ADC_RSLT12	$18	Result Register 12
ADC_RSLT13	$19	Result Register 13
ADC_RSLT14	$1A	Result Register 14
ADC_RSLT15	$1B	Result Register 15
ADC_LOLIM0	$1C	Low Limit Register 0
ADC_LOLIM1	$1D	Low Limit Register 1
ADC_LOLIM2	$1E	Low Limit Register 2
ADC_LOLIM3	$1F	Low Limit Register 3
ADC_LOLIM4	$20	Low Limit Register 4
ADC_LOLIM5	$21	Low Limit Register 5
ADC_LOLIM6	$22	Low Limit Register 6
ADC_LOLIM7	$23	Low Limit Register 7

Table 4-11 Analog-to-Digital Converter Registers Address Map (Continued) (ADC_BASE = $00 F080)

Register Acronym	Address Offset	Register Description
ADC_HILIM0	$24	High Limit Register 0
ADC_HILIM1	$25	High Limit Register 1
ADC_HILIM2	$26	High Limit Register 2
ADC_HILIM3	$27	High Limit Register 3
ADC_HILIM4	$28	High Limit Register 4
ADC_HILIM5	$29	High Limit Register 5
ADC_HILIM6	$2A	High Limit Register 6
ADC_HILIM7	$2B	High Limit Register 7
ADC_OFFST0	$2C	Offset Register 0
ADC_OFFST1	$2D	Offset Register 1
ADC_OFFST2	$2E	Offset Register 2
ADC_OFFST3	$2F	Offset Register 3
ADC_OFFST4	$30	Offset Register 4
ADC_OFFST5	$31	Offset Register 5
ADC_OFFST6	$32	Offset Register 6
ADC_OFFST7	$33	Offset Register 7
ADC_PWR	$34	Power Control Register
ADC_CAL	$35	Calibration Register
		Reserved

Table 4-12 Pulse Width Modulator Registers Address Map (PWM_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
PWM_CTRL	$0	Control Register
PWM_FCTRL	$1	Fault Control Register
PWM_FLTACK	$2	Fault Status Acknowledge Register
PWM_OUT	$3	Output Control Register
PWM_CNTR	$4	Counter Register
PWM_CMOD	$5	Counter Modulo Register
PWM_VAL0	$6	Value Register 0
PWM_VAL1	$7	Value Register 1
PWM_VAL2	$8	Value Register 2
PWM_VAL3	$9	Value Register 3
PWM_VAL4	$A	Value Register 4
PWM_VAL5	$B	Value Register 5
PWM_DTIM0	$C	Dead Time Register 0

Table 4-21 GPIOD Registers Address Map (GPIOD_BASE = $00 F180)

Register Acronym	Address Offset	Register Description
GPIOD_PUPEN	$0	Pull-up Enable Register
GPIOD_DATA	$1	Data Register
GPIOD_DDIR	$2	Data Direction Register
GPIOD_PEREN	$3	Peripheral Enable Register
GPIOD_IASSRT	$4	Interrupt Assert Register
GPIOD_IEN	$5	Interrupt Enable Register
GPIOD_IPOL	$6	Interrupt Polarity Register
GPIOD_IPEND	$7	Interrupt Pending Register
GPIOD_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOD_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOD_RDATA	$A	Raw Data Input Register
GPIOD_DRIVE	$B	Output Drive Strength Control Register

Table 4-22 Programmable Interval Timer 0 Registers Address Map (PIT0_BASE = $00 F190)

Register Acronym	Address Offset	Register Description
PIT0_CTRL	$0	Control Register
PIT0_MOD	$1	Modulo Register
PIT0_CNTR	$2	Counter Register

Table 4-23 Programmable Interval Timer 1 Registers Address Map (PIT1_BASE = $00 F1A0)

Register Acronym	Address Offset	Register Description
PIT1_CTRL	$0	Control Register
PIT1_MOD	$1	Modulo Register
PIT1_CNTR	$2	Counter Register

Table 4-24 Programmable Interval Timer 2 Registers Address Map (PIT2_BASE = $00 F1B0)

Register Acronym	Address Offset	Register Description
PIT2_CTRL	$0	Control Register
PIT2_MOD	$1	Modulo Register

5.6.1.5 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)— Bits 7–6

This field is used to set the interrupt priority level for the EOnCE Transmit Register Empty IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.6 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)— Bits 5–4

This field is used to set the interrupt priority level for the EOnCE Trace Buffer IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.7 EOnCE Breakpoint Unit Interrupt Priority Level (BKPT_U IPL)— Bits 3–2

This field is used to set the interrupt priority level for the EOnCE Breakpoint Unit IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.8 EOnCE Step Counter Interrupt Priority Level (STPCNT IPL)— Bits 1–0

This field is used to set the interrupt priority level for the EOnCE Step Counter IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.5 Interrupt Priority Register 4 (IPR4)

Base + $4	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TMRA_3 IPL		TMRA_2 IPL		TMRA_1 IPL		TMRA_0 IPL		I2C_STAT IPL		I2C_TX IPL		I2C_RX IPL		I2C_GEN IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-7 Interrupt Priority Register 4 (IPR4)

5.6.5.1 Timer A, Channel 3 Interrupt Priority Level (TMRA_3 IPL)—Bits 15–14

This field is used to set the interrupt priority level for the Timer A, Channel 3 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.2 Timer A, Channel 2 Interrupt Priority Level (TMRA_2 IPL)—Bits 13–12

This field is used to set the interrupt priority level for the Timer A, Channel 2 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.3 Timer A, Channel 1 Interrupt Priority Level (TMRA_1 IPL)—Bits 11–10

This field is used to set the interrupt priority level for the Timer A, Channel 1 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

6.3.8 Peripheral Clock Rate Register (SIM_PCR)

By default, all peripherals are clocked at the system clock rate, which has a maximum of 32MHz. Selected peripherals clocks have the option to be clocked at 3X system clock rate, which has a maximum of 96MHz, if the PLL output clock is selected as the system clock. If PLL is disabled, the 3X system clock will not be available. This register is used to enable high-speed clocking for those peripherals that support it.

Note: Operation is unpredictable if peripheral clocks are reconfigured at runtime, so peripherals should be disabled before a peripheral clock is reconfigured.

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TMRB_CR	TMRA_CR	PWM_CR	I2C_CR	0	0	0	0	0	0	0	0	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-9 Peripheral Clock Rate Register (SIM_PCR)

6.3.8.1 Quad Timer B Clock Rate (TMRB_CR)—Bit 15

This bit selects the clock speed for the Quad Timer B module.

- 0 = Quad Timer B clock rate equals the system clock rate, to a maximum 32MHz (default)
- 1 = Quad Timer B clock rate equals 3X system clock rate, to a maximum 96MHz

6.3.8.2 Quad Timer A Clock Rate (TMRA_CR)—Bit 14

This bit selects the clock speed for the Quad Timer A module.

- 0 = Quad Timer A clock rate equals the system clock rate, to a maximum 32MHz (default)
- 1 = Quad Timer A clock rate equals 3X system clock rate, to a maximum 96MHz

6.3.8.3 Pulse Width Modulator Clock Rate (PWM_CR)—Bit 13

This bit selects the clock speed for the PWM module.

- 0 = PWM module clock rate equals the system clock rate, to a maximum 32MHz (default)
- 1 = PWM module clock rate equals 3X system clock rate, to a maximum 96MHz

6.3.8.4 Inter-Integrated Circuit Run Clock Rate (I2C_CR)—Bit 12

This bit selects the clock speed for the I^2C run clock.

- 0 = I^2C module run clock rate equals the system clock rate, to a maximum 32MHz (default)
- 1 = I^2C module run clock rate equals 3X system clock rate, to a maximum 96MHz

6.3.8.5 Reserved—Bits 11–0

This bit field is reserved. Each bit must be set to 0.

6.3.10.12 Quad Timer A, Channel 1 Clock Enable (TA1)—Bit 1

- 0 = The clock is not provided to the Timer A1 module (the Timer A1 module is disabled)
- 1 = The clock is enabled to the Timer A1 module

6.3.10.13 Quad Timer A, Channel 0 Clock Enable (TA0)—Bit 0

- 0 = The clock is not provided to the Timer A0 module (the Timer A0 module is disabled)
- 1 = The clock is enabled to the Timer A0 module

6.3.11 Stop Disable Register 0 (SD0)

By default, peripheral clocks are disabled during Stop mode in order to maximize power savings. This register will allow an individual peripheral to operate in Stop mode. Since asserting an interrupt causes the system to return to Run mode, this feature is provided so that selected peripherals can be left operating in Stop mode for the purpose of generating a wake-up interrupt.

For power-conscious applications, it is recommended that only a minimum set of peripherals be configured to remain operational during Stop mode.

Peripherals should be put in a non-operating (disabled) configuration prior to entering Stop mode unless their corresponding Stop Disable control is set to 1. Refer to the **56F802x and 56F803x Peripheral Reference Manual** for further details. Reads and writes cannot be made to a module that has its clock disabled.

Note: The MSCAN module supports extended power management capabilities including Sleep, Stop-in-Wait, and Disable modes. MSCAN clocks are selected by MSCAN control registers. For details, refer to the **56F802x and 56F803x Peripheral Reference Manual**.

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	CMPB_SD	CMPA_SD	DAC1_SD	DAC0_SD	0	ADC_SD	0	0	0	I2C_SD	QSCI1_SD	QSCI0_SD	QSPI1_SD	QSPI0_SD	0	PWM_SD
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-12 Stop Disable Register 0 (SD0)

6.3.11.1 Comparator B Clock Stop Disable (CMPB_SD)—Bit 15

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.2 Comparator A Clock Stop Disable (CMPA_SD)—Bit 14

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.20.2 Configure GPIOD5 (GPS_D5)—Bit 12

This field selects the alternate function for GPIOD5.

- 0 = XTAL - External Crystal Oscillator Output (default)
- 1 = CLKIN - External Clock Input

6.3.20.3 Reserved—Bits 11–5

This bit field is reserved. Each bit must be set to 0.

6.3.20.4 Configure GPIOC12 (GPS_C12)—Bit 4

This field selects the alternate function for GPIOC12.

- 0 = ANB4 - ADCB, Channel 4 (default)
- 1 = RXD1 - QSCI1 Receive Data

6.3.20.5 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

6.3.20.6 Configure GPIOC8 (GPS_C8)—Bit 2

This field selects the alternate function for GPIOC8.

- 0 = ANA4 - ADCA, Channel 4 (default)
- 1 = TXD1 - QSCI1 Transmit Data

6.3.20.7 Reserved—Bits 1—0

This bit field is reserved. Each bit must be set to 0.

6.3.21 Internal Peripheral Source Select Register 0 for Pulse Width Modulator (SIM_IPS0)

The internal integration of peripherals provides input signal source selection for peripherals where an input signal to a peripheral can be fed from one of several sources. These registers are organized by peripheral type and provide a selection list for every peripheral input signal that has more than one alternative source to indicate which source is selected.

If one of the alternative sources is GPIO, the setting in these registers must be made consistently with the settings in the GPS*n* and GPIO*x*_PEREN registers. Specifically, when an IPS*n* field is configured to select an I/O pin as the source, then GPS*n* register settings must configure only one I/O pin to feed this peripheral input function. Also, the GPIO*x*_PEREN bit for that I/O pin must be set to 1 to enable peripheral control of the I/O.

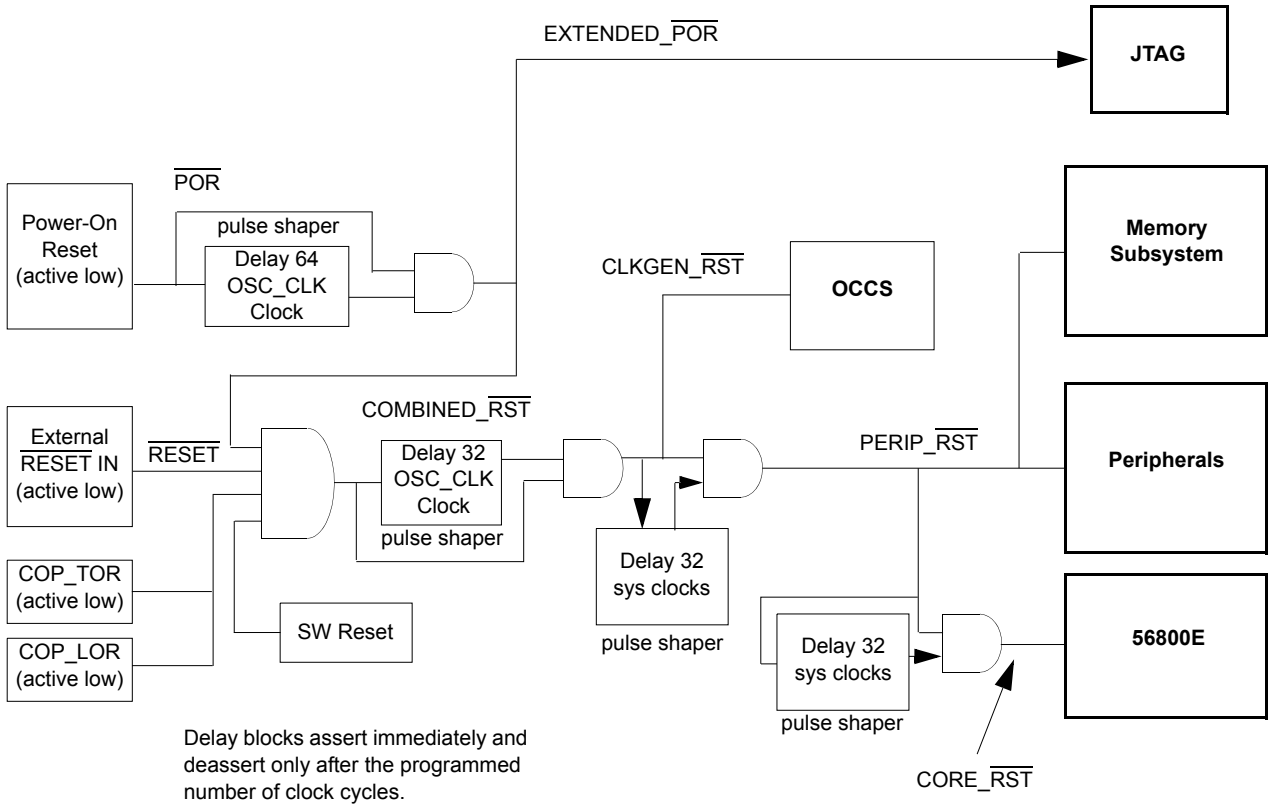

Figure 6-28 Sources of RESET Functional Diagram (Test modes not included)

POR resets are extended 64 OSC_CLK clocks to stabilize the power supply and clock source. All resets are subsequently extended for an additional 32 OSC_CLK clocks and 64 system clocks as the various internal reset controls are released. Given the normal relaxation oscillator rate of 8MHz, the duration of a POR reset from when power comes on to when code is running is 28µS. An external reset generation circuit may also be used. A description of how these resets are used to initialize the clocking system and system modules is included in **Section 6.7**.

6.7 Clocks

The memory, peripheral and core clocks all operate at the same frequency (32MHz maximum) with the exception of the peripheral clocks for quad timers TMRA and TMRB and the PWM, which have the option to operate at 3X system clock. The SIM is responsible for clock distributions.

While the SIM generates the ADC peripheral clock in the same way it generates all other peripheral clocks, the ADC standby and conversion clocks are generated by a direct interface between the ADC and the OCCS module.

program execution is otherwise unaffected.

7.2 Flash Access Lock and Unlock Mechanisms

There are several methods that effectively lock or unlock the on-chip flash.

7.2.1 Disabling EOnCE Access

On-chip flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E CPU. The TCK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port) is active and provides the chip's boundary scan capability and access to the ID register, but proper implementation of flash security will block any attempt to access the internal flash memory via the EOnCE port when security is enabled.

7.2.2 Flash Lockout Recovery Using JTAG

If the device is secured, one lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared). This does not compromise security, as the entire contents of the user's secured code stored in flash are erased before security is disabled on the device on the next reset or power-up sequence.

To start the lockout recovery sequence via JTAG, the JTAG public instruction (LOCKOUT_RECOVERY) must first be shifted into the chip-level TAP controller's instruction register. Once the LOCKOUT_RECOVERY instruction has been shifted into the instruction register, the clock divider value must be shifted into the corresponding 7-bit data register. After the data register has been updated, the user must transition the TAP controller into the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence is complete. Refer to the **56F802x and 56F803x Peripheral Reference Manual** for more details, or contact Freescale.

Note: Once the lockout recovery sequence has completed, the user must reset both the JTAG-TAP controller and device to return to normal unsecured operation. Power-on reset will reset both too.

7.2.3 Flash Lockout Recovery using CodeWarrior

CodeWarrior can unlock a device by selecting the *Debug* menu, then selecting *DSP56800E*, followed by *Unlock Flash*. Another mechanism is also built into CodeWarrior using the device's memory configuration file. The command "*Unlock_Flash_on_Connect 1*" in the *.cfg* file accomplishes the same task as using the *Debug* menu.

This lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared).

7.2.4 Flash Lockout Recovery without mass erase

A user can un-secure a secured device by programming the word $0000 into program memory location $00 7FF7. After completing the programming, both the JTAG TAP controller and the device must be reset in order to return to normal unsecured operation. Power-on reset will also reset both.

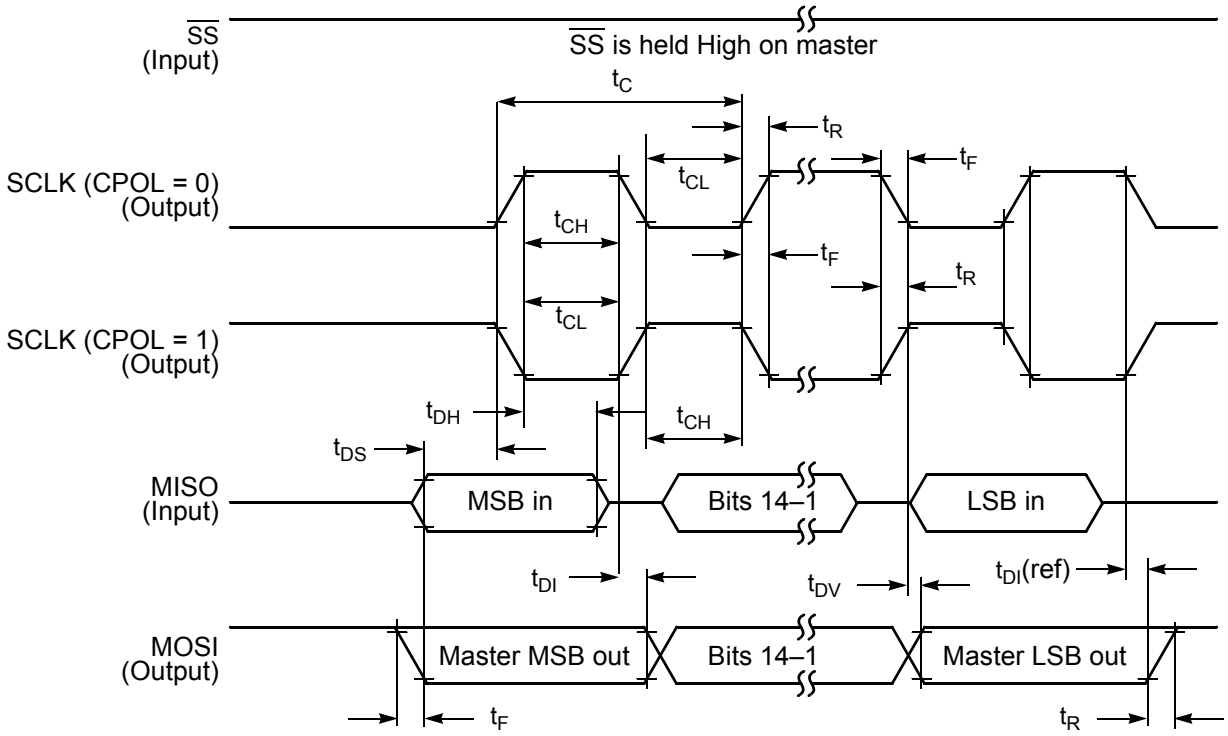

Figure 10-7 SPI Master Timing (CPHA = 0)

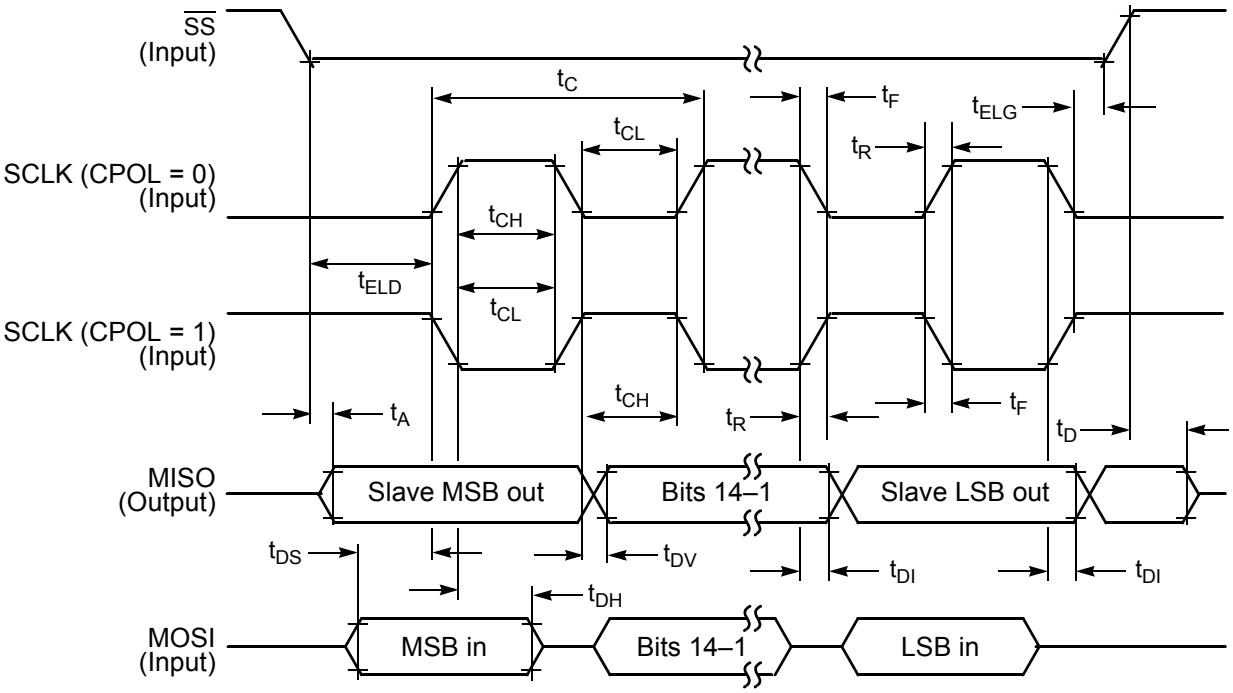

Figure 10-9 SPI Slave Timing (CPHA = 0)

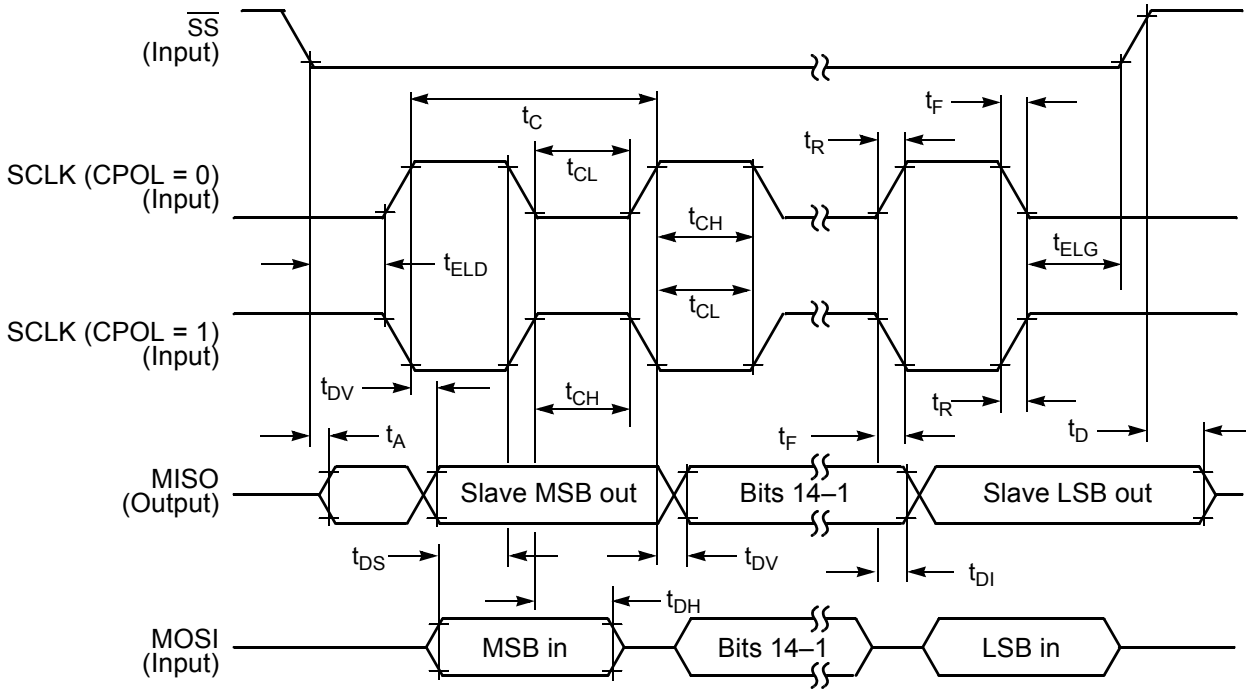

Figure 10-10 SPI Slave Timing (CPHA = 1)

10.10 Quad Timer Timing

Table 10-15 Timer Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	10-11
Timer input high / low period	P_{INHL}	1T + 3	—	ns	10-11
Timer output period	P_{OUT}	125	—	ns	10-11
Timer output high / low period	P_{OUTHL}	50	—	ns	10-11

1. In the formulas listed, T = the clock cycle. For 32MHz operation, T = 31.25ns.
2. Parameters listed are guaranteed by design.

10.14 JTAG Timing

Table 10-19 JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation[1]	f_{OP}	DC	SYS_CLK/8	MHz	10-16
TCK clock pulse width	t_{PW}	50	—	ns	10-16
TMS, TDI data set-up time	t_{DS}	5	—	ns	10-17
TMS, TDI data hold time	t_{DH}	5	—	ns	10-17
TCK low to TDO data valid	t_{DV}	—	30	ns	10-17
TCK low to TDO tri-state	t_{TS}	—	30	ns	10-17

1. TCK frequency of operation must be less than 1/8 the processor rate.

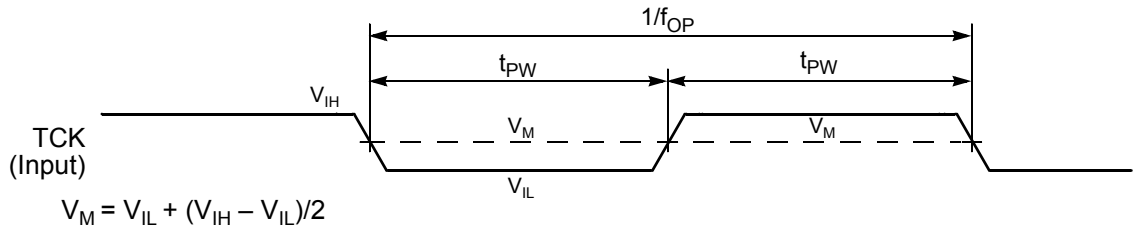

Figure 10-16 Test Clock Input Timing Diagram

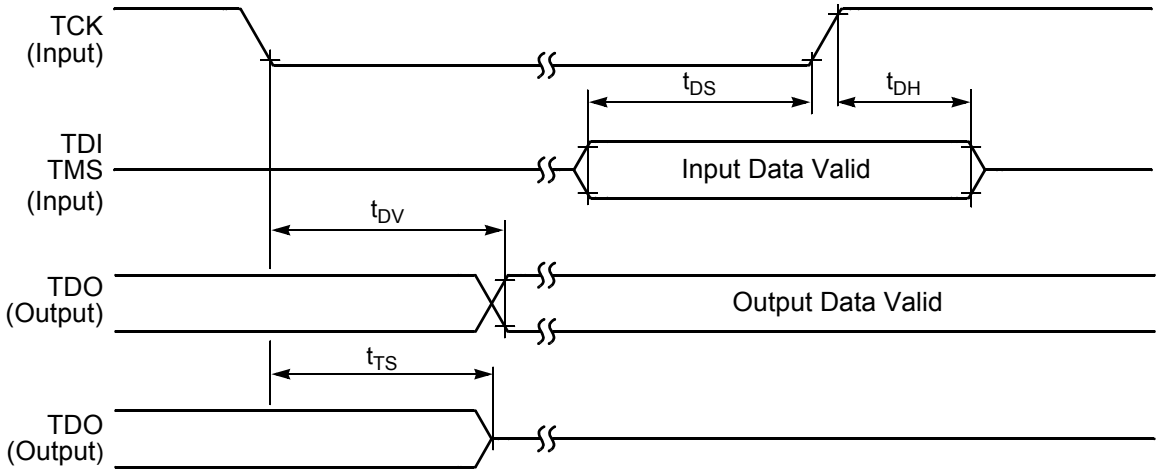

Figure 10-17 Test Access Port Timing Diagram

10.19 Power Consumption

See Section 10.1 for a list of IDD requirements for the 56F8037/56F8027. This section provides additional detail which can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static component]
+B: internal [state-dependent component]
+C: internal [dynamic component]
+D: external [dynamic component]
+E: external [static component]

A, the internal [static component], is comprised of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent component], reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, Flash memory and the ADCs.

C, the internal [dynamic component], is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic component], reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 10-23 I/O Loading Coefficients at 10MHz

	Intercept	Slope
8mA drive	1.3	0.11mW / pF
4mA drive	1.15mW	0.11mW / pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. Table 10-23 provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases:

$$TotalPower = \Sigma((\text{Intercept} + \text{Slope}*\text{Cload})*\text{frequency}/10\text{MHz})$$

where:

- Summation is performed over all output pins with capacitive loads
- TotalPower is expressed in mW
- Cload is expressed in pF

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Pulse Width Modulator (PWM) Module							
Control Register	CTRL	PMCTL	PWM_CTRL	PWM_PMCTL	PWM_PMCTL	0xF0C0	
Fault Control Register	FCTRL	PMFCTL	PWM_FCTRL	PWM_PMFCTL	PWM_PMFCTL	0xF0C1	
Fault Status/Acknowledge Regis.	FLTACK	PMFSA	PWM_FLTACK	PWM_PMFSA	PWM_PMFSA	0xF0C2	
Output Control Register	OUT	PMOUT	PWM_OUT	PWM_PMOUT	PWM_PMOUT	0xF0C3	
Counter Register	CNTR	PMCNT	PWM_CNTR	PWM_PMCNT	PWM_PMCNT	0xF0C4	
Counter Modulo Register	CMOD	MCM	PWM_CMOD	PWM_MCM	PWM_MCM	0xF0C5	
Value 0-5 Registers	VAL0-5	PMVAL0-5	PWM_VAL0-5	PWM_PMVAL0-5	PWM_PMVAL0-5	0xF0C6	0xF0CB
Deadtime 0-1 Registers	DTIM0-1	PMDEADTM0-1	PWM_DTIM0-1	PWM_PMDEADTM0-1	PWM_PMDEADTM0-1	0xF0CC	0xF0CD
Disable Mapping 1-2 Registers	DMAP1-2	PMDISMAP1-2	PWM_DMAP1-2	PWM_PMDISMAP1-2	PWM_PMDISMAP1-2	0xF0CE	0xF0CF
Configure Register	CNFG	PMCFG	PWM_CNFG	PWM_PMCFG	PWM_PMCFG	0xF0D0	
Channel Control Register	CCTRL	PMCCR	PWM_CCTRL	PWM_PMCCR	PWM_PMCCR	0xF0D1	
Port Register	PORT	PMPORT	PWM_PORT	PWM_PMPORT	PWM_PMPORT	0xF0D2	
Internal Correction Control Register	ICCTRL	PMICCR	PWM_ICCTRL	PWM_PMICCR	PWM_PMICCR	0xF0D3	
Source Control Register	SCTRL	PMSRC	PWM_SCTRL	PWM_PMSRC	PWM_PMSRC	0xF0D4	
Synchronization Window Register	SYNC		PWM_SYNC	PWM_SYNC	PWM_SYNC	0xF0D5	
Fault Filter 0-3 Register	FFILT0-3		PWM_FFILT0-3	PWM_FFILT0-3	PWM_FFILT0-3	0xF0D6	0xF0D9
Multi-Scalable Controller Area Network (MSCAN) Module							
Control 0 Register	CTRL0		CAN_CTRL0		CANCTRL0	0XF800	
Control 1 Register	CTRL1		CAN_CTRL1		CANCTRL1	0XF801	
Bus Timing 0 Register	BTR0		CAN_BTR0		CANBTR0	0XF802	
Bus Timing 1 Register	BTR1		CAN_BTR1		CANBTR1	0XF803	
Receive Flag Register	RFLG		CAN_RFLG		CANRFLG	0XF804	
Receiver Interrupt Enable Register	RIER		CAN_RIER		CANRIER	0XF805	
Transmitter Flag Register	TFLG		CAN_TFLG		CANTFLG	0XF806	
Transmitter Interrupt Enable Register.	TIER		CAN_TIER		CANTIER	0XF807	
Transmitter Msg Abort Request Register	TARQ		CAN_TARQ		CANTARQ	0XF808	

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Transmitter Message Abort Acknowledge Register	TAAK		CAN_TAAK		CANTAAK	0XF809	
Transmitter FIFO Selection Register	TBSEL		CAN_TBSEL		CANTBSEL	0XF80A	
Identifier Acceptance Control Register	IDAC		CAN_IDAC		CANIDAC	0XF80B	
Miscellaneous Register	MISC		CAN_MISC		CANMISC	0XF80D	
Receive Error Register	RXERR		CAN_RXERR		CANRXERR	0XF80E	
Transmit Error Register	TXERR		CAN_TXERR		CANTXERR	0XF80F	
Identifier Acceptance 0-3 Registers	IDAR0-3		CAN_IDAR0-3		CANIDAR0-3	0xF810	0xF813
Identifier Mask 0-3 Registers	IDMR0-3		CAN_IDMR0-3		CANIDMR0-3	0xF814	0xF817
Identifier Acceptance 4-7 Register	IDAR4-7		CAN_IDAR4-7		CANIDAR4-7	0xF818	0xF81B
Identifier Mask 4-7 Registers	IDMR4-7		CAN_IDMR4-7		CANIDMR4-7	0xF81C	0xF81F
Foreground Receive FIFO Register	RXFG		CAN_RXFG		CANRXFG	0xF82F	0xF820
Foreground Transmit FIFO Register	TXFG		CAN_TXFG		CANTXFG	0xF830	0xF83F
Power Supervisor (PS) Module							
Control Register	CTRL	LVICONTROL	PS_CTRL	LVICONTROL	LVICTRL	0xF140	
Status Register	STAT	LVISTATUS	PS_STAT	LVISTATUS	LVISR	0xF141	
Queued Serial Communications Interface (QSCI) Module							
					n=0, 1		
Baud Rate Register	RATE		QSCI_RATE		QSCI_SCIBR	0xF2***n***0	
Control 1 Register	CTRL1		QSCI_CTRL1		QSCI_SCICR	0xF2***n***1	
Control 2 Register	CTRL2		QSCI_CTRL2		QSCI_SCICR2	0xF2***n***2	
Status Register	STAT		QSCI_STAT		QSCI_SCISR	0xF2***n***3	
Data Register	DATA		QSCI_DATA		QSCI_SCIDR	0xF2***n***4	
Queued Serial Peripheral Interface (QSPI) Module							
Status and Control Register	SCTRL		QSPI_SCTRL		QSPI_SPSCR	0xF2***n***0	
Data Size and Control Register	DSCTRL		QSPI_DSCTRL		QSPI_SPDSR	0xF2***n***1	
Data Receive Register	DRCV		QSPI_DRCV		QSPI_SPDRR	0xF2***n***2	
Data Transmit Register	DXMIT		QSPI_DXMIT		QSPI_SPDTR	0xF2***n***3	