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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8027vlhr

configuration flexibility, and compact program code, the 56F8037/56F8027 is well-suited for many applications. The 56F8037/56F8027 includes many peripherals that are especially useful for industrial control, motion control, home appliances, general purpose inverters, smart sensors, fire and security systems, switched-mode power supply, power management, and medical monitoring applications.

The 56800E core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The 56F8037/56F8027 supports program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. The 56F8037/56F8027 also offers up to 53 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F8037 Digital Signal Controller includes 64KB of Program Flash and 8KB of Unified Data/Program RAM. The 56F8027 Digital Signal Controller includes 32KB of Program Flash and 4KB of Unified Data/Program RAM. Program Flash memory can be independently bulk erased or erased in pages. Program Flash page erase size is 512 Bytes (256 Words).

A full set of programmable peripherals—PWM, ADCs, QSCIs, QSPIs, I2C, PITs, Quad Timers, DACs and analog comparators—supports various applications. Each peripheral can be independently shut down to save power. Any pin in these peripherals can also be used as General Purpose Input/Outputs (GPIOs).

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Architecture Block Diagram

The 56F8037/56F8027's architecture is shown in **Figures 1-1**, **1-2**, **1-3**, **1-4**, **1-5**, **1-6**, and **1-7**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories and the IPBus Bridge and the internal connections between each unit of the 56800E core. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. **Figures 1-3**, **1-4**, **1-5**, **1-6** and **1-7** detail how the device's I/O pins are muxed. The figures do not show the on-board regulator and power and ground signals. Please see **Part 2, Signal/Connection Descriptions**, for information about which signals are multiplexed with those of other peripherals.

1.4.1 PWM, TMR and ADC Connections

Figure 1-6 shows the over-limit and under-limit connections from the ADC to the PWM and the

connections to the PWM from the TMR and GPIO. These signals can control the PWM outputs in a similar manner as the PWM generator. See the **56F802x and 56F803x Peripheral Reference Manual** for additional information.

The PWM_reload_sync output can be connected to Timer A's (TMRA) Channel 3 input; TMRA's Channels 2 and 3 outputs are connected to the ADC sync inputs. TMRA Channel 3 output is connected to SYNC0 and TMRA Channel 2 is connected to SYNC1. SYNC0 is the master ADC sync input that is used to trigger ADCA and ADCB in sequence and parallel mode. SYNC1 is used to trigger ADCB in parallel independent mode. These are controlled by bits in the SIM Control Register; see **Section 6.3.1**.

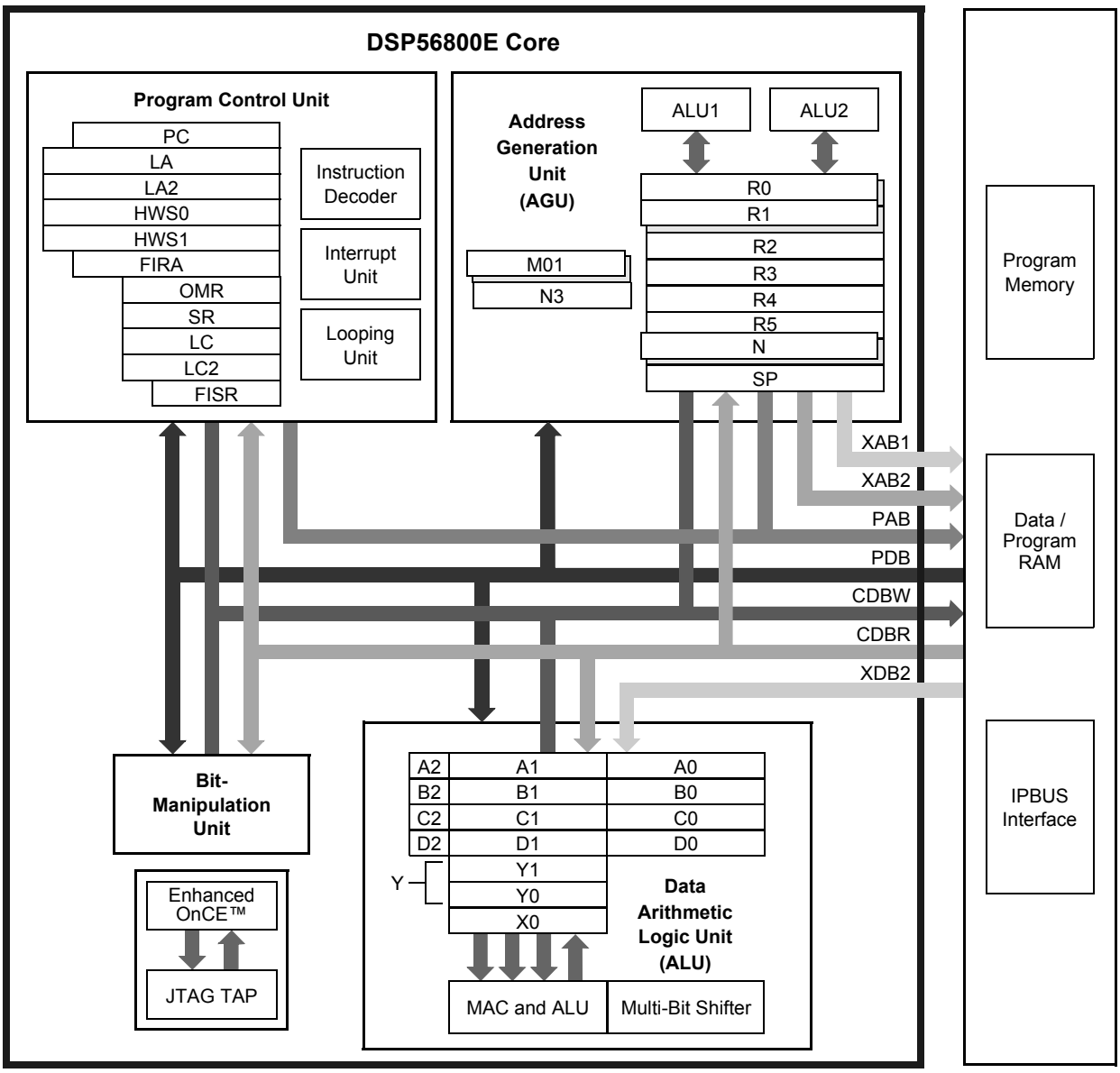

Figure 1-1 56800E Core Block Diagram

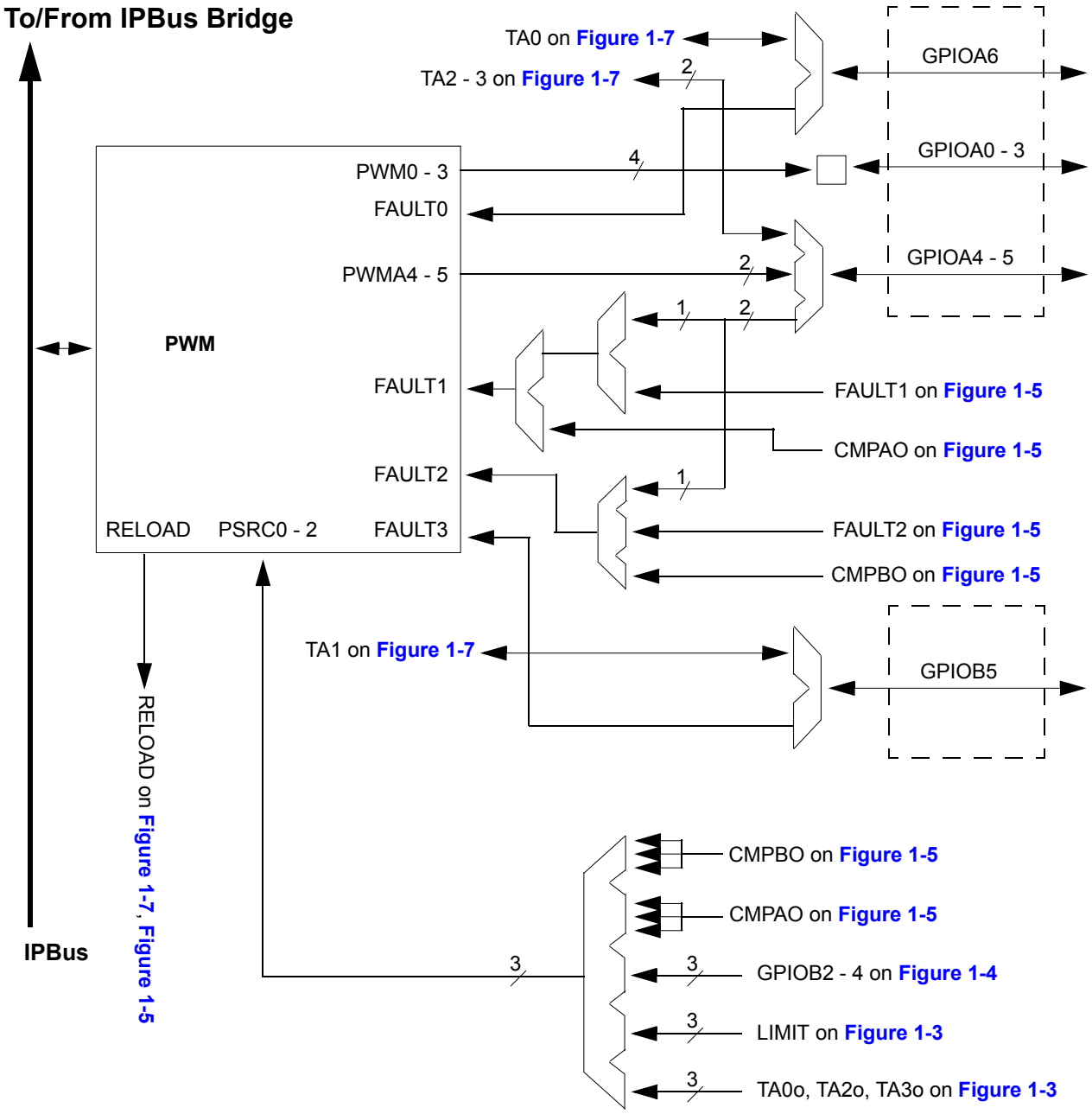

Figure 1-6 56F8037/56F8027 I/O Pin-Out Muxing (Part 4/5)

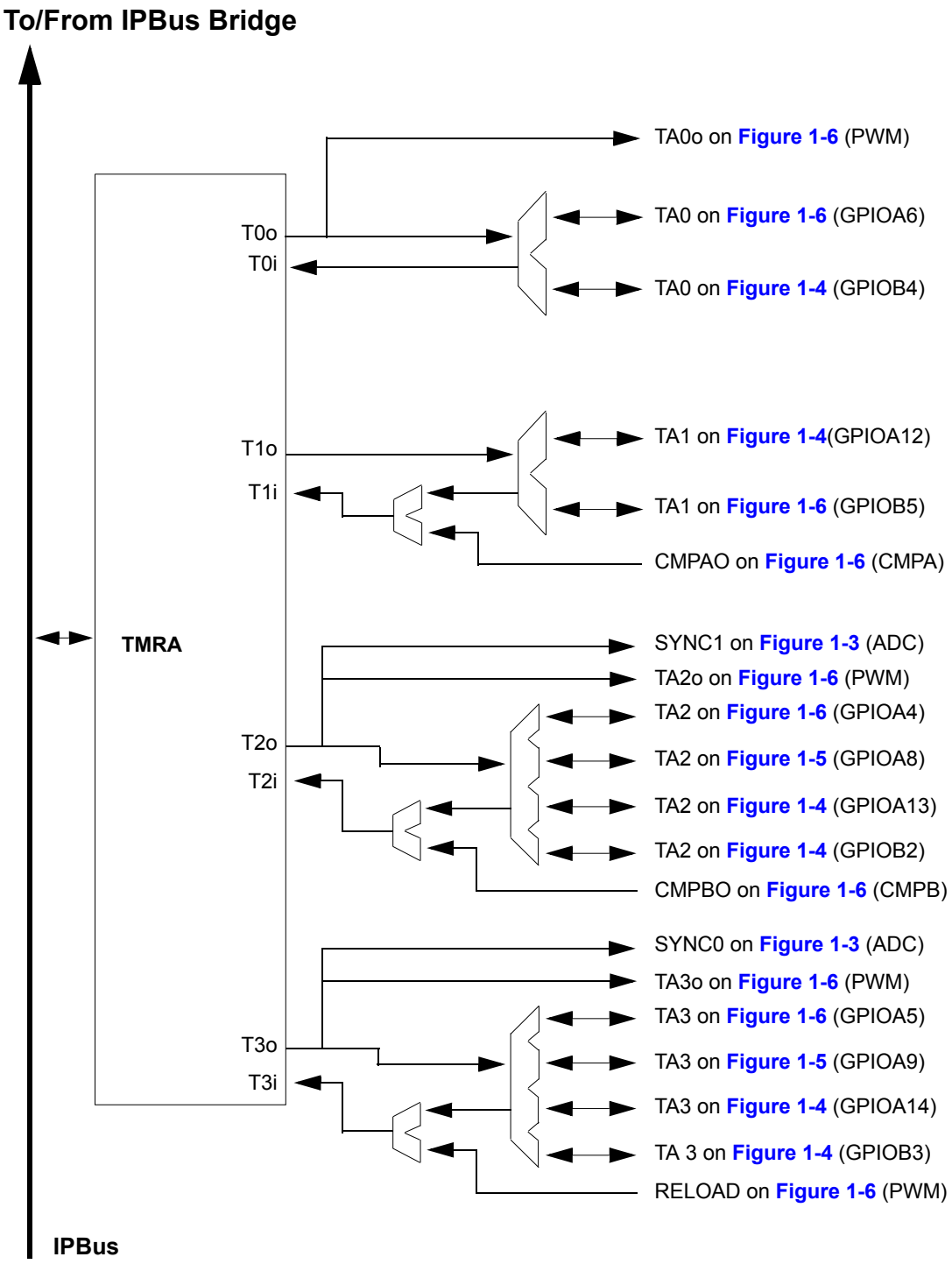

Figure 1-7 56F8037/56F8027 I/O Pin-Out Muxing (Part 5/5)

2.2 56F8037/56F8027 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed.

Table 2-3 56F8037/56F8027 Signal and Package Information for the 64-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
V_{DD}	7	Supply	Supply	**I/O Power** — This pin supplies 3.3V power to the chip I/O interface.
V_{DD}	41			
V_{DD}	50			
V_{SS}	8	Supply	Supply	V_{SS} — These pins provide ground for chip logic and I/O drivers.
V_{SS}	27			
V_{SS}	40			
V_{SS}	51			
V_{DDA}	16	Supply	Supply	**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
V_{SSA}	17	Supply	Supply	**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
V_{CAP}	28	Supply	Supply	V_{CAP} — Connect this pin to a 2.2µF or greater bypass capacitor in order to bypass the core voltage regulator, required for proper chip operation. See Section 10.2.1.
V_{CAP}	49			
$\overline{\text{RESET}}$ (GPIOA7)	31	Input Input/Open Drain Output	Input, internal pull-up enabled	**Reset** — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the chip is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. The internal reset signal will be deasserted synchronous with the internal clocks after a fixed number of internal clocks. **Port A GPIO** — This GPIO pin can be individually programmed as an input or open drain output pin. Note that $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can only be reset via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.

Return to Table 2-2

Table 4-8 Data Memory Peripheral Base Address Map Summary (Continued)

Peripheral	Prefix	Base Address	Table Number
DAC 0	DAC0	X:$00 F1C0	4-25
DAC 1	DAC1	X:$00 F1D0	4-26
Comparator A	CMPA	X:$00 F1E0	4-27
Comparator B	CMPB	X:$00 F1F0	4-28
QSCI 0	QSCI0	X:$00 F200	4-29
QSCI 1	QSCI1	X:$00 F210	4-30
QSPI 0	QSPI0	X:$00 F220	4-31
QSPI 1	QSPI1	X:$00 F230	4-32
I^2C	I2C	X:$00 F280	4-33
FM	FM	X:$00 F400	4-34
MSCAN	CAN	X:$00 F800	4-35

Table 4-12 Pulse Width Modulator Registers Address Map (Continued) (PWM_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
PWM_DTIM1	$D	Dead Time Register 1
PWM_DMAP1	$E	Disable Mapping Register 1
PWM_DMAP2	$F	Disable Mapping Register 2
PWM_CNFG	$10	Configure Register
PWM_CCTRL	$11	Channel Control Register
PWM_PORT	$12	Port Register
PWM_ICCTRL	$13	Internal Correction Control Register
PWM_SCTRL	$14	Source Control Register
PWM_SYNC	$15	Synchronization Window Register
PWM_FFILT0	$16	Fault0 Filter Register
PWM_FFILT1	$17	Fault1 Filter Register
PWM_FFILT2	$18	Fault2 Filter Register
PWM_FFILT3	$19	Fault3 Filter Register

Table 4-13 Interrupt Control Registers Address Map (ITCN_BASE = $00 F0E0)

Register Acronym	Address Offset	Register Description
ITCN_IPR0	$0	Interrupt Priority Register 0
ITCN_IPR1	$1	Interrupt Priority Register 1
ITCN_IPR2	$2	Interrupt Priority Register 2
ITCN_IPR3	$3	Interrupt Priority Register 3
ITCN_IPR4	$4	Interrupt Priority Register 4
ITCN_IPR5	$5	Interrupt Priority Register 5
ITCN_IPR6	$6	Interrupt Priority Register 6
ITCN_VBA	$7	Vector Base Address Register
ITCN_FIM0	$8	Fast Interrupt Match 0 Register
ITCN_FIVAL0	$9	Fast Interrupt Vector Address Low 0 Register
ITCN_FIVAH0	$A	Fast Interrupt Vector Address High 0 Register
ITCN_FIM1	$B	Fast Interrupt Match 1 Register
ITCN_FIVAL1	$C	Fast Interrupt Vector Address Low 1 Register
ITCN_FIVAH1	$D	Fast Interrupt Vector Address High 1 Register
ITCN_IRQP0	$E	IRQ Pending Register 0
ITCN_IRQP1	$F	IRQ Pending Register 1
ITCN_IRQP2	$10	IRQ Pending Register 2

5.3.1 Normal Interrupt Handling

Once the INTC has determined that an interrupt is to be serviced and which interrupt has the highest priority, an interrupt vector address is generated. Normal interrupt handling concatenates the Vector Base Address (VBA) and the vector number to determine the vector address, generating an offset into the vector table for each interrupt.

5.3.2 Interrupt Nesting

Interrupt exceptions may be nested to allow an IRQ of higher priority than the current exception to be serviced. The 56800E core controls the masking of interrupt priority levels it will accept by setting the I0 and I1 bits in its status register.

Table 5-1 Interrupt Mask Bit Definition

SR[9] (I1)	SR[8] (I0)	Exceptions Permitted	Exceptions Masked
0	0	Priorities 0, 1, 2, 3	None
0	1	Priorities 1, 2, 3	Priority 0
1	0	Priorities 2, 3	Priorities 0, 1
1	1	Priority 3	Priorities 0, 1, 2

The IPIC bits of the ICTRL register reflect the state of the priority level being presented to the 56800E core.

Table 5-2 Interrupt Priority Encoding

IPIC_VALUE[1:0]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No interrupt or SWILP	Priorities 0, 1, 2, 3
01	Priority 0	Priorities 1, 2, 3
10	Priority 1	Priorities 2, 3
11	Priority 2 or 3	Priority 3

5.3.3 Fast Interrupt Handling

Fast interrupts are described in the **DSP56800E Reference Manual**. The interrupt controller recognizes Fast Interrupts before the core does.

A Fast Interrupt is defined (to the ITCN) by:

1. Setting the priority of the interrupt as level 2, with the appropriate field in the IPR registers
2. Setting the FIM*n* register to the appropriate vector number

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	IPR0	R	PLL IPL		LVI IPL		0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL		BKPT_U IPL		STPCNT IPL	
		W																
$1	IPR1	R	GPIOD IPL		MSCAN_WKUP IPL		MSCAN_TX IPL		MSCAN_RX IPL		MSCAN_ERR IPL		FM_CBE IPL		FM_CC IPL		FM_ERR IPL	
		W																
$2	IPR2	R	QSCI0_XMIT IPL		QSPI1_XMIT IPL		QSPI1_RCV IPL		QSPI0_XMIT IPL		QSPI0_RCV IPL		GPIOA IPL		GPIOB IPL		GPIOC IPL	
		W																
$3	IPR3	R	I2C_ERR IPL		QSCI1_RCV IPL		QSCI1_RERR IPL		QSCI1_TIDL IPL		QSCI1_XMIT IPL		QSCI0_RCV IPL		QSCI0_RERR IPL		QSCI0_TIDL IPL	
		W																
$4	IPR4	R	TMRA_3 IPL		TMRA_2 IPL		TMRA_1 IPL		TMRA_0 IPL		I2C_STAT IPL		I2C_TX IPL		I2C_RX IPL		I2C_GEN IPL	
		W																
$5	IPR5	R	PIT1 IPL		PIT0 IPL		COMPB IPL		COMPA IPL		TMRB_3 IPL		TMRB_2 IPL		TMRB_1 IPL		TMRB_0 IPL	
		W																
$6	IPR6		0	0	0	0	PWM_F IPL		PWM_RL IPL		ADC_ZC IPL		ADCB_CC IPL		ADCA_CC IPL		PIT2 IPL	
$7	VBA	R	0	0	VECTOR_BASE_ADDRESS													
		W																
$8	FIM0	R	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0					
		W																
$9	FIVAL0	R	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
		W																
$A	FIVAH0	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
		W																
$B	FIM1	R	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1					
		W																
$C	FIVAL1	R	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
		W																
$D	FIVAH1	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
		W																
$E	IRQP0	R	PENDING[16:2]															1
		W																
$F	IRQP1	R	PENDING[32:17]															
		W																
$10	IRQP2	R	PENDING[48:33]															
		W																
$11	IRQP3	R	PENDING[63:49]															
		W																
	Reserved																	
$16	ICTRL	R	INT	IPIC			VAB						INT_DIS	1	1	1	0	0
		W																
	Reserved																	

= Reserved

Figure 5-2 ITCN Register Map Summary

- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6 Interrupt Priority Register 5 (IPR5)

Base + $5	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	PIT1 IPL		PIT0 IPL		COMPB IPL		COMPA IPL		TMRB_3 IPL		TMRB_2 IPL		TMRB_1 IPL		TMRB_0 IPL	
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-8 Interrupt Priority Register 5 (IPR6)

5.6.6.1 Programmable Interval Timer 1 Interrupt Priority Level (PIT1 IPL)—Bits 15–14

This field is used to set the interrupt priority level for the Programmable Interval Timer 1 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.2 Programmable Interval Timer 0 Interrupt Priority Level (PIT0 IPL)—Bits 13–12

This field is used to set the interrupt priority level for the Programmable Interval Timer 0 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.3 Comparator B Interrupt Priority Level (COMPB IPL)—Bits 11–10

This field is used to set the interrupt priority level for the Comparator B IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.5 ADC B Conversion Complete Interrupt Priority Level (ADCB_CC IPL)—Bits 5–4

This field is used to set the interrupt priority level for the ADC B Conversion Complete IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.6 ADC A Conversion Complete Interrupt Priority Level (ADCA_CC IPL)—Bits 3–2

This field is used to set the interrupt priority level for the ADC A Conversion Complete IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.7 Programmable Interval Timer 2 Interrupt Priority Level (PIT2 IPL)—Bits 1–0

This field is used to set the interrupt priority level for the Programmable Interval Timer 2 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8 Vector Base Address Register (VBA)

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	VECTOR_BASE_ADDRESS													
Write																
RESET[1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1. The 56F8037 resets to a value of 0x0000. This corresponds to reset addresses of 0x000000.
The 56F8027 resets to a value of 0x0080. This corresponds to reset addresses of 0x004000.

Figure 5-10 Vector Base Address Register (VBA)

5.6.8.1 Reserved—Bits 15–14

This bit field is reserved. Each bit must be set to 0.

- 000 = I/O pin (External) - Use a PSRC0 input pin as PWM source (default)
- 001 = TA0 (Internal) - Use Timer A0 output as PWM source
- 010 = ADC SAMPLE0 (Internal) - Use ADC SAMPLE0 result as PWM source
  - If the ADC conversion result in SAMPLE0 is greater than the value programmed into the High Limit register HLMT0, then PWM0 is set to 0 and PWM1 is set to 1
  - If the ADC conversion result in SAMPLE0 is less than the value programmed into the Low Limit register LLMT0, then PWM0 is set to 1 and PWM1 is set to 0
- 011 = CMPAO (Internal) - Use Comparator A output as PWM source
- 100 = CMPBO (Internal) - Use Comparator B output as PWM source
- 11x = Reserved
- 1x1 = Reserved

6.3.22 Internal Peripheral Source Select Register 1 for Digital-to-Analog Converters (SIM_IPS1)

See **Section 6.3.21** for general information about Internal Peripheral Source Select registers.

Base + $19	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	IPS1_DSYNC1			0	IPS1_DSYNC0		
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-26 Internal Peripheral Source Select Register for DACs (SIM_IPS1)

6.3.22.1 Reserved—Bits 15–7

This bit field is reserved. Each bit must be set to 0.

6.3.22.2 Select Input Peripheral Source for SYNC Input to DAC 1 (IPS1_DSYNC1)—Bits 6–4

This field selects the alternate input source signal to feed DAC1 SYNC input.

- 000 = PIT0 (Internal) - Use Programmable Interval Timer 0 Output as DAC SYNC input (default)
- 001 = PIT1 (Internal) - Use Programmable Interval Timer 1 Output as DAC SYNC input
- 010 = PIT2 (Internal) - Use Programmable Interval Timer 2 Output as DAC SYNC input
- 011 = PWM SYNC (Internal) - Use PWM reload synchronization signal as DAC SYNC input
- 100 = TA0 (Internal) - Use Timer A0 output as DAC SYNC input
- 101 = TA1 (Internal) - Use Timer A1 output as DAC SYNC input
- 11x = Reserved

6.3.22.3 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

6.3.22.4 Select Peripheral Input Source for SYNC Input to DAC 0 (IPS1_DSYNC0)—Bits 2–0

This field selects the alternate input source signal to feed DAC0 SYNC input.

- 000 = PIT0 (Internal) - Use Programmable Interval Timer 0 Output as DAC SYNC input (default)
- 001 = PIT1 (Internal) - Use Programmable Interval Timer 1 Output as DAC SYNC input
- 010 = PIT2 (Internal) - Use Programmable Interval Timer 2 Output as DAC SYNC input
- 011 = PWM SYNC (Internal) - Use PWM reload synchronization signal as DAC SYNC input
- 100 = TA0 (Internal) - Use Timer A0 output as DAC SYNC input
- 101 = TA1 (Internal) - Use Timer A1 output as DAC SYNC input
- 11x = Reserved

6.3.23 Internal Peripheral Source Select Register 2 for Quad Timer A (SIM_IPS2)

See **Section 6.3.21** for general information about Internal Peripheral Source Select registers.

Base + $1A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	IPS2_ TA3	0	0	0	IPS2_ TA2	0	0	0	IPS2_ TA1	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-27 Internal Peripheral Source Select Register for TMRA (SIM_IPS2)

6.3.23.1 Reserved—Bits 15–13

This bit field is reserved. Each bit must be set to 0.

6.3.23.2 Select Peripheral Input Source for TA3 (IPS2_TA3)—Bit 12

This field selects the alternate input source signal to feed Quad Timer A, input 3.

- 0 = I/O pin (External) - Use Timer A3 input/output pin
- 1 = PWM SYNC (Internal) - Use PWM reload synchronization signal

6.3.23.3 Reserved—Bits 11–9

This bit field is reserved. Each bit must be set to 0.

6.3.23.4 Select Peripheral Input Source for TA2 (IPS2_TA2)—Bit 8

This field selects the alternate input source signal to feed Quad Timer A, input 2.

- 0 = I/O pin (External) - Use Timer A2 input/output pin
- 1 = CMPBO (Internal) - Use Comparator B output

possible to invoke Stop or Wait mode while in Standby mode for even greater levels of power reduction. A 400kHz external clock can optionally be used in Standby mode to produce the required Standby 200kHz system clock rate. Power-down mode, which selects the ROSC clock source but shuts it off, fully disables the device and minimizes its power utilization but is only recoverable via reset.

When the PLL is not selected and the system bus is operating at 200kHz or less, the large regulator can be put into its Standby mode (LRSTDBY) to reduce the power utilization of that regulator.

All peripherals, except the COP/watchdog timer, run at the system clock frequency or optional 3X system clock for PWM, Timers, and I^2C. The COP timer runs at OSC_CLK / 1024. The maximum frequency of operation is 32MHz.

6.6 Resets

The SIM supports five sources of reset, as shown in **Figure 6-28**. The two asynchronous sources are the external reset pin and the Power-On Reset (POR). The three synchronous sources are the software reset (SW reset), which is generated within the SIM itself by writing the SIM_CTRL register in **Section 6.3.1**, the COP time-out reset (COP_TOR), and the COP loss-of-reference reset (COP_LOR). The reset generation module has three reset detectors, which resolve into four primary resets. These are outlined in **Table 6-3**. The JTAG circuitry is reset by the Power-On Reset.

Table 6-3 Primary System Resets

	Reset Sources				
Reset Signal	**POR**	**External**	**Software**	**COP**	**Comments**
EXTENDED_$\overline{\text{POR}}$	X				Stretched version of $\overline{\text{POR}}$ released 64 OSC_CLK cycles after $\overline{\text{POR}}$ deasserts
CLKGEN_$\overline{\text{RST}}$	X	X	X	X	Released 32 OSC_CLK cycles after all reset sources, including EXTENDED_$\overline{\text{POR}}$, have released
PERIP_$\overline{\text{RST}}$	X	X	X	X	Releases 32 SYS_CLK cycles after the CLKGEN_$\overline{\text{RST}}$ is released
CORE_$\overline{\text{RST}}$	X	X	X	X	Releases 32 SYS_CLK cycles after PERIP_$\overline{\text{RST}}$ is released

Figure 6-28 provides a graphic illustration of the details in **Table 6-3**. Note that the POR_Delay blocks use the OSC_CLK as their time base, since other system clocks are inactive during this phase of reset.

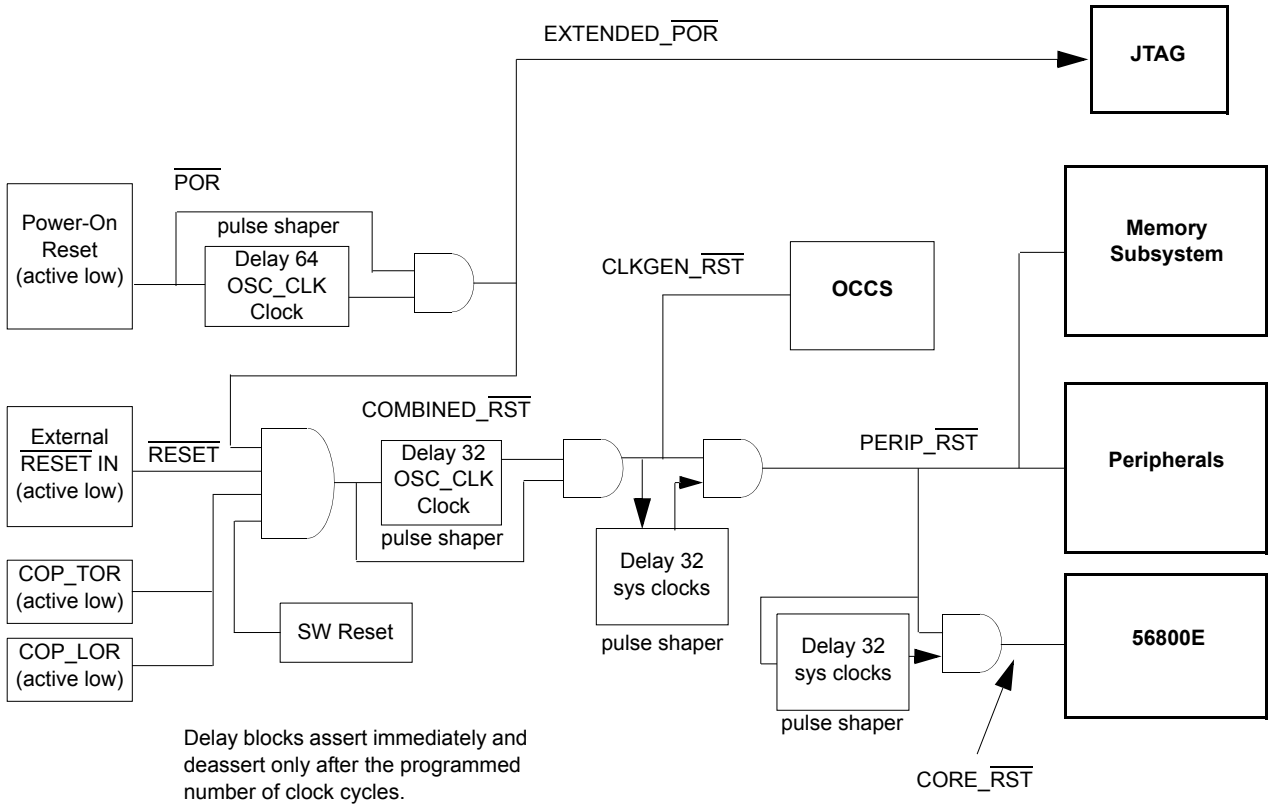

Figure 6-28 Sources of RESET Functional Diagram (Test modes not included)

POR resets are extended 64 OSC_CLK clocks to stabilize the power supply and clock source. All resets are subsequently extended for an additional 32 OSC_CLK clocks and 64 system clocks as the various internal reset controls are released. Given the normal relaxation oscillator rate of 8MHz, the duration of a POR reset from when power comes on to when code is running is 28µS. An external reset generation circuit may also be used. A description of how these resets are used to initialize the clocking system and system modules is included in **Section 6.7**.

6.7 Clocks

The memory, peripheral and core clocks all operate at the same frequency (32MHz maximum) with the exception of the peripheral clocks for quad timers TMRA and TMRB and the PWM, which have the option to operate at 3X system clock. The SIM is responsible for clock distributions.

While the SIM generates the ADC peripheral clock in the same way it generates all other peripheral clocks, the ADC standby and conversion clocks are generated by a direct interface between the ADC and the OCCS module.

Table 8-2 GPIO External Signals Map (Continued)

GPIO Function	Peripheral Function	LQFP Package Pin	Notes
GPIOD2	TCK	29	Defaults to TCK
GPIOD3	TMS	63	Defaults to TMS
GPIOD4	EXTAL	53	Defaults to D4
GPIOD5	XTAL / CLKIN	52	SIM register SIM_GPSCD is used to select between XTAL and CLKIN. Defaults to D5
GPIOD6	DAC0	18	Defaults to D6
GPIOD7	DAC1	15	Defaults to D7

8.3 Reset Values

Tables 8-1 and 8-2 detail registers for the 56F8037/56F8027; Figures 8-1 through 8-4 summarize register maps and reset values.

Table 10-18 I²C Timing (Continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum $t_{HD;\ DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
4. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement $t_{SU;\ DAT}$ >= 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT}$ = 1000 + 250 = 1250ns (according to the Standard mode I²C bus specification) before the SCL line is released.
5. C_b = total capacitance of the one bus line in pF

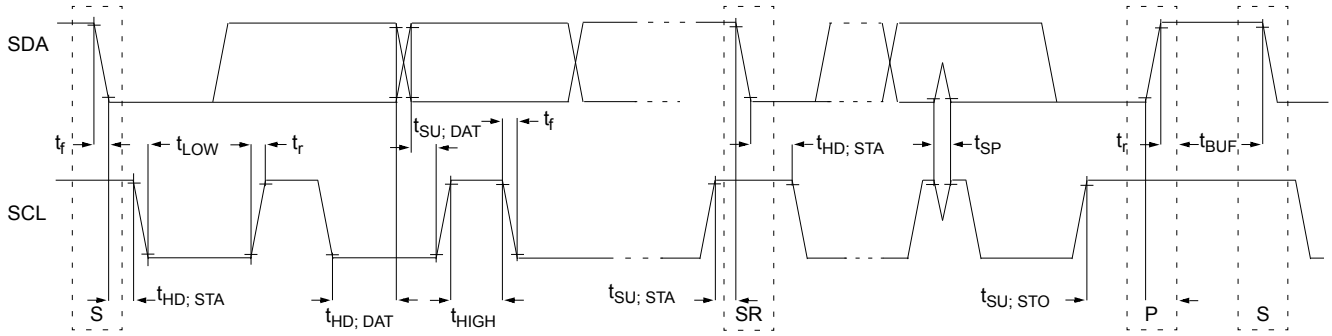

Figure 10-15 Timing Definition for Fast and Standard Mode Devices on the I²C Bus

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10mA into LEDs, then P = 8*.5*.01 = 40mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8037/56F8027:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the 56F8037/56F8027 and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible
- Bypass the V_{DD} and V_{SS} with approximately 100µF, plus the number of 0.1µF ceramic capacitors
- PCB trace lengths should be minimal for high-frequency signals
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.