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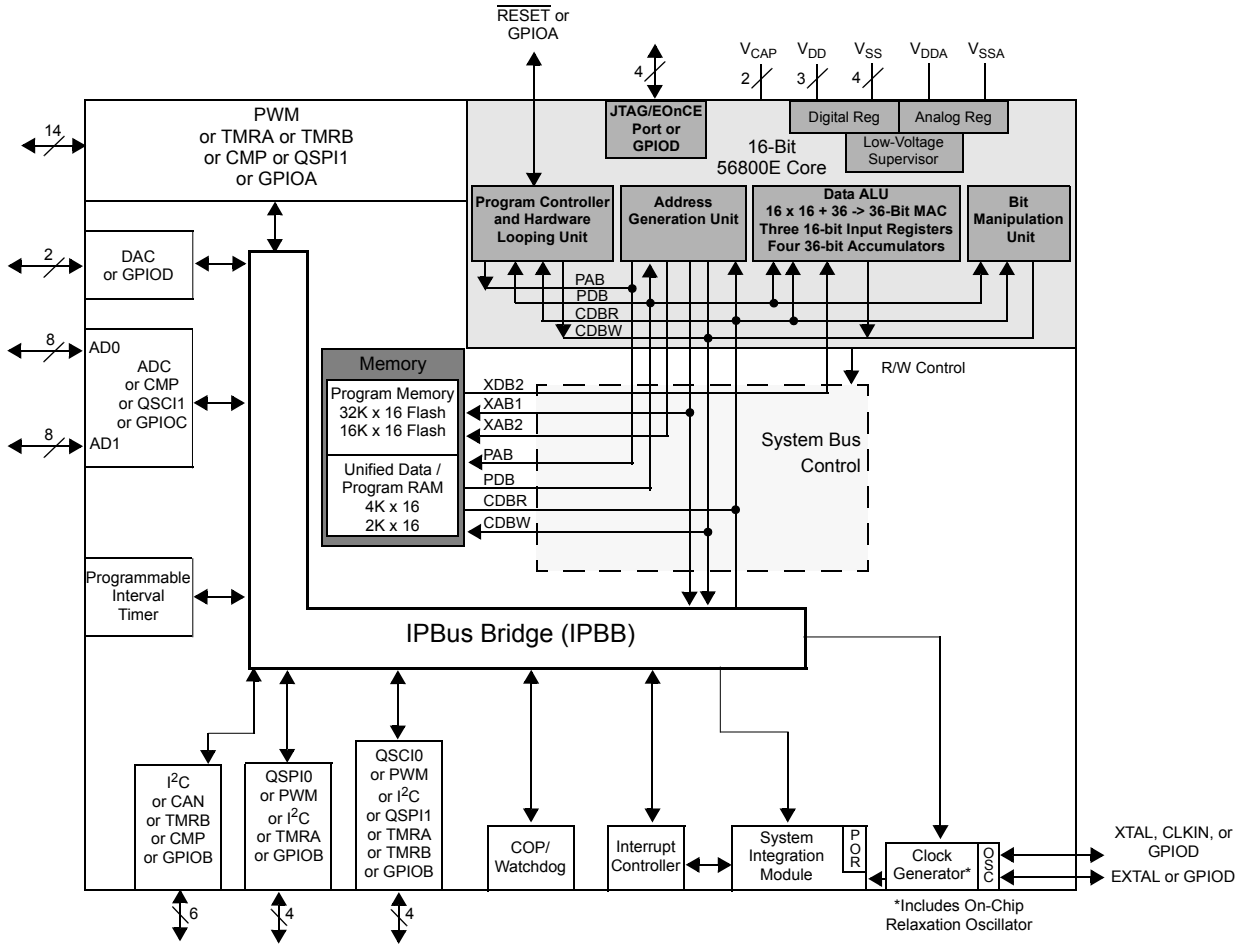
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8037mlh

56F8037/56F8027 General Description

- Up to 32 MIPS at 32MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- 56F8037 offers 64KB (32K x 16) Program Flash
- 56F8027 offers 32KB (16K x 16) Program Flash
- 56F8037 offers 8KB (4K x 16) Unified Data/Program RAM
- 56F8027 offers 4KB (2K x 16) Unified Data/Program RAM
- One 6-channel PWM module
- Two 8-channel 12-bit Analog-to-Digital Converters (ADCs)
- Two 12-bit Digital-to-Analog Converters (DACs)
- Two Analog Comparators
- Three Programmable Interval Timers (PITs)
- Two Queued Serial Communication Interfaces (QSCIs) with LIN slave functionality
- Two Queued Serial Peripheral Interfaces (QSPIs)
- Freescale's scalable controller area network (MSCAN) 2.0 A/B Module
- Two 16-bit Quad Timers
- One Inter-Integrated Circuit (I^2C) port
- Computer Operating Properly (COP)/Watchdog
- On-Chip Relaxation Oscillator
- Integrated Power-On Reset (POR) and Low-Voltage Interrupt (LVI) module
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging



56F8037/56F8027 Block Diagram

connections to the PWM from the TMR and GPIO. These signals can control the PWM outputs in a similar manner as the PWM generator. See the **56F802x and 56F803x Peripheral Reference Manual** for additional information.

The PWM_reload_sync output can be connected to Timer A's (TMRA) Channel 3 input; TMRA's Channels 2 and 3 outputs are connected to the ADC sync inputs. TMRA Channel 3 output is connected to SYNC0 and TMRA Channel 2 is connected to SYNC1. SYNC0 is the master ADC sync input that is used to trigger ADCA and ADCB in sequence and parallel mode. SYNC1 is used to trigger ADCB in parallel independent mode. These are controlled by bits in the SIM Control Register; see **Section 6.3.1**.

Table 2-3 56F8037/56F8027 Signal and Package Information for the 64-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOA10	35	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(TB2[6])		Input/ Output		**TB2** — Timer B, Channel 2.
(CMPAI2)		Input		**Comparator A, Input 2** — This is an analog input to Comparator A. After reset, the default state is GPIOA10. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[6]The TB2 signal is also brought out on the GPIOA13 pin.				
GPIOA11	6	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(TB3[7])		Input/ Output		**TB3** — Timer B, Channel 3.
(CMPBI2)		Input		**Comparator B, Input 2** — This is an analog input to Comparator B. After reset, the default state is GPIOA11. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[7]The TB3 signal is also brought out on the GPIOA14 pin.				
GPIOA12	37	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(SCLK1)		Input/ Output		**QSPI1 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity.
(TB1[8])		Input/ Output		**TB1** — Timer B, Channel 1.
(TA1[9])		Input/ Output		**TA1** — Timer A, Channel 1. After reset, the default state is GPIOA12. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[8]The TB1 signal is also brought out on the GPIOB11 pin. [9]The TA1 signal is also brought out on the GPIOB5 pin.				

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Table 2-3 56F8037/56F8027 Signal and Package Information for the 64-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB0	42	Input/ Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(SCLK0)		Input/ Output		**QSPI0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity.
(SCL[14])		Input/ Output		**Serial Clock** — This pin serves as the I^2C serial clock. After reset, the default state is GPIOB0. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[14]The SCL signal is also brought out on the GPIOB7 and GPIOB8 pins.				
GPIOB1	2	Input/ Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
($\overline{SS0}$)		Input/ Output		**QSPI0 Slave Select** — $\overline{SS}$ is used in slave mode to indicate to the QSPI0 module that the current transfer is to be received.
(SDA[15])		Input		**Serial Data** — This pin serves as the I^2C serial data line. After reset, the default state is GPIOB1. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[15]The SDA signal is also brought out on the GPIOB6 and GPIOB9 pins.				

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Table 2-3 56F8037/56F8027 Signal and Package Information for the 64-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOC12 **(ANB4)** **(RXD1)**	9	Input/ Output Analog Input Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANB4** — Analog input to ADC B, Channel 4. **Receive Data 1** — SCI1 receive data input. After reset, the default state is GPIOC12.
GPIOC13 **(ANB5)**	12	Input/ Output Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANB5** — Analog input to ADC B, Channel 5. After reset, the default state is GPIOC13.
GPIOC14 **(ANB6)**	62	Input/ Output Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANB6** — Analog input to ADC B, Channel 6. After reset, the default state is GPIOC14.
GPIOC15 **(ANB7)**	61	Input/ Output Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANB7** — Analog input to ADC B, Channel 7. After reset, the default state is GPIOC15.
GPIOD4 **(EXTAL)**	53	Input/ Output Analog Input	Input	**Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. **External Crystal Oscillator Input** — This input can be connected to an 8MHz external crystal. Tie this pin low if XTAL is being driven by an external clock source. After reset, the default state is GPIOD4.

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Table 4-8 Data Memory Peripheral Base Address Map Summary (Continued)

Peripheral	Prefix	Base Address	Table Number
DAC 0	DAC0	X:$00 F1C0	4-25
DAC 1	DAC1	X:$00 F1D0	4-26
Comparator A	CMPA	X:$00 F1E0	4-27
Comparator B	CMPB	X:$00 F1F0	4-28
QSCI 0	QSCI0	X:$00 F200	4-29
QSCI 1	QSCI1	X:$00 F210	4-30
QSPI 0	QSPI0	X:$00 F220	4-31
QSPI 1	QSPI1	X:$00 F230	4-32
I^2C	I2C	X:$00 F280	4-33
FM	FM	X:$00 F400	4-34
MSCAN	CAN	X:$00 F800	4-35

Table 4-10 Quad Timer B Registers Address Map (Continued) (TMRB_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
TMRB1_LOAD	$13	Load Register
TMRB1_HOLD	$14	Hold Register
TMRB1_CNTR	$15	Counter Register
TMRB1_CTRL	$16	Control Register
TMRB1_SCTRL	$17	Status and Control Register
TMRB1_CMPLD1	$18	Comparator Load Register 1
TMRB1_CMPLD2	$19	Comparator Load Register 2
TMRB1_CSCTRL	$1A	Comparator Status and Control Register
TMRB1_FILT	$1B	Input Filter Register
		Reserved
TMRB2_COMP1	$20	Compare Register 1
TMRB2_COMP2	$21	Compare Register 2
TMRB2_CAPT	$22	Capture Register
TMRB2_LOAD	$23	Load Register
TMRB2_HOLD	$24	Hold Register
TMRB2_CNTR	$25	Counter Register
TMRB2_CTRL	$26	Control Register
TMRB2_SCTRL	$27	Status and Control Register
TMRB2_CMPLD1	$28	Comparator Load Register 1
TMRB2_CMPLD2	$29	Comparator Load Register 2
TMRB2_CSCTRL	$2A	Comparator Status and Control Register
TMRB2_FILT	$2B	Input Filter Register
		Reserved
TMRB3_COMP1	$30	Compare Register 1
TMRB3_COMP2	$31	Compare Register 2
TMRB3_CAPT	$32	Capture Register
TMRB3_LOAD	$33	Load Register
TMRB3_HOLD	$34	Hold Register
TMRB3_CNTR	$35	Counter Register
TMRB3_CTRL	$36	Control Register
TMRB3_SCTRL	$37	Status and Control Register
TMRB3_CMPLD1	$38	Comparator Load Register 1
TMRB3_CMPLD2	$39	Comparator Load Register 2
TMRB3_CSCTRL	$3A	Comparator Status and Control Register
TMRB3_FILT	$3B	Input Filter Register
		Reserved

5.6.1.5 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)— Bits 7–6

This field is used to set the interrupt priority level for the EOnCE Transmit Register Empty IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.6 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)— Bits 5–4

This field is used to set the interrupt priority level for the EOnCE Trace Buffer IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.7 EOnCE Breakpoint Unit Interrupt Priority Level (BKPT_U IPL)— Bits 3–2

This field is used to set the interrupt priority level for the EOnCE Breakpoint Unit IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.8 EOnCE Step Counter Interrupt Priority Level (STPCNT IPL)— Bits 1–0

This field is used to set the interrupt priority level for the EOnCE Step Counter IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.3 Interrupt Priority Register 2 (IPR2)

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	QSCI0_XMIT IPL		QSPI1_XMIT IPL		QSPI1_RCV IPL		QSPI0_XMIT IPL		QSPI0_RCV IPL		GPIOA IPL		GPIOB IPL		GPIOC IPL	
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-5 Interrupt Priority Register 2 (IPR2)

5.6.3.1 QSCI 0 Transmitter Empty Interrupt Priority Level (QSCI0_XMIT IPL)—Bits 15–14

This field is used to set the interrupt priority level for the QSCI0 Transmitter Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.2 QSPI 1 Transmitter Empty Interrupt Priority Level (QSPI1_XMIT IPL)—Bits 13–12

This field is used to set the interrupt priority level for the QSPI1 Transmitter Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.3 QSPI 1 Receiver Full Interrupt Priority Level (QSPI1_RCV IPL)—Bits 11–10

This field is used to set the interrupt priority level for the QSPI1 Receiver Full IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.4 QSPI 0 Transmitter Empty Interrupt Priority Level (QSPI0_XMIT IPL)—Bits 9–8

This field is used to set the interrupt priority level for the QSPI0 Transmitter Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

5.6.5 Interrupt Priority Register 4 (IPR4)

Base + $4	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TMRA_3 IPL		TMRA_2 IPL		TMRA_1 IPL		TMRA_0 IPL		I2C_STAT IPL		I2C_TX IPL		I2C_RX IPL		I2C_GEN IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-7 Interrupt Priority Register 4 (IPR4)

5.6.5.1 Timer A, Channel 3 Interrupt Priority Level (TMRA_3 IPL)—Bits 15–14

This field is used to set the interrupt priority level for the Timer A, Channel 3 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.2 Timer A, Channel 2 Interrupt Priority Level (TMRA_2 IPL)—Bits 13–12

This field is used to set the interrupt priority level for the Timer A, Channel 2 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.3 Timer A, Channel 1 Interrupt Priority Level (TMRA_1 IPL)—Bits 11–10

This field is used to set the interrupt priority level for the Timer A, Channel 1 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

- 11 = IRQ is priority level 2

5.6.7 Interrupt Priority Register 6 (IPR6)

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	PWM_F IPL		PWM_RL IPL		ADC_ZC IPL		ADCB_CC IPL		ADCA_CC IPL		PIT2 IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-9 Interrupt Priority Register 6 (IPR6)

5.6.7.1 Reserved—Bits 15–12

This bit field is reserved. Each bit must be set to 0.

5.6.7.2 PWM Fault Interrupt Priority Level (PWM_F IPL)—Bits 11–10

This field is used to set the interrupt priority level for the PWM Fault Interrupt IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.3 Reload PWM Interrupt Priority Level (PWM_RL IPL)—Bits 9–8

This field is used to set the interrupt priority level for the Reload PWM Interrupt IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.4 ADC Zero Crossing Interrupt Priority Level (ADC_ZC IPL)—Bits 7–6

This field is used to set the interrupt priority level for the ADC Zero Crossing IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

- 11 = Write protection on and locked until chip reset

6.3.15.3 GPIO and Internal Peripheral Select Protection (GIPSP)—Bits 1–0

These bits enable write protection of GPS*n* and IPS*n* registers in the SIM module and write protect all GPIO*x*_PEREN, GPIO*x*_PPOUTM and GPIO*x*_DRIVE registers in GPIO modules.

- 00 = Write protection off (default)
- 01 = Write protection on
- 10 = Write protection off and locked until chip reset
- 11 = Write protection on and locked until chip reset

Note: The PWM fields in the CLKOUT register are also write protected by GIPSP. They are reserved for in-house test only.

6.3.16 SIM GPIO Peripheral Select Register 0 for GPIOA (SIM_GPSA0)

Most I/O pins have an associated GPIO function. In addition to the GPIO function, I/O can be configured to be one of several peripheral functions. The GPIO*x*_PEREN register within the GPIO module controls the selection between peripheral or GPIO control of the I/O pins. The GPIO function is selected when the GPIO*x*_PEREN bit for the I/O is 0. When the GPIO*x*_PEREN bit of the GPIO is 1, the fields in the GPS*n* registers select which peripheral function has control of the I/O. **Figure 6-18** illustrates the output path to an I/O pin when an I/O has two peripheral functions. Similar muxing is required on peripheral function inputs to receive input from the properly selected I/O pin.

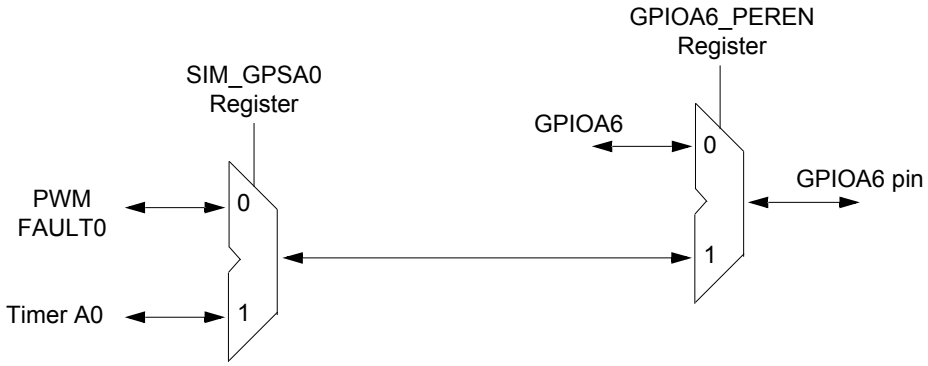


Figure 6-18 Overall Control of Signal Source Using SIM_GPS*nn* Control

In some cases, the user can choose peripheral function between several I/O, each of which have the option to be programmed to control a specific peripheral function. If the user wishes to use that function, only one of these I/O must be configured to control that peripheral function. If more than one I/O is configured to control the peripheral function, the peripheral output signal will fan out to each I/O, but the peripheral input signal will be the logical OR and AND of all the I/O signals.

Complete lists of I/O muxings are provided in **Table 2-3**.

The GPS*n* setting can be altered during normal operation, but a delay must be inserted between the time when one function is disabled and another function is enabled.

6.3.19.6 Configure GPIOB9 (GPS_B9)—Bit 4

This field selects the alternate function for GPIOB9.

- 0 = SDA - I^2C Serial Data (default)
- 1 = MSCANRX - MSCAN Receive Data

6.3.19.7 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

6.3.19.8 Configure GPIOB8 (GPS_B8)—Bit 2

This field selects the alternate function for GPIOB8.

- 0 = SCL - I2C Serial Clock (default)
- 1 = MSCANTX - MSCAN Transmit Data

6.3.19.9 Reserved—Bit 1

This bit field is reserved. It must be set to 0.

6.3.19.10 Configure GPIOB7 (GPS_B7)—Bit 0

This field selects the alternate function for GPIOB7.

- 0 = TXD0 - QSCI0 Transmit Data (default)
- 1 = SCL - I2C Serial Clock

6.3.20 SIM GPIO Peripheral Select Register for GPIOC and GPIOD (SIM_GPSCD)

See **Section 6.3.16** for general information about GPIO Peripheral Select Registers.

Base + $17	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	GPS_D5	0	0	0	0	0	0	0	GPS_C12	0	GPS_C8	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-23 GPIO Peripheral Select Register for GPIOC and GPIOD (SIM_GPSCD)

6.3.20.1 Reserved—Bits 15–13

This bit field is reserved. Each bit must be set to 0.

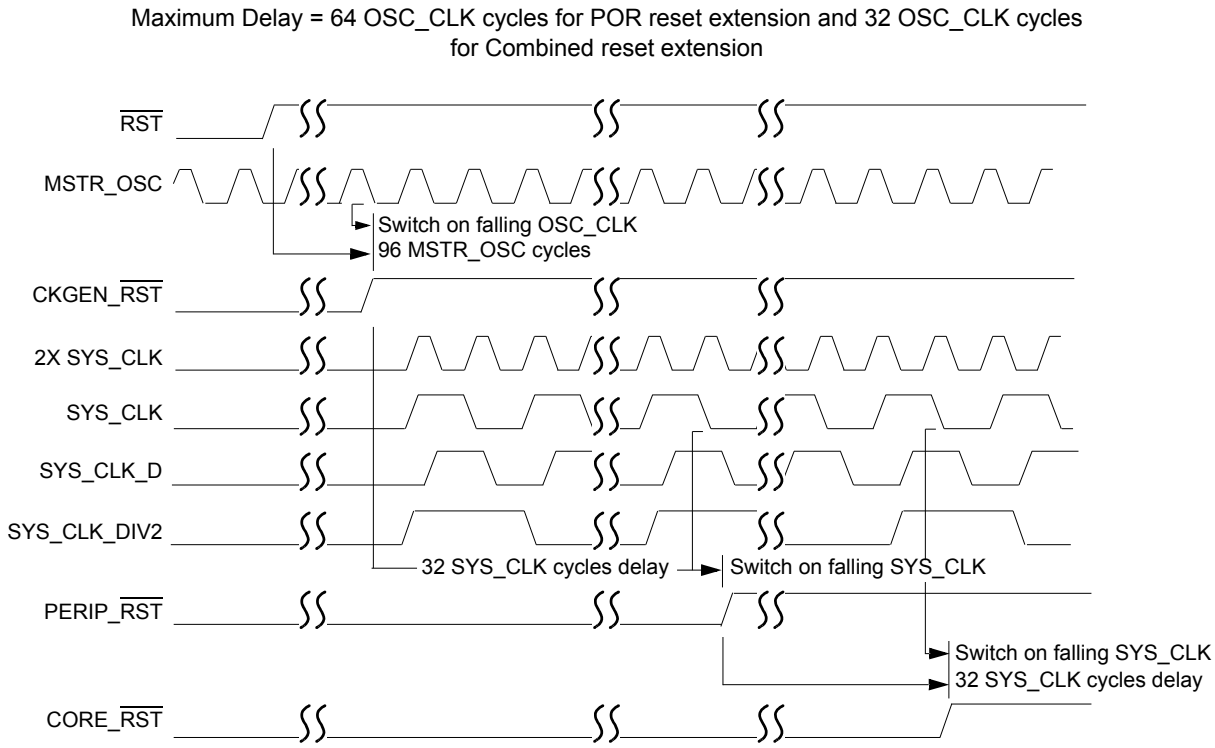


Figure 6-29 Timing Relationships of Reset Signal to Clocks

6.8 Interrupts

The SIM generates no interrupts.

Part 7 Security Features

The 56F8037/56F8027 offers security features intended to prevent unauthorized users from reading the contents of the flash memory (FM) array. The 56F8037/56F8027's flash security consists of several hardware interlocks that prevent unauthorized users from gaining access to the flash array.

After flash security is set, an authorized user is still able to access on-chip memory if a user-defined software subroutine, which reads and transfers the contents of internal memory via serial communication peripherals, is included in the application software.

7.1 Operation with Security Enabled

After the user has programmed flash with the application code, the 56F8037/56F8027 can be secured by programming the security word $0002 into program memory location $00 7FF7. This non-volatile word will keep the device secured through reset and through power-down of the device. Refer to the flash memory chapter in the **56F802x and 56F803x Peripheral Reference Manual** for the details. When flash security mode is enabled, the 56F8037/56F8027 will disable the core EOnCE debug capabilities. Normal

The user is responsible for directing the device to invoke the flash programming subroutine to reprogram the word $0000 into program memory location $00 7FF7. This is done by, for example, toggling a specific pin or downloading a user-defined key through serial interfaces.

Note: Flash contents can only be programmed for 1s to 0s.

7.3 Product Analysis

The recommended method of unsecuring a secured device for product analysis of field failures is via the method described in section 7.2.4. The customer would need to supply Technical Support with the details of the protocol to access the subroutines in flash memory. An alternative method for performing analysis on a secured device would be to mass-erase and reprogram the flash with the original code, but modify the security word or not program the security word.

Part 8 General Purpose Input/Output (GPIO)

8.1 Introduction

This section is intended to supplement the GPIO information found in the **56F802x and 56F803x Peripheral Reference Manual** and contains only chip-specific information. This information supersedes the generic information in the **56F802x and 56F803x Peripheral Reference Manual**.

8.2 Configuration

There are four GPIO ports defined on the 56F8037/56F8027. The width of each port, the associated peripheral and reset functions are shown in **Table 8-1**. The specific mapping of GPIO port pins is shown in **Table 8-2**. Additional details are shown in **Tables 2-2** and **2-3**.

Table 8-1 GPIO Ports Configuration

GPIO Port	Available Pins in 56F8037/56F8027	Peripheral Function	Reset Function
A	15	PWM, Timer, QSPI, Comparator, Reset	GPIO, $\overline{\text{RESET}}$
B	14	QSPI, I^2C, PWM, Clock, MSCAN, Comparator, Timer	GPIO
C	16	ADC, Comparator, QSCI	GPIO
D	8	Clock, Oscillator, DAC, JTAG	GPIO, JTAG

Part 9 Joint Test Action Group (JTAG)

9.1 56F8037/56F8027 Information

Please contact your Freescale sales representative or authorized distributor for device/package-specific BSDL information.

The $\overline{\text{TRST}}$ pin is not available in this package. The pin is tied to V_{DD} in the package.

The JTAG state machine is reset during POR and can also be reset via a soft reset by holding TMS high for five rising edges of TCK, as described in the **56F802x and 56F803x Peripheral Reference Manual**.

Part 10 Specifications

10.1 General Characteristics

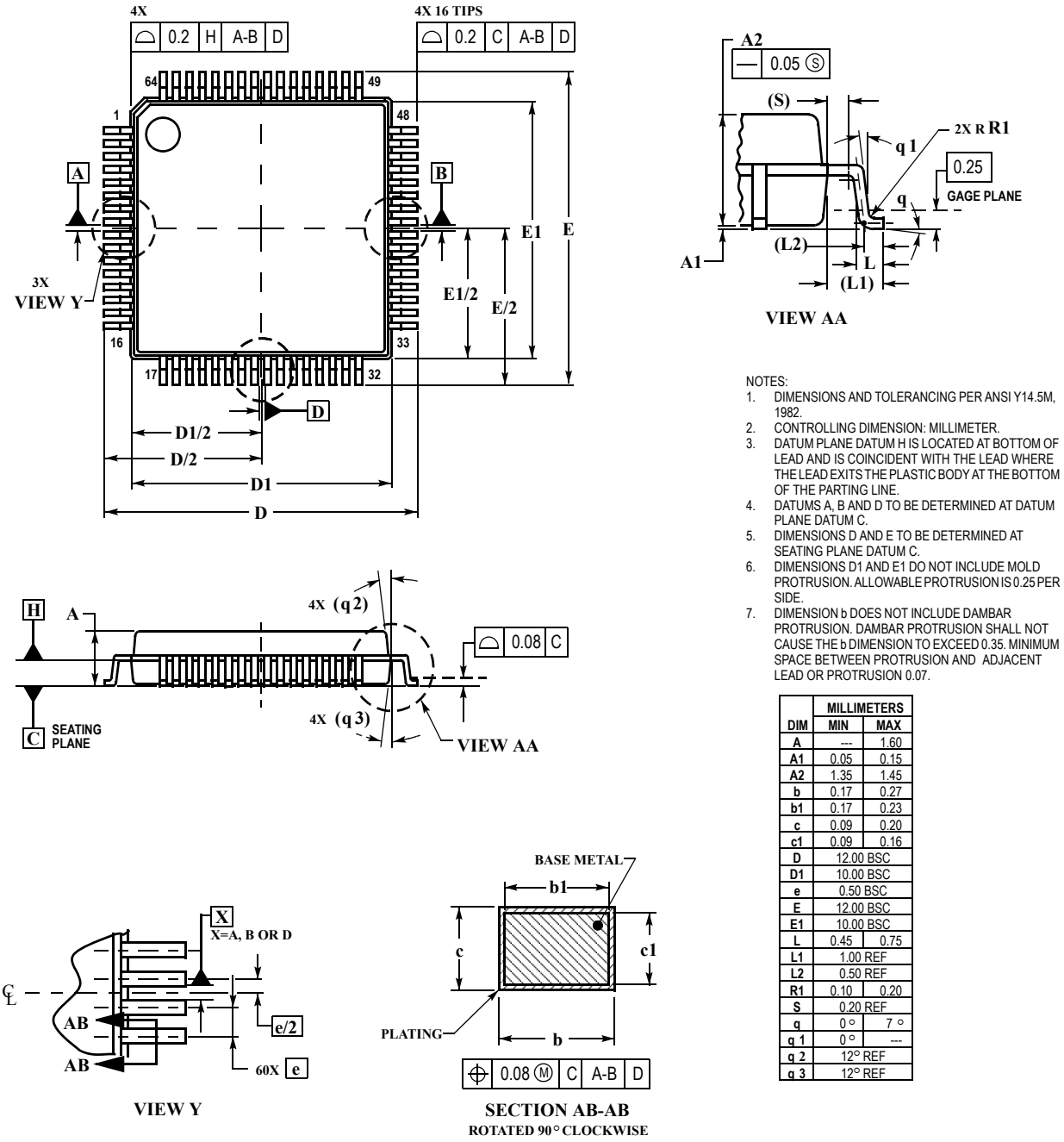
The 56F8037/56F8027 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term "5V-tolerant" refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels, combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40ºC to 125ºC ambient temperature over the following supply ranges:
$V_{SS} = V_{SSA} = 0V$, $V_{DD} = V_{DDA} = 3.0–3.6V$, $CL \leq 50pF$, $f_{OP} = 32MHz$

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either V_{DD} or V_{SS}).



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE DATUM H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE DATUM C.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM C.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	12.00 BSC	
D1	10.00 BSC	
e	0.50 BSC	
E	12.00 BSC	
E1	10.00 BSC	
L	0.45	0.75
L1	1.00 REF	
L2	0.50 REF	
R1	0.10	0.20
S	0.20 REF	
q	0°	7°
q 1	0°	---
q 2	12° REF	
q 3	12° REF	

Figure 11-2 56F8037/56F8027 64-Pin LQFP Mechanical Information

Please see **www.freescale.com** for the most current case outline.

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Security Low Half Register	SECLO	FMSECL	FM_SECLO	FMSECL	FMSECL	0xF404	
Protection Register	PROT	FMPROT	FM_PROT	FMPROT	FMPROT	0xF410	
User Status Register	USTAT	FMUSTAT	FM_USTAT	FMUSTAT	FMUSTAT	0xF413	
Command Register	CMD	FMCMD	FM_CMD	FMCMD	FMCMD	0xF414	
Data Buffer Register	DATA	FMDATA	FM_DATA	FMDATA	FMDATA	0xF418	
Info Optional Data 1 Register	OPT1	FMOPT1	FM_OPT1	FMOPT1	FMOPT1	0xF41B	
Test Array Signature Register	TSTSIG	FMTST_SIG	FM_TSTSIG	FMTST_SIG	FMTST_SIG	0xF41D	
General Purpose Input/Output (GPIO) Module							
					x = A (***n***=0) B (***n***=1) C (***n***=2) D (***n***=3)		
Pull-Up Enable Register	PUPEN	PUR	GPIO***x***_PUPEN	GPIO***x***_PUR	GPIO_***x***_PUR	0xF1***n***0	
Data Register	DATA	DR	GPIO***x***_DATA	GPIO***x***_DR	GPIO_***x***_DR	0xF1***n***1	
Data Direction Register	DDIR	DDR	GPIO***x***_DDIR	GPIO***x***_DDR	GPIO_***x***_DDR	0xF1***n***2	
Peripheral Enable Register	PEREN	PER	GPIO***x***_PEREN	GPIO***x***_PER	GPIO_***x***_PER	0xF1***n***3	
Interrupt Assert Register	IASSRT	IAR	GPIO***x***_IASSRT	GPIO***x***_IAR	GPIO_***x***_IAR	0xF1***n***4	
Interrupt Enable Register	IEN	IENR	GPIO***x***_IEN	GPIO***x***_IENR	GPIO_***x***_IENR	0xF1***n***5	
Interrupt Polarity Register	IPOL	IPOLR	GPIO***x***_IPOL	GPIO***x***_IPOLR	GPIO_***x***_IPOLR	0xF1***n***6	
Interrupt Pending Register	IPEND	IPR	GPIO***x***_IPEND	GPIO***x***_IPR	GPIO_***x***_IPR	0xF1***n***7	
Interrupt Edge-Sensitive Register	IEDGE	IESR	GPIO***x***_IEDGE	GPIO***x***_IESR	GPIO_***x***_IESR	0xF1***n***8	
Push-Pull Mode Registers	PPOUTM	PPMODE	GPIOx_PPOUTM	GPIO***x***_PPMODE	GPIO_***x***_PPMODE	0xF1***n***9	
Raw Data Input Register	RDATA	RAWDATA	GPIO***x***_RDATA	GPIOx_RAWDATA	GPIO_***x***_RAWDATA	0xF1***n***A	
Output Drive Strength Register	DRIVE	DRIVE	GPIO***x***_DRIVE	GPIO***x***_DRIVE	GPIO_***x***_DRIVE	0xF1***n***B	

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Transmitter Message Abort Acknowledge Register	TAAK		CAN_TAAK		CANTAAK	0XF809	
Transmitter FIFO Selection Register	TBSEL		CAN_TBSEL		CANTBSEL	0XF80A	
Identifier Acceptance Control Register	IDAC		CAN_IDAC		CANIDAC	0XF80B	
Miscellaneous Register	MISC		CAN_MISC		CANMISC	0XF80D	
Receive Error Register	RXERR		CAN_RXERR		CANRXERR	0XF80E	
Transmit Error Register	TXERR		CAN_TXERR		CANTXERR	0XF80F	
Identifier Acceptance 0-3 Registers	IDAR0-3		CAN_IDAR0-3		CANIDAR0-3	0xF810	0xF813
Identifier Mask 0-3 Registers	IDMR0-3		CAN_IDMR0-3		CANIDMR0-3	0xF814	0xF817
Identifier Acceptance 4-7 Register	IDAR4-7		CAN_IDAR4-7		CANIDAR4-7	0xF818	0xF81B
Identifier Mask 4-7 Registers	IDMR4-7		CAN_IDMR4-7		CANIDMR4-7	0xF81C	0xF81F
Foreground Receive FIFO Register	RXFG		CAN_RXFG		CANRXFG	0xF82F	0xF820
Foreground Transmit FIFO Register	TXFG		CAN_TXFG		CANTXFG	0xF830	0xF83F
Power Supervisor (PS) Module							
Control Register	CTRL	LVICONTROL	PS_CTRL	LVICONTROL	LVICTRL	0xF140	
Status Register	STAT	LVISTATUS	PS_STAT	LVISTATUS	LVISR	0xF141	
Queued Serial Communications Interface (QSCI) Module							
					n=0, 1		
Baud Rate Register	RATE		QSCI_RATE		QSCI_SCIBR	0xF2***n***0	
Control 1 Register	CTRL1		QSCI_CTRL1		QSCI_SCICR	0xF2***n***1	
Control 2 Register	CTRL2		QSCI_CTRL2		QSCI_SCICR2	0xF2***n***2	
Status Register	STAT		QSCI_STAT		QSCI_SCISR	0xF2***n***3	
Data Register	DATA		QSCI_DATA		QSCI_SCIDR	0xF2***n***4	
Queued Serial Peripheral Interface (QSPI) Module							
Status and Control Register	SCTRL		QSPI_SCTRL		QSPI_SPSCR	0xF2***n***0	
Data Size and Control Register	DSCTRL		QSPI_DSCTRL		QSPI_SPDSR	0xF2***n***1	
Data Receive Register	DRCV		QSPI_DRCV		QSPI_SPDRR	0xF2***n***2	
Data Transmit Register	DXMIT		QSPI_DXMIT		QSPI_SPDTR	0xF2***n***3	

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