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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8037vlh

Part 1 Overview

1.1 56F8037/56F8027 Features

1.1.1 Digital Signal Controller Core

- Efficient 16-bit 56800E family Digital Signal Controller (DSC) engine with dual Harvard architecture
- As many as 32 Million Instructions Per Second (MIPS) at 32MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging

1.1.2 Difference Between Devices

Table 1-1 outlines the key differences between the 56F8037 and 56F8027 devices.

Table 1-1 Device Differences

Feature	56F8037	56F8027
Program Flash	64KB	32KB
Unified Data/Program RAM	8KB	4KB

1.1.3 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal Flash
- On-chip memory
  - 64KB of Program Flash (56F8037 device)
    32KB of Program Flash (56F8027 device)
  - 8KB of Unified Data/Program RAM (56F8037 device)
    4KB of Unified Data/Program RAM (56F8027 device)
- EEPROM emulation capability using Flash

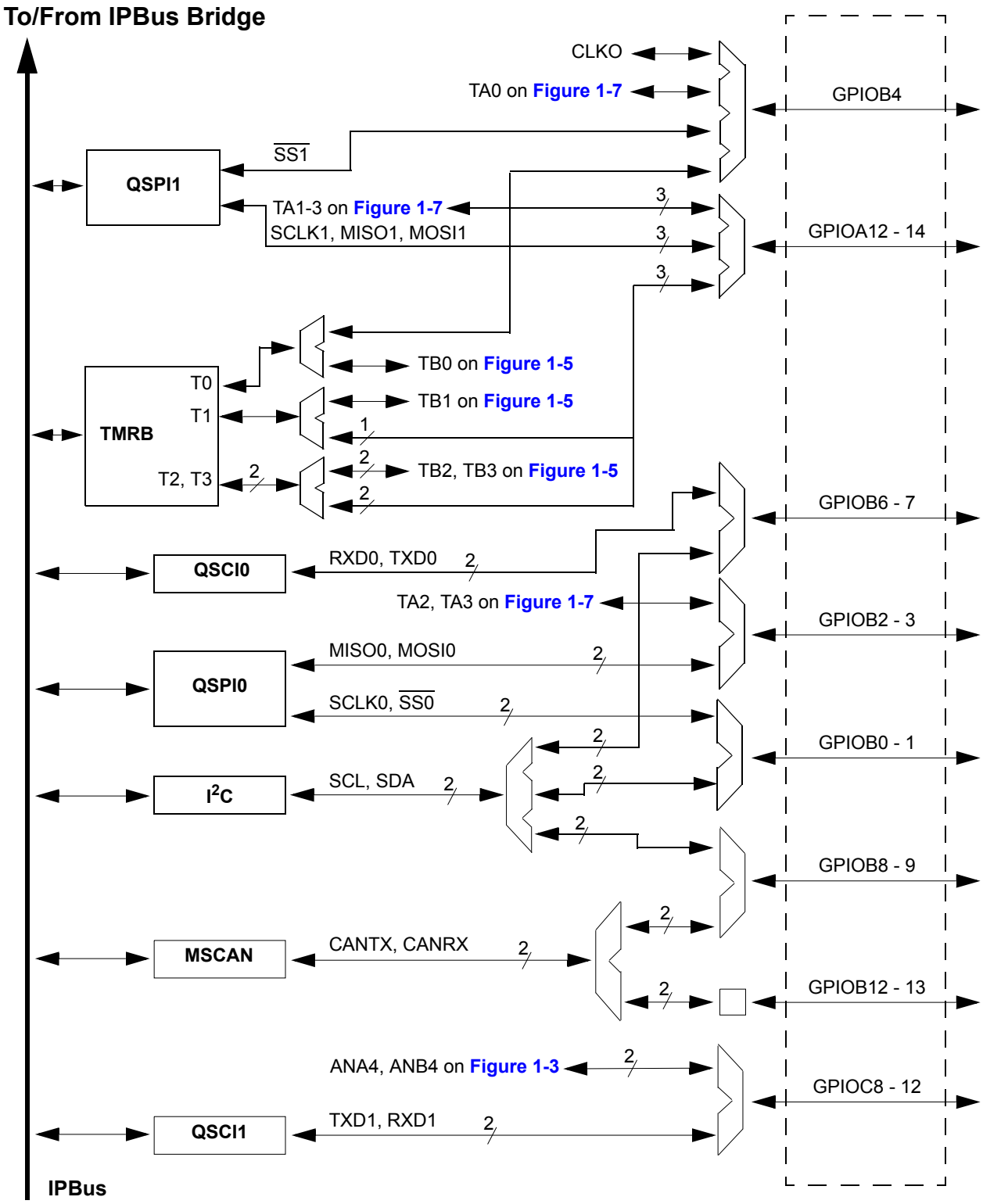

Figure 1-4 56F8037/56F8027 I/O Pin-Out Muxing (Part 2/5)

Table 2-3 56F8037/56F8027 Signal and Package Information for the 64-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOA10	35	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(TB2[6])		Input/ Output		**TB2** — Timer B, Channel 2.
(CMPAI2)		Input		**Comparator A, Input 2** — This is an analog input to Comparator A. After reset, the default state is GPIOA10. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[6]The TB2 signal is also brought out on the GPIOA13 pin.				
GPIOA11	6	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(TB3[7])		Input/ Output		**TB3** — Timer B, Channel 3.
(CMPBI2)		Input		**Comparator B, Input 2** — This is an analog input to Comparator B. After reset, the default state is GPIOA11. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[7]The TB3 signal is also brought out on the GPIOA14 pin.				
GPIOA12	37	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(SCLK1)		Input/ Output		**QSPI1 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity.
(TB1[8])		Input/ Output		**TB1** — Timer B, Channel 1.
(TA1[9])		Input/ Output		**TA1** — Timer A, Channel 1. After reset, the default state is GPIOA12. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[8]The TB1 signal is also brought out on the GPIOB11 pin. [9]The TA1 signal is also brought out on the GPIOB5 pin.				

Return to Table 2-2

Table 4-1 Chip Memory Configurations

On-Chip Memory	56F8037	56F8027	Use Restrictions
Program Flash (PFLASH)	32k x 16 or 64KB	16k x 16 or 32KB	Erase / Program via Flash interface unit and word writes to CDBW
Unified RAM (RAM)	4k x 16 or 8KB	2k x 16 or 4KB	Usable by both the Program and Data memory spaces

4.2 Interrupt Vector Table

Table 4-2 provides the 56F8037/56F8027's reset and interrupt priority structure, including on-chip peripherals. The table is organized with higher-priority vectors at the top and lower-priority interrupts lower in the table. As indicated, the priority of an interrupt can be assigned to different levels, allowing some control over interrupt priorities. All level 3 interrupts will be serviced before level 2, and so on. For a selected priority level, the lowest vector number has the highest priority.

The location of the vector table is determined by the Vector Base Address (VBA). Please see Section 5.6.8 for the reset value of the VBA.

By default, the chip reset address and COP reset address will correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Table 4-2 Interrupt Vector Table Contents[1]

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
core			P:$00	Reserved for Reset Overlay[2]
core			P:$02	Reserved for COP Reset Overlay
core	2	3	P:$04	Illegal Instruction
core	3	3	P:$06	SW Interrupt 3
core	4	3	P:$08	HW Stack Overflow
core	5	3	P:$0A	Misaligned Long Word Access
core	6	1-3	P:$0C	EOnCE Step Counter
core	7	1-3	P:$0E	EOnCE Breakpoint Unit
core	8	1-3	P:$10	EOnCE Trace Buffer
core	9	1-3	P:$12	EOnCE Transmit Register Empty
core	10	1-3	P:$14	EOnCE Receive Register Full
core	11	2	P:$16	SW Interrupt 2
core	12	1	P:$18	SW Interrupt 1
core	13	0	P:$1A	SW Interrupt 0
	14			Reserved

Table 4-24 Programmable Interval Timer 2 Registers Address Map (Continued) (PIT2_BASE = $00 F1B0)

Register Acronym	Address Offset	Register Description
PIT2_CNTR	$2	Counter Register

Table 4-25 Digital-to-Analog Converter 0 Registers Address Map (DAC0_BASE = $00 F1C0)

Register Acronym	Address Offset	Register Description
DAC0_CTRL	$0	Control Register
DAC0_DATA	$1	Data Register
DAC0_STEP	$2	Step Register
DAC0_MINVAL	$3	Minimum Value Register
DAC0_MAXVAL	$4	Maximum Value Register

Table 4-26 Digital-to-Analog Converter 0 Registers Address Map (DAC1_BASE = $00 F1D0)

Register Acronym	Address Offset	Register Description
DAC1_CTRL	$0	Control Register
DAC1_DATA	$1	Data Register
DAC1_STEP	$2	Step Register
DAC1_MINVAL	$3	Minimum Value Register
DAC1_MAXVAL	$4	Maximum Value Register

Table 4-27 Comparator A Registers Address Map (CMPA_BASE = $00 F1E0)

Register Acronym	Address Offset	Register Description
CMPA_CTRL	$0	Control Register
CMPA_STAT	$1	Status Register
CMPA_FILT	$2	Filter Register

Table 4-28 Comparator B Registers Address Map (CMPB_BASE = $00 F1F0)

Register Acronym	Address Offset	Register Description
CMPB_CTRL	$0	Control Register
CMPB_STAT	$1	Status Register
CMPB_FILT	$2	Filter Register

5.6.4 Interrupt Priority Register 3 (IPR3)

Base + $3	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	I2C_ERR IPL		QSCI1_RCV IPL		QSCI1_RERR IPL		QSCI1_TIDL IPL		QSCI1_XMIT IPL		QSCI0_RCV IPL		QSCI0_RERR IPL		QSCI0_TIDL IPL	
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-6 Interrupt Priority Register 3 (IPR3)

5.6.4.1 I^2C Error Interrupt Priority Level (I2C_ERR IPL)—Bits 15–14

This field is used to set the interrupt priority level for the I^2C Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.2 QSCI 1 Receiver Full Interrupt Priority Level (QSCI1_RCV IPL)—Bits 13–12

This field is used to set the interrupt priority level for the QSCI1 Receiver Full IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.3 QSCI 1 Receiver Error Interrupt Priority Level (QSCI1_RERR IPL)—Bits 11–10

This field is used to set the interrupt priority level for the QSCI1 Receiver Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.4 QSCI 1 Transmitter Idle Interrupt Priority Level (QSCI1_TIDL IPL)—Bits 9–8

This field is used to set the interrupt priority level for the QSCI1 Transmitter Idle IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1

5.6.8.2 Vector Address Bus (VAB) Bits 13–0

The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower 7 bits are determined based on the highest priority interrupt and are then appended onto VBA before presenting the full VAB to the Core.

5.6.9 Fast Interrupt Match 0 Register (FIM0)

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0					
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-11 Fast Interrupt Match 0 Register (FIM0)

5.6.9.1 Reserved—Bits 15–6

This bit field is reserved. Each bit must be set to 0.

5.6.9.2 Fast Interrupt 0 Vector Number (FAST INTERRUPT 0)—Bits 5–0

These values determine which IRQ will be Fast Interrupt 0. Fast Interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first. IRQs used as Fast Interrupts *must* be set to priority level 2. Unexpected results will occur if a Fast Interrupt vector is set to any other priority. A Fast Interrupt automatically becomes the highest-priority level 2 interrupt regardless of its location in the interrupt table prior to being declared as Fast Interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to the vector table.

5.6.10 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

Base + $9	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-12 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

5.6.10.1 Fast Interrupt 0 Vector Address Low (FIVAL0)—Bits 15–0

The lower 16 bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAH0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

$1A	SIM_IPS2	R	0	0	0	IPS2_TA3	0	0	0	IPS2_TA2	0	0	0	IPS2_TA1	0	0	0	0
		W																
	Reserved																	

0 = Read as 0 1 = Read as 1 = Reserved

Figure 6-1 SIM Register Map Summary

6.3.1 SIM Control Register (SIM_CTRL)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	ONCE EBL	SW RST	STOP_DISABLE		WAIT_DISABLE	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-2 SIM Control Register (SIM_CTRL)

6.3.1.1 Reserved—Bits 15–6

This bit field is reserved. Each bit must be set to 0.

6.3.1.2 OnCE Enable (ONCEEBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

Note: Using default state “0” is recommended.

6.3.1.3 Software Reset (SWRST)—Bit 4

- Writing 1 to this field will cause the device to reset
- Read is zero

6.3.1.4 Stop Disable (STOP_DISABLE)—Bits 3–2

- 00 = Stop mode will be entered when the 56800E core executes a STOP instruction
- 01 = The 56800E STOP instruction will not cause entry into Stop mode
- 10 = Stop mode will be entered when the 56800E core executes a STOP instruction and the STOP_DISABLE field is write-protected until the next reset
- 11 = The 56800E STOP instruction will not cause entry into Stop mode and the STOP_DISABLE field is write-protected until the next reset

6.3.1.5 Wait Disable (WAIT_DISABLE)—Bits 1–0

- 00 = Wait mode will be entered when the 56800E core executes a WAIT instruction
- 01 = The 56800E WAIT instruction will not cause entry into Wait mode
- 10 = Wait mode will be entered when the 56800E core executes a WAIT instruction and the WAIT_DISABLE field is write-protected until the next reset
- 11 = The 56800E WAIT instruction will not cause entry into Wait mode and the WAIT_DISABLE field is write-protected until the next reset

6.3.2 SIM Reset Status Register (SIM_RSTAT)

This read-only register is updated upon any system reset and indicates the cause of the most recent reset. It indicates whether the COP reset vector or regular reset vector (including Power-On Reset, External Reset, Software Reset) in the vector table is used. This register is asynchronously reset during Power-On Reset and subsequently is synchronously updated based on the precedence level of reset inputs. Only the most recent reset source will be indicated if multiple resets occur. If multiple reset sources assert simultaneously, the highest-precedence source will be indicated. The precedence from highest to lowest is Power-On Reset, External Reset, COP Loss of Reference Reset, COP Time-Out Reset, and Software Reset. Power-On Reset is always set during a Power-On Reset; however, Power-On Reset will be cleared and External Reset will be set if the external reset pin is asserted or remains asserted after the Power-On Reset has deasserted.

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	SWR	COP_ TOR	COP_ LOR	EXTR	POR	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Figure 6-3 SIM Reset Status Register (SIM_RSTAT)

6.3.2.1 Reserved—Bits 15–7

This bit field is reserved. Each bit must be set to 0.

6.3.2.2 Software Reset (SWR)—Bit 6

When set, this bit indicates that the previous system reset occurred as a result of a software reset (written 1 to SWRST bit in the SIM_CTRL register).

6.3.2.3 COP Time-Out Reset (COP_TOR)—Bit 5

When set, this bit indicates that the previous system reset was caused by the Computer Operating Properly (COP) module signaling a COP time-out reset. If COP_TOR is set as code starts executing, the COP reset vector in the vector table will be used. Otherwise, the normal reset vector is used.

6.3.2.4 COP Loss of Reference Reset (COP_LOR)—Bit 4

When set, this bit indicates that the previous system reset was caused by the Computer Operating Properly (COP) module signaling a loss of COP reference clock reset. If COP_LOR is set as code starts executing, the COP reset vector in the vector table will be used. Otherwise, the normal reset vector is used.

6.3.2.5 External Reset (EXTR)—Bit 3

When set, this bit indicates that the previous system reset was caused by an external reset.

6.3.2.6 Power-On Reset (POR)—Bit 2

This bit is set during a Power-On Reset.

The user is responsible for directing the device to invoke the flash programming subroutine to reprogram the word $0000 into program memory location $00 7FF7. This is done by, for example, toggling a specific pin or downloading a user-defined key through serial interfaces.

Note: Flash contents can only be programmed for 1s to 0s.

7.3 Product Analysis

The recommended method of unsecuring a secured device for product analysis of field failures is via the method described in section 7.2.4. The customer would need to supply Technical Support with the details of the protocol to access the subroutines in flash memory. An alternative method for performing analysis on a secured device would be to mass-erase and reprogram the flash with the original code, but modify the security word or not program the security word.

Part 8 General Purpose Input/Output (GPIO)

8.1 Introduction

This section is intended to supplement the GPIO information found in the **56F802x and 56F803x Peripheral Reference Manual** and contains only chip-specific information. This information supersedes the generic information in the **56F802x and 56F803x Peripheral Reference Manual**.

8.2 Configuration

There are four GPIO ports defined on the 56F8037/56F8027. The width of each port, the associated peripheral and reset functions are shown in **Table 8-1**. The specific mapping of GPIO port pins is shown in **Table 8-2**. Additional details are shown in **Tables 2-2** and **2-3**.

Table 8-1 GPIO Ports Configuration

GPIO Port	Available Pins in 56F8037/56F8027	Peripheral Function	Reset Function
A	15	PWM, Timer, QSPI, Comparator, Reset	GPIO, $\overline{\text{RESET}}$
B	14	QSPI, I^2C, PWM, Clock, MSCAN, Comparator, Timer	GPIO
C	16	ADC, Comparator, QSCI	GPIO
D	8	Clock, Oscillator, DAC, JTAG	GPIO, JTAG

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOA_PUPEN	R	0	PU[15:0]														
		W																
		RS	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$1	GPIOA_DATA	R	.0	D[15:0]														
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2	GPIOA_DDIR	R	.0.	DD[15:0]														
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOA_PEREN	R	0	PE[15:0]														
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$4	GPIOA_IASSRT	R	0	IA[15:0]														
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOA_IEN	R	0	IEN[15:0]														
		W																
		RS		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOA_IEPOL	R	0	IEPOL[15:0]														
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOA_IPEND	R	0	IPR[15:0]														
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOA_IEDGE	R	0	IES[15:0]														
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOA_PPOUTM	R	0	OEN[15:0]														
		W																
		RS	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$A	GPIOA_RDATA	R	0	RAW DATA[15:0]														
		W																
		RS	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$B	GPIOA_DRIVE	R	0	DRIVE[15:0]														
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-1 GPIOA Register Map Summary

Part 9 Joint Test Action Group (JTAG)

9.1 56F8037/56F8027 Information

Please contact your Freescale sales representative or authorized distributor for device/package-specific BSDL information.

The $\overline{\text{TRST}}$ pin is not available in this package. The pin is tied to V_{DD} in the package.

The JTAG state machine is reset during POR and can also be reset via a soft reset by holding TMS high for five rising edges of TCK, as described in the **56F802x and 56F803x Peripheral Reference Manual**.

Part 10 Specifications

10.1 General Characteristics

The 56F8037/56F8027 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term "5V-tolerant" refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels, combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40ºC to 125ºC ambient temperature over the following supply ranges:
$V_{SS} = V_{SSA} = 0V$, $V_{DD} = V_{DDA} = 3.0–3.6V$, $CL \leq 50pF$, $f_{OP} = 32MHz$

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either V_{DD} or V_{SS}).

10.2 DC Electrical Characteristics

Table 10-5 DC Electrical Characteristics
At Recommended Operating Conditions

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High (a) pull-up enabled or disabled	I_{IH}	Pin Groups 1, 2	—	0	+/- 2.5	µA	V_{IN} = 2.4V to 5.5V
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low[1] pull-up enabled pull-up disabled	I_{IL}	Pin Groups 1, 2	 -15 —	 -30 0	 -60 +/- 2.5	µA	V_{IN} = 0V
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40mV	—	Typically V_{DDA} - 40mV	V	—
Output Current [1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 2.5	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	—	0.35	—	V	—
Input Capacitance	C_{IN}		—	10	—	pF	—
Output Capacitance	C_{OUT}		—	10	—	pF	—

1. See **Figure 10-1**

Note: Pin groups are detailed following **Table 10-1**

Table 10-6 Current Consumption per Power Supply Pin (Continued)

Mode	Conditions	Typical @ 3.3V, 25°C		Maximum@ 3.6V, 25°C	
		I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
STANDBY > STOP	100kHz Device Clock Relaxation Oscillator in Standby mode PLL powered off Processor Core in STOP state All peripheral module and core clocks are off ADC/DAC/Comparator powered off Voltage regulator in Standby mode	540µA	0µA	650µA	1µA
POWERDOWN	Device Clock is off Relaxation Oscillator powered off PLL powered off Processor Core in STOP state All peripheral module and core clocks are off ADC /DAC/Comparator powered off Voltage Regulator in Standby mode	440µA	0µA	550µA	1µA

1. No Output Switching
   All ports configured as inputs
   All inputs Low
   No DC Loads

Table 10-7 Power-On Reset Low-Voltage Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Voltage Interrupt for 3.3V supply[1]	$V_{EI3.3}$	2.58	2.7	—	V
Low-Voltage Interrupt for 2.5V supply[2]	$V_{E12.5}$	—	2.15	—	V
Low-Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power-On Reset[3]	POR	—	1.8	1.9	V

1. When V_{DD} drops below $V_{EI3.3}$, an interrupt is generated.
2. When V_{DD} drops below $V_{EI32.5}$, an interrupt is generated.
3. Power-On Reset occurs whenever the internally regulated 2.5V digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 2.15V or the 3.3V 1/O voltage is below 2.7V, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp-up until 2.5V is reached, at which time it self-regulates.

10.2.1 Voltage Regulator Specifications

The 56F8037/56F8027 has two on-chip regulators. One supplies the PLL and relaxation oscillator. It has no external pins and therefore has no external characteristics which must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.5V to the 56F8037/56F8027's core logic. This regulator requires an external 4.4µF, or greater, capacitor for proper operation. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be

10.6 Phase Locked Loop Timing

Table 10-11 PLL Timing

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	4	8	—	MHz
Internal reference relaxation oscillator frequency for the PLL	f_{rosc}	—	8	—	MHz
PLL output frequency[2] (24 x reference frequency)	f_{op}	96	192	—	MHz
PLL lock time[3]	t_{plls}	—	40	100	µs
Accumulated jitter using an 8MHz external crystal as the PLL source[4]	J_A	—	—	0.37	%
Cycle-to-cycle jitter	$t_{jitterpll}$	—	350	—	ps

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input.
2. The core system clock will operate at 1/6 of the PLL output frequency.
3. This is the time required after the PLL is enabled to ensure reliable operation.
4. This is measured on the CLKO signal (programmed as System clock) over 264 System clocks at 32MHz System clock frequency and using an 8MHz oscillator frequency.

10.7 Relaxation Oscillator Timing

Table 10-12 Relaxation Oscillator Timing

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
Relaxation Oscillator output frequency[1] Normal Mode Standby Mode	f_{op}	—	 8.05 200	—	 MHz kHz
Relaxation Oscillator stabilization time[2]	t_{roscs}	—	1	3	ms
Cycle-to-cycle jitter. This is measured on the CLKO signal (programmed prescaler_clock) over 264 clocks[3]	$t_{jitterrosc}$	—	400	—	ps
Minimum tuning step size		—	.08	—	%
Maximum tuning step size		—	40	—	%
Variation over temperature -40°C to 150ºC[4]		—	+1.0 to -1.5	+3.0 to -3.0	%
Variation over temperature 0°C to 105ºC[4]		—	0 to +1	+2.0 to -2.0	%

1. Output frequency after factory trim.
2. This is the time required from Standby to Normal mode transition.
3. J_A is required to meet QSCI requirements.
4. See **Figure 10-5**

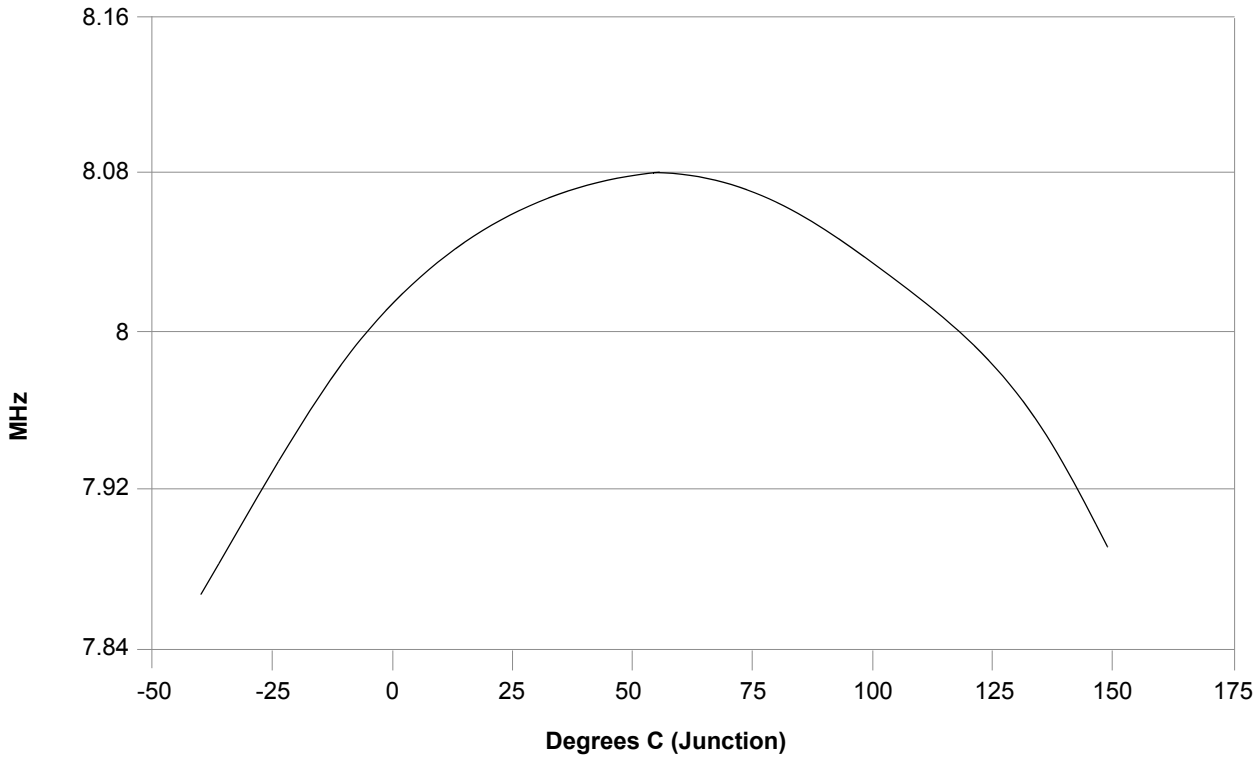

Figure 10-5 Relaxation Oscillator Temperature Variation (Typical) After Trim

10.9 Serial Peripheral Interface (SPI) Timing

Table 10-14 SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 125 62.5	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Enable lead time Master Slave	t_{ELD}	 — 31	 — —	 ns ns	10-10
Enable lag time Master Slave	t_{ELG}	 — 125	 — —	 ns ns	10-10
Clock (SCK) high time Master Slave	t_{CH}	 50 31	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Clock (SCK) low time Master Slave	t_{CL}	 50 31	 — —	 ns ns	10-10
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	10-10
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	10-10
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	10-7, 10-8, 10-9, 10-10
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	10-7, 10-8, 10-9, 10-10
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	10-7, 10-8, 10-9, 10-10
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	10-7, 10-8, 10-9, 10-10

1. Parameters listed are guaranteed by design.

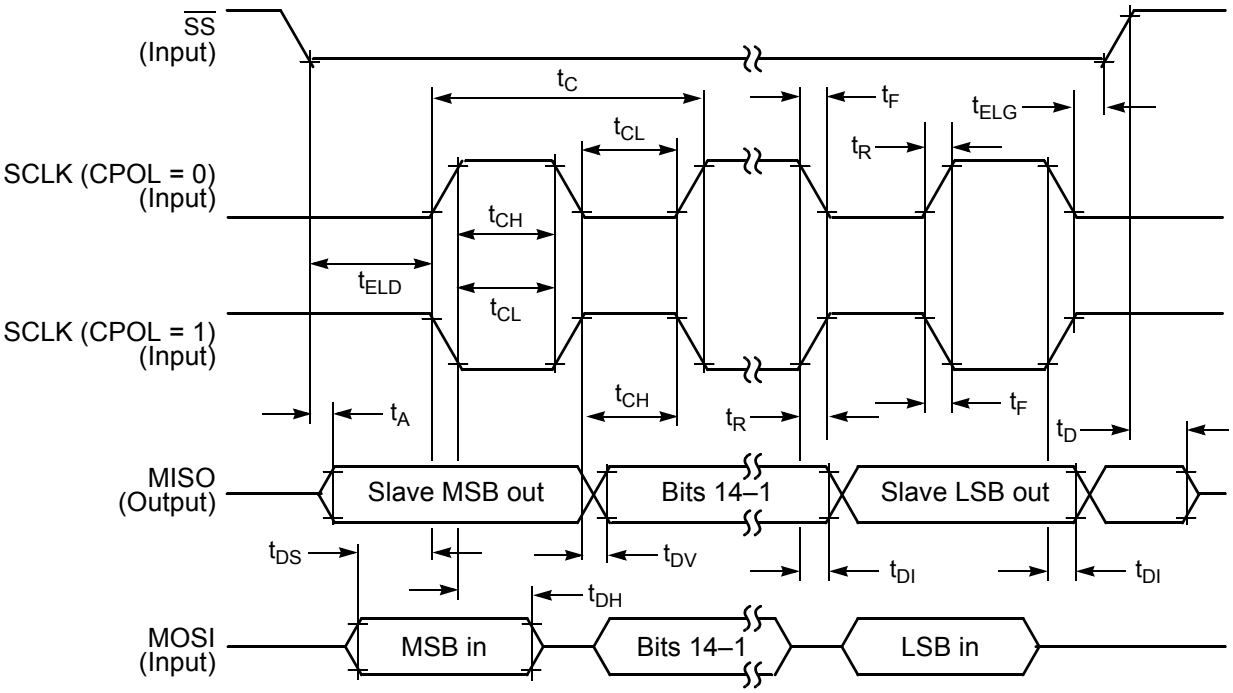

Figure 10-9 SPI Slave Timing (CPHA = 0)

10.15 Analog-to-Digital Converter (ADC) Parameters

Table 10-20 ADC Parameters[1]

Parameter	Symbol	Min	Typ	Max	Unit
DC Specifications					
Resolution	R_{ES}	12	—	12	Bits
ADC internal clock	f_{ADIC}	0.1	—	5.33	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC power-up time[2]	t_{ADPU}	—	6	13	t_{AIC} cycles[3]
Recovery from auto standby	t_{REC}	—	0	1	t_{AIC} cycles[3]
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Accuracy					
Integral non-linearity[4] (Full input signal range)	INL	—	+/- 3	+/- 5	LSB[5]
Differential non-linearity	DNL	—	+/- .6	+/- 1	LSB[5]
Monotonicity			GUARANTEED		
Offset Voltage Internal Ref	V_{OFFSET}	—	+/- 4	+/- 9	mV
Offset Voltage External Ref	V_{OFFSET}	—	+/- 6	+/- 12	mV
Gain Error (transfer gain)	E_{GAIN}	—	.998 to 1.002	1.01 to .99	—
ADC Inputs[6] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0	—	µA
Input injection current[7], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See **Figure 10-18**	—	pF
Input impedance	X_{IN}	—	See **Figure 10-18**	—	Ohms
AC Specifications					
Signal-to-noise ratio	SNR	60	65		dB
Total Harmonic Distortion	THD	60	64		dB
Spurious Free Dynamic Range	SFDR	61	66		dB
Signal-to-noise plus distortion	SINAD	58	62		dB
Effective Number Of Bits	ENOB	—	10.0		Bits

1. All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2. Includes power-up of ADC and V_{REF}
3. ADC clock cycles
4. INL measured from V_{IN} = V_{REFL} to V_{IN} = V_{REFH}
5. LSB = Least Significant Bit = 0.806mV
6. Pin groups are detailed following **Table 10-1**.
7. The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC.