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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8037vlhr

In **Table 2-2**, peripheral pins in bold identify reset state.

Table 2-2 56F8037/56F8027 Pins

			Peripherals:												
Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**QSCI**	**QSPI**	**ADC**	**PWM**	**Quad Timer**	**DAC**	**Comp**	**MSCAN**	**Power & Ground**	**JTAG**	**Misc.**
1	**GPIOB6**	GPIOB6, RXD0, SDA, CLKIN	**B6**	SDA	RXD0										CLKIN
2	**GPIOB1**	GPIOB1, $\overline{SS0}$, SDA	**B1**	SDA		$\overline{SS0}$									
3	**GPIOB7**	GPIOB7, TXD0, SCL	**B7**	SCL	TXD0										
4	**GPIOB5**	GPIOB5, TA1, FAULT3, CLKIN	**B5**					FAULT3	TA1						CLKIN
5	**GPIOA9**	GPIOA9, FAULT2, TA3, CMPBI1	**A9**					FAULT2	TA3		CMPBI1				
6	**GPIOA11**	GPIOA11, TB3, CMPBI2	**A11**						TB3		CMPBI2				
7	**VDD**	V_{DD}											V_{DD}		
8	**VSS**	V_{SS}											V_{SS}		
9	**GPIOC12**	GPIOC12, ANB4, RXD1	**C12**		RXD1		ANB4								
10	**GPIOC4**	GPIOC4, ANB0, CMPBI3	**C4**				ANB0				CMPBI3				
11	**GPIOC5**	GPIOC5, ANB1	**C5**				ANB1								
12	**GPIOC13**	GPIOC13, ANB5	**C13**				ANB5								
13	**GPIOC6**	ANB2, V_{REFHB}	**C6**				ANB2 V_{REFHB}								
14	**GPIOC7**	GPIOC7, ANB3, V_{REFLB}	**C7**				ANB3 V_{REFLB}								
15	**GPIOD7**	GPIOD7, DAC1	**D7**							DAC1					
16	**VDDA**	V_{DDA}											V_{DDA}		
17	**VSSA**	V_{SSA}											V_{SSA}		
18	**GPIOD6**	GPIOD6, DAC0	**D6**							DAC0					
19	**GPIOC3**	GPIOC3, ANA3, V_{REFLA}	**C3**				ANA3 V_{REFLA}								
20	**GPIOC2**	GPIOC2, ANA2, V_{REFHA}	**C2**				ANA2 V_{REFHA}								
21	**GPIOC9**	GPIOC9, ANA5	**C9**				ANA5								
22	**GPIOC1**	GPIOC1, ANA1	**C1**				ANA1								
23	**GPIOC10**	GPIOC10, ANA6	**C10**				ANA6								
24	**GPIOC0**	GPIOC0, ANA0, CMPAI3	**C0**				ANA0				CMPAI3				
25	**GPIOC11**	GPIOC11, ANA7	**C11**				ANA7								
26	**GPIOC8**	GPIOC8, ANA4, TXD1	**C8**		TXD1		ANA4								
27	**VSS**	V_{SS}											**V_{SS}**		

Table 4-1 Chip Memory Configurations

On-Chip Memory	56F8037	56F8027	Use Restrictions
Program Flash (PFLASH)	32k x 16 or 64KB	16k x 16 or 32KB	Erase / Program via Flash interface unit and word writes to CDBW
Unified RAM (RAM)	4k x 16 or 8KB	2k x 16 or 4KB	Usable by both the Program and Data memory spaces

4.2 Interrupt Vector Table

Table 4-2 provides the 56F8037/56F8027's reset and interrupt priority structure, including on-chip peripherals. The table is organized with higher-priority vectors at the top and lower-priority interrupts lower in the table. As indicated, the priority of an interrupt can be assigned to different levels, allowing some control over interrupt priorities. All level 3 interrupts will be serviced before level 2, and so on. For a selected priority level, the lowest vector number has the highest priority.

The location of the vector table is determined by the Vector Base Address (VBA). Please see Section 5.6.8 for the reset value of the VBA.

By default, the chip reset address and COP reset address will correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Table 4-2 Interrupt Vector Table Contents[1]

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
core			P:$00	Reserved for Reset Overlay[2]
core			P:$02	Reserved for COP Reset Overlay
core	2	3	P:$04	Illegal Instruction
core	3	3	P:$06	SW Interrupt 3
core	4	3	P:$08	HW Stack Overflow
core	5	3	P:$0A	Misaligned Long Word Access
core	6	1-3	P:$0C	EOnCE Step Counter
core	7	1-3	P:$0E	EOnCE Breakpoint Unit
core	8	1-3	P:$10	EOnCE Trace Buffer
core	9	1-3	P:$12	EOnCE Transmit Register Empty
core	10	1-3	P:$14	EOnCE Receive Register Full
core	11	2	P:$16	SW Interrupt 2
core	12	1	P:$18	SW Interrupt 1
core	13	0	P:$1A	SW Interrupt 0
	14			Reserved

5.3.1 Normal Interrupt Handling

Once the INTC has determined that an interrupt is to be serviced and which interrupt has the highest priority, an interrupt vector address is generated. Normal interrupt handling concatenates the Vector Base Address (VBA) and the vector number to determine the vector address, generating an offset into the vector table for each interrupt.

5.3.2 Interrupt Nesting

Interrupt exceptions may be nested to allow an IRQ of higher priority than the current exception to be serviced. The 56800E core controls the masking of interrupt priority levels it will accept by setting the I0 and I1 bits in its status register.

Table 5-1 Interrupt Mask Bit Definition

SR[9] (I1)	SR[8] (I0)	Exceptions Permitted	Exceptions Masked
0	0	Priorities 0, 1, 2, 3	None
0	1	Priorities 1, 2, 3	Priority 0
1	0	Priorities 2, 3	Priorities 0, 1
1	1	Priority 3	Priorities 0, 1, 2

The IPIC bits of the ICTRL register reflect the state of the priority level being presented to the 56800E core.

Table 5-2 Interrupt Priority Encoding

IPIC_VALUE[1:0]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No interrupt or SWILP	Priorities 0, 1, 2, 3
01	Priority 0	Priorities 1, 2, 3
10	Priority 1	Priorities 2, 3
11	Priority 2 or 3	Priority 3

5.3.3 Fast Interrupt Handling

Fast interrupts are described in the **DSP56800E Reference Manual**. The interrupt controller recognizes Fast Interrupts before the core does.

A Fast Interrupt is defined (to the ITCN) by:

1. Setting the priority of the interrupt as level 2, with the appropriate field in the IPR registers
2. Setting the FIM*n* register to the appropriate vector number

5.6.1 Interrupt Priority Register 0 (IPR0)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PLL IPL		LVI IPL		0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL		BKPT_U IPL		STPCNT IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-3 Interrupt Priority Register 0 (IPR0)

5.6.1.1 PLL Loss of Reference or Change in Lock Status Interrupt Priority Level (PLL IPL)—Bits 15–14

This field is used to set the interrupt priority levels for the PLL Loss of Reference or Change in Lock Status IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.2 Low Voltage Detector Interrupt Priority Level (LVI IPL)—Bits 13–12

This field is used to set the interrupt priority levels for the Low Voltage Detector IRQ. This IRQ is limited to priorities 1 through 3 and is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.3 Reserved—Bits 11–10

This bit field is reserved. Each bit must be set to 0.

5.6.1.4 EOnCE Receive Register Full Interrupt Priority Level (RX_REG IPL)— Bits 9–8

This field is used to set the interrupt priority level for the EOnCE Receive Register Full IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.5 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)— Bits 7–6

This field is used to set the interrupt priority level for the EOnCE Transmit Register Empty IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.6 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)— Bits 5–4

This field is used to set the interrupt priority level for the EOnCE Trace Buffer IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.7 EOnCE Breakpoint Unit Interrupt Priority Level (BKPT_U IPL)— Bits 3–2

This field is used to set the interrupt priority level for the EOnCE Breakpoint Unit IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.1.8 EOnCE Step Counter Interrupt Priority Level (STPCNT IPL)— Bits 1–0

This field is used to set the interrupt priority level for the EOnCE Step Counter IRQ. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.4 Interrupt Priority Register 3 (IPR3)

Base + $3	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	I2C_ERR IPL		QSCI1_RCV IPL		QSCI1_RERR IPL		QSCI1_TIDL IPL		QSCI1_XMIT IPL		QSCI0_RCV IPL		QSCI0_RERR IPL		QSCI0_TIDL IPL	
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-6 Interrupt Priority Register 3 (IPR3)

5.6.4.1 I^2C Error Interrupt Priority Level (I2C_ERR IPL)—Bits 15–14

This field is used to set the interrupt priority level for the I^2C Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.2 QSCI 1 Receiver Full Interrupt Priority Level (QSCI1_RCV IPL)—Bits 13–12

This field is used to set the interrupt priority level for the QSCI1 Receiver Full IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.3 QSCI 1 Receiver Error Interrupt Priority Level (QSCI1_RERR IPL)—Bits 11–10

This field is used to set the interrupt priority level for the QSCI1 Receiver Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.4 QSCI 1 Transmitter Idle Interrupt Priority Level (QSCI1_TIDL IPL)—Bits 9–8

This field is used to set the interrupt priority level for the QSCI1 Transmitter Idle IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1

5.6.7.5 ADC B Conversion Complete Interrupt Priority Level (ADCB_CC IPL)—Bits 5–4

This field is used to set the interrupt priority level for the ADC B Conversion Complete IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.6 ADC A Conversion Complete Interrupt Priority Level (ADCA_CC IPL)—Bits 3–2

This field is used to set the interrupt priority level for the ADC A Conversion Complete IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.7 Programmable Interval Timer 2 Interrupt Priority Level (PIT2 IPL)—Bits 1–0

This field is used to set the interrupt priority level for the Programmable Interval Timer 2 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8 Vector Base Address Register (VBA)

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	VECTOR_BASE_ADDRESS													
Write																
RESET[1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1. The 56F8037 resets to a value of 0x0000. This corresponds to reset addresses of 0x000000.
The 56F8027 resets to a value of 0x0080. This corresponds to reset addresses of 0x004000.

Figure 5-10 Vector Base Address Register (VBA)

5.6.8.1 Reserved—Bits 15–14

This bit field is reserved. Each bit must be set to 0.

6.3 Register Descriptions

A write to an address without an associated register is an NOP. A read from an address without an associated register returns unknown data.

Table 6-1 SIM Registers (SIM_BASE = $00 F100)

Register Acronym	Base Address +	Register Name	Section Location
CTRL	$0	Control Register	6.3.1
RSTAT	$1	Reset Status Register	6.3.2
SWC0	$2	Software Control Register 0	6.3.3
SWC1	$3	Software Control Register 1	6.3.3
SWC2	$4	Software Control Register 2	6.3.3
SWC3	$5	Software Control Register 3	6.3.3
MSHID	$6	Most Significant Half of JTAG ID	6.3.4
LSHID	$7	Least Significant Half of JTAG ID	6.3.5
PWR	$8	Power Control Register	6.3.6
		Reserved	
CLKOUT	$A	CLKO Select Register	6.3.7
PCR	$B	Peripheral Clock Rate Register	6.3.8
PCE0	$C	Peripheral Clock Enable Register 0	6.3.9
PCE1	$D	Peripheral Clock Enable Register 0	6.3.10
SD0	$E	Stop Disable Register 0	6.3.11
SD1	$F	Stop Disable Register 1	6.3.12
IOSAHI	$10	I/O Short Address Location High Register	6.3.13
IOSALO	$11	I/O Short Address Location Low Register	6.3.14
PROT	$12	Protection Register	6.3.15
GPSA0	$13	GPIO Peripheral Select Register 0 for GPIOA	6.3.16
GPSA1	$14	GPIO Peripheral Select Register 1 for GPIOA	6.3.17
GPSB0	$15	GPIO Peripheral Select Register 0 for GPIOB	6.3.18
GPSB1	$16	GPIO Peripheral Select Register 1 for GPIOB	6.3.19
GPSCD	$17	GPIO Peripheral Select Register for GPIOC and GPIOD	6.3.20
IPS0	$18	Internal Peripheral Source Select Register 0 for PWM	6.3.21
IPS1	$19	Internal Peripheral Source Select Register 1 for DACs	6.3.22
IPS2	$1A	Internal Peripheral Source Select Register 2 for Quad Timer A	6.3.23
		Reserved	

6.3.10.1 Reserved—Bit 15

This bit field is reserved. It must be set to 0.

6.3.10.2 Programmable Interval Timer 2 Clock Enable (PIT2)—Bit 14

- 0 = The clock is not provided to the PIT2 module (the PIT2 module is disabled)
- 1 = The clock is enabled to the PIT2 module

6.3.10.3 Programmable Interval Timer 1 Clock Enable (PIT1)—Bit 13

- 0 = The clock is not provided to the PIT1 module (the PIT1 module is disabled)
- 1 = The clock is enabled to the PIT1 module

6.3.10.4 Programmable Interval Timer 0 Clock Enable (PIT0)—Bit 12

- 0 = The clock is not provided to the PIT0 module (the PIT0 module is disabled)
- 1 = The clock is enabled to the PIT0 module

6.3.10.5 Reserved—Bits 11–8

This bit field is reserved. Each bit must be set to 0.

6.3.10.6 Quad Timer B, Channel 3 Clock Enable (TB3)—Bit 7

- 0 = The clock is not provided to the Timer B3 module (the Timer B3 module is disabled)
- 1 = The clock is enabled to the Timer B3 module

6.3.10.7 Quad Timer B, Channel 2 Clock Enable (TB2)—Bit 6

- 0 = The clock is not provided to the Timer B2 module (the Timer B2 module is disabled)
- 1 = The clock is enabled to the Timer B2 module

6.3.10.8 Quad Timer B, Channel 1 Clock Enable (TB1)—Bit 5

- 0 = The clock is not provided to the Timer B1 module (the Timer B1 module is disabled)
- 1 = The clock is enabled to the Timer B1 module

6.3.10.9 Quad Timer B, Channel 0 Clock Enable (TB0)—Bit 4

- 0 = The clock is not provided to the Timer B0 module (the Timer B0 module is disabled)
- 1 = The clock is enabled to the Timer B0 module

6.3.10.10 Quad Timer A, Channel 3 Clock Enable (TA3)—Bit 3

- 0 = The clock is not provided to the Timer A3 module (the Timer A3 module is disabled)
- 1 = The clock is enabled to the Timer A3 module

6.3.10.11 Quad Timer A, Channel 2 Clock Enable (TA2)—Bit 2

- 0 = The clock is not provided to the Timer A2 module (the Timer A2 module is disabled)
- 1 = The clock is enabled to the Timer A2 module

6.3.11.3 Digital-to-Analog Converter 1 Clock Stop Disable (DAC1_SD)—Bit 13

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.4 Digital-to-Analog Converter 0 Clock Stop Disable (DAC0_SD)—Bit 12

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.5 Reserved—Bit 11

This bit field is reserved. It must be set to 0.

6.3.11.6 Analog-to-Digital Converter Clock Stop Disable (ADC_SD)—Bit 10

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.7 Reserved—Bits 9–7

This bit field is reserved. Each bit must be set to 0.

6.3.11.8 Inter-Integrated Circuit Clock Stop Disable (I2C_SD)—Bit 6

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.9 QSCI1 Clock Stop Disable (QSCI1_SD)—Bit 5

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.10 QSCI0 Clock Stop Disable (QSCI0_SD)—Bit 4

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.11 QSPI1 Clock Stop Disable (QSPI1_SD)—Bit 3

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

6.3.11.12 QSPI0 Clock Stop Disable (QSPI0_SD)—Bit 2

Each bit controls clocks to the indicated peripheral.

Note: After reset, all I/O pins are GPIO, except the JTAG pins and the $\overline{\text{RESET}}$ pin.

Base + $13	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	GPS_A6	GPS_A5		GPS_A4		0	0	0	0	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-19 GPIO Peripheral Select Register 0 for GPIOA (SIM_GPSA0)

6.3.16.1 Reserved—Bits 15–13

This bit field is reserved. Each bit must be set to 0.

6.3.16.2 Configure GPIOA6 (GPS_A6)—Bit 12

This field selects the alternate function for GPIOA6.

- 0 = FAULT0 - PWM FAULT0 Input (default)
- 1 = TA0 - Timer A0

6.3.16.3 Configure GPIOA5 (GPS_A5)—Bits 11–10

This field selects the alternate function for GPIOA5.

- 00 = PWM5 - PWM5 (default)
- 01 = FAULT2 - PWM FAULT2 Input
- 10 = TA3 - Timer A3
- 11 = Reserved

6.3.16.4 Configure GPIOA4 (GPS_A4)—Bits 9–8

This field selects the alternate function for GPIOA4.

- 00 = PWM4 - PWM4 (default)
- 01 = FAULT1 - PWM FAULT1 Input
- 10 = TA2 - Timer A2
- 11 = Reserved

6.3.16.5 Reserved—Bits 7–0

This bit field is reserved. Each bit must be set to 0.

6.3.17 SIM GPIO Peripheral Select Register 1 for GPIOA (SIM_GPSA1)

See **Section 6.3.16** for general information about GPIO Peripheral Select Registers.

Base + $14	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	GPS_A14		GPS_A13		GPS_A12		0	GPS_A11	0	GPS_A10	GPS_A9		GPS_A8	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-20 GPIO Peripheral Select Register 1 for GPIOA (SIM_GPSA1)

6.3.17.1 Reserved—Bits 15–14

This bit field is reserved. Each bit must be set to 0.

6.3.17.2 Configure GPIOA14 (GPS_A14)—Bits 13–12

This field selects the alternate function for GPIOA14.

- 00 = TB3 - Timer B3 (default)
- 01 = MOSI1 - QSPI1 Master Out/Slave In
- 10 = TA3 - Timer A3
- 11 = Reserved

6.3.17.3 Configure GPIOA13 (GPS_A13)—Bits 11–10

This field selects the alternate function for GPIOA13.

- 00 = TB2 - Timer B2 (default)
- 01 = MISO1 - QSPI1 Master In/Slave Out
- 10 = TA2 - Timer A2
- 11 = Reserved

6.3.17.4 Configure GPIOA12 (GPS_A12)—Bits 9–8

This field selects the alternate function for GPIOA12.

- 00 = TB1- Timer B1 (default)
- 01 = SCLK1 - QSPI1 Serial Clock
- 10 = TA1 - Timer A1
- 11 = Reserved

6.3.17.5 Reserved—Bit 7

This bit field is reserved. It must be set to 0.

6.3.17.6 Configure GPIOA11 (GPS_A11)—Bit 6

This field selects the alternate function for GPIOA11.

- 0 = CMPBI2 - Comparator B Input 2 (default)
- 1 = TB3 - Timer B3

- 10 = CLKIN - External Clock Input
- 11 = Reserved

6.3.18.3 Configure GPIOB5 (GPS_B5)—Bits 12–11

This field selects the alternate function for GPIOB5.

- 00 = TA1 - Timer A1 (default)
- 01 = FAULT3 - PWM FAULT3 Input
- 10 = CLKIN - External Clock Input
- 11 = Reserved

6.3.18.4 Configure GPIOB4(GPS_B4)—Bits 10–8

This field selects the alternate function for GPIOB4.

- 000 = TA0 - Timer A0 (default)
- 001 = CLKO - Clock Output
- 010 = $\overline{SS}$1 - QSPI1 Slave Select
- 011 = TB0 - Timer B0
- 100 = PSRC2 - PWM4 / PWM5 Pair External Source
- 11x = Reserved
- 1x1 = Reserved

6.3.18.5 Configure GPIOB3 (GPS_B3)—Bits 7–6

This field selects the alternate function for GPIOB3.

- 00 = MOSI0 - QSPI0 Master Out/Slave In (default)
- 01 = TA3 - Timer A3
- 10 = PSRC1 - PWM2 / PWM3 Pair External Source
- 11 = Reserved

6.3.18.6 Configure GPIOB2 (GPS_B2)—Bits 5–4

This field selects the alternate function for GPIOB2.

- 00 = MISO0 QSPI0 Master In/Slave Out (default)
- 01 = TA2 - Timer A2
- 10 = PSRC0 - PWM0 / PWM1 Pair External Source
- 11 = Reserved

6.3.18.7 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

6.3.18.8 Configure GPIOB1 (GPS_B1)—Bit 2

This field selects the alternate function for GPIOB1.

The user is responsible for directing the device to invoke the flash programming subroutine to reprogram the word $0000 into program memory location $00 7FF7. This is done by, for example, toggling a specific pin or downloading a user-defined key through serial interfaces.

Note: Flash contents can only be programmed for 1s to 0s.

7.3 Product Analysis

The recommended method of unsecuring a secured device for product analysis of field failures is via the method described in section 7.2.4. The customer would need to supply Technical Support with the details of the protocol to access the subroutines in flash memory. An alternative method for performing analysis on a secured device would be to mass-erase and reprogram the flash with the original code, but modify the security word or not program the security word.

Part 8 General Purpose Input/Output (GPIO)

8.1 Introduction

This section is intended to supplement the GPIO information found in the **56F802x and 56F803x Peripheral Reference Manual** and contains only chip-specific information. This information supersedes the generic information in the **56F802x and 56F803x Peripheral Reference Manual**.

8.2 Configuration

There are four GPIO ports defined on the 56F8037/56F8027. The width of each port, the associated peripheral and reset functions are shown in **Table 8-1**. The specific mapping of GPIO port pins is shown in **Table 8-2**. Additional details are shown in **Tables 2-2** and **2-3**.

Table 8-1 GPIO Ports Configuration

GPIO Port	Available Pins in 56F8037/56F8027	Peripheral Function	Reset Function
A	15	PWM, Timer, QSPI, Comparator, Reset	GPIO, $\overline{\text{RESET}}$
B	14	QSPI, I^2C, PWM, Clock, MSCAN, Comparator, Timer	GPIO
C	16	ADC, Comparator, QSCI	GPIO
D	8	Clock, Oscillator, DAC, JTAG	GPIO, JTAG

Part 9 Joint Test Action Group (JTAG)

9.1 56F8037/56F8027 Information

Please contact your Freescale sales representative or authorized distributor for device/package-specific BSDL information.

The $\overline{\text{TRST}}$ pin is not available in this package. The pin is tied to V_{DD} in the package.

The JTAG state machine is reset during POR and can also be reset via a soft reset by holding TMS high for five rising edges of TCK, as described in the **56F802x and 56F803x Peripheral Reference Manual**.

Part 10 Specifications

10.1 General Characteristics

The 56F8037/56F8027 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term "5V-tolerant" refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels, combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40ºC to 125ºC ambient temperature over the following supply ranges:
$V_{SS} = V_{SSA} = 0V$, $V_{DD} = V_{DDA} = 3.0–3.6V$, $CL \leq 50pF$, $f_{OP} = 32MHz$

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either V_{DD} or V_{SS}).

temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

7. See **Section 12.1** for more details on thermal design considerations.

Table 10-4 Recommended Operating Conditions
($V_{REFL\ x}$= 0V, V_{SSA} = 0V, V_{SS} = 0V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD}, V_{DDA}		3	3.3	3.6	V
ADC Reference Voltage High	V_{REFHx}		3.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		 1 0		 32 32	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2.0		5.5	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	-0.3		0.8	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DDA} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
DAC Output Load Resistance	RLD		3K		—	ohms
DAC Output Load Capacitance	CLD		—		400	pF
Output Source Current High at V_{OH} min.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -4 -8	mA
Output Source Current Low (at V_{OL} max.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 4 8	mA
Ambient Operating Temperature (Extended Industrial)	T_A		-40		105	°C
Flash Endurance (Program Erase Cycles)	N_F	T_A = -40°C to 125°C	10,000		—	cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15		—	years
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	years

1. Total chip source or sink current cannot exceed 75mA

Note: Pin groups are detailed following **Table 10-1**

Table 11-1 56F8037/56F8027 64-Pin LQFP Package Identification by Pin Number[1]

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	**GPIOB6** *RXD0 / SDA / CLKIN*	17	**V_{SSA}**	33	**GPIOB2** *MISO0 / TA2 / PSRC0*	49	**V_{CAP}**
2	**GPIOB1** *$\overline{SS0}$ / SDA*	18	**GPIOD6** *DAC0*	34	**GPIOA6** *FAULT0 / TA0*	50	**V_{DD}**
3	**GPIOB7** *TXD0 / SCL*	19	**GPIOC3** *ANA3 / V_{REFLA}*	35	**GPIOA10** *TB2 / CMPAI2*	51	**V_{SS}**
4	**GPIOB5** *TA1 / FAULT3 / CLKIN*	20	**GPIOC2** *ANA2 / V_{REFHA}*	36	**GPIOA8** *FAULT1 / TA2 / CMPAI1*	52	**GPIOD5** *XTAL / CLKIN*
5	**GPIOA9** *FAULT2 / TA3 / CMPBI1*	21	**GPIOC9** *ANA5*	37	**GPIOA12** *SCLK1 / TB1 / TA1*	53	**GPIOD4** *EXTAL*
6	**GPIOA11** *TB3 / CMPBI2*	22	**GPIOC1** *ANA1*	38	**GPIOB4** *$\overline{SS1}$ / TB0 / TA0 / PSRC2 / CLKO*	54	**GPIOB8** *SCL / CANTX*
7	**VDD**	23	**GPIOC10** *ANA6*	39	**GPIOA5** *PWM5 / TA3 / FAULT2*	55	**GPIOA1** *PWM1*
8	**VSS**	24	**GPIOC0** *ANA0 & CMPAI3*	40	**V_{SS}**	56	**GPIOA0** *PWM0*
9	**GPIOC12** *ANB4 / RXD1*	25	**GPIOC11** *ANA7*	41	**V_{DD}**	57	**GPIOB12** *CANTX*
10	**GPIOC4** *ANB0 & CMPBI3*	26	**GPIOC8** *ANA4 / TXD1*	42	**GPIOB0** *SCLK0 / SCL*	58	**GPIOB13** *CANRX*
11	**GPIOC5** *ANB1*	27	**V_{SS}**	43	**GPIOA4** *PWM4 / TA2 / FAULT1*	59	**TDI** *GPIOD0*
12	**GPIOC13** *ANB5*	28	**V_{CAP}**	44	**GPIOA13** *MISO1 / TB2 / TA2*	60	**GPIOB11** *TB1 / CMPBO*
13	**GPIOC6** *ANB2 / V_{REFHB}*	29	**TCK** *GPIOD2*	45	**GPIOA14** *MOSI1 / TB3 / TA3*	61	**GPIOC15** *ANB7*
14	**GPIOC7** *ANB3 / V_{REFLB}*	30	**GPIOB10** *TB0 / CMPAO*	46	**GPIOB9** *SDA / CANRX*	62	**GPIOC14** *ANB6*
15	**GPIOD7** *DAC1*	31	**$\overline{RESET}$** *GPIOA7*	47	**GPIOA2** *PWM2*	63	**TMS** *GPIOD3*
16	**V_{DDA}**	32	**GPIOB3** *MOSI0 / TA3 / PSRC1*	48	**GPIOA3** *PWM3*	64	**TDO** *GPIOD1*

1. Alternate signals are in italic

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8037/56F8027:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the 56F8037/56F8027 and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible
- Bypass the V_{DD} and V_{SS} with approximately 100µF, plus the number of 0.1µF ceramic capacitors
- PCB trace lengths should be minimal for high-frequency signals
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Pulse Width Modulator (PWM) Module							
Control Register	CTRL	PMCTL	PWM_CTRL	PWM_PMCTL	PWM_PMCTL	0xF0C0	
Fault Control Register	FCTRL	PMFCTL	PWM_FCTRL	PWM_PMFCTL	PWM_PMFCTL	0xF0C1	
Fault Status/Acknowledge Regis.	FLTACK	PMFSA	PWM_FLTACK	PWM_PMFSA	PWM_PMFSA	0xF0C2	
Output Control Register	OUT	PMOUT	PWM_OUT	PWM_PMOUT	PWM_PMOUT	0xF0C3	
Counter Register	CNTR	PMCNT	PWM_CNTR	PWM_PMCNT	PWM_PMCNT	0xF0C4	
Counter Modulo Register	CMOD	MCM	PWM_CMOD	PWM_MCM	PWM_MCM	0xF0C5	
Value 0-5 Registers	VAL0-5	PMVAL0-5	PWM_VAL0-5	PWM_PMVAL0-5	PWM_PMVAL0-5	0xF0C6	0xF0CB
Deadtime 0-1 Registers	DTIM0-1	PMDEADTM0-1	PWM_DTIM0-1	PWM_PMDEADTM0-1	PWM_PMDEADTM0-1	0xF0CC	0xF0CD
Disable Mapping 1-2 Registers	DMAP1-2	PMDISMAP1-2	PWM_DMAP1-2	PWM_PMDISMAP1-2	PWM_PMDISMAP1-2	0xF0CE	0xF0CF
Configure Register	CNFG	PMCFG	PWM_CNFG	PWM_PMCFG	PWM_PMCFG	0xF0D0	
Channel Control Register	CCTRL	PMCCR	PWM_CCTRL	PWM_PMCCR	PWM_PMCCR	0xF0D1	
Port Register	PORT	PMPORT	PWM_PORT	PWM_PMPORT	PWM_PMPORT	0xF0D2	
Internal Correction Control Register	ICCTRL	PMICCR	PWM_ICCTRL	PWM_PMICCR	PWM_PMICCR	0xF0D3	
Source Control Register	SCTRL	PMSRC	PWM_SCTRL	PWM_PMSRC	PWM_PMSRC	0xF0D4	
Synchronization Window Register	SYNC		PWM_SYNC	PWM_SYNC	PWM_SYNC	0xF0D5	
Fault Filter 0-3 Register	FFILT0-3		PWM_FFILT0-3	PWM_FFILT0-3	PWM_FFILT0-3	0xF0D6	0xF0D9
Multi-Scalable Controller Area Network (MSCAN) Module							
Control 0 Register	CTRL0		CAN_CTRL0		CANCTRL0	0XF800	
Control 1 Register	CTRL1		CAN_CTRL1		CANCTRL1	0XF801	
Bus Timing 0 Register	BTR0		CAN_BTR0		CANBTR0	0XF802	
Bus Timing 1 Register	BTR1		CAN_BTR1		CANBTR1	0XF803	
Receive Flag Register	RFLG		CAN_RFLG		CANRFLG	0XF804	
Receiver Interrupt Enable Register	RIER		CAN_RIER		CANRIER	0XF805	
Transmitter Flag Register	TFLG		CAN_TFLG		CANTFLG	0XF806	
Transmitter Interrupt Enable Register.	TIER		CAN_TIER		CANTIER	0XF807	
Transmitter Msg Abort Request Register	TARQ		CAN_TARQ		CANTARQ	0XF808	

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MC56F8037
Rev. 8
04/2012