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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1516-e-sp

PIC16(L)F151X/152X

1.2 Pin Utilization

Five pins are needed for ICSP™ programming. The pins are listed in [Table 1-1](#) and [Table 1-2](#).

TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING – PIC16(L)F1526 AND PIC16(L)F1527

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RG5/ $\overline{\text{MCLR}}$ /VPP	Program/Verify mode	P ⁽¹⁾	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{\text{MCLR}}$ input. Since the $\overline{\text{MCLR}}$ is used for a level source, $\overline{\text{MCLR}}$ does not draw any significant current.

TABLE 1-2: PIN DESCRIPTIONS DURING PROGRAMMING – PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516, PIC16(L)F1517, PIC16(L)F1518 and PIC16(L)F1519

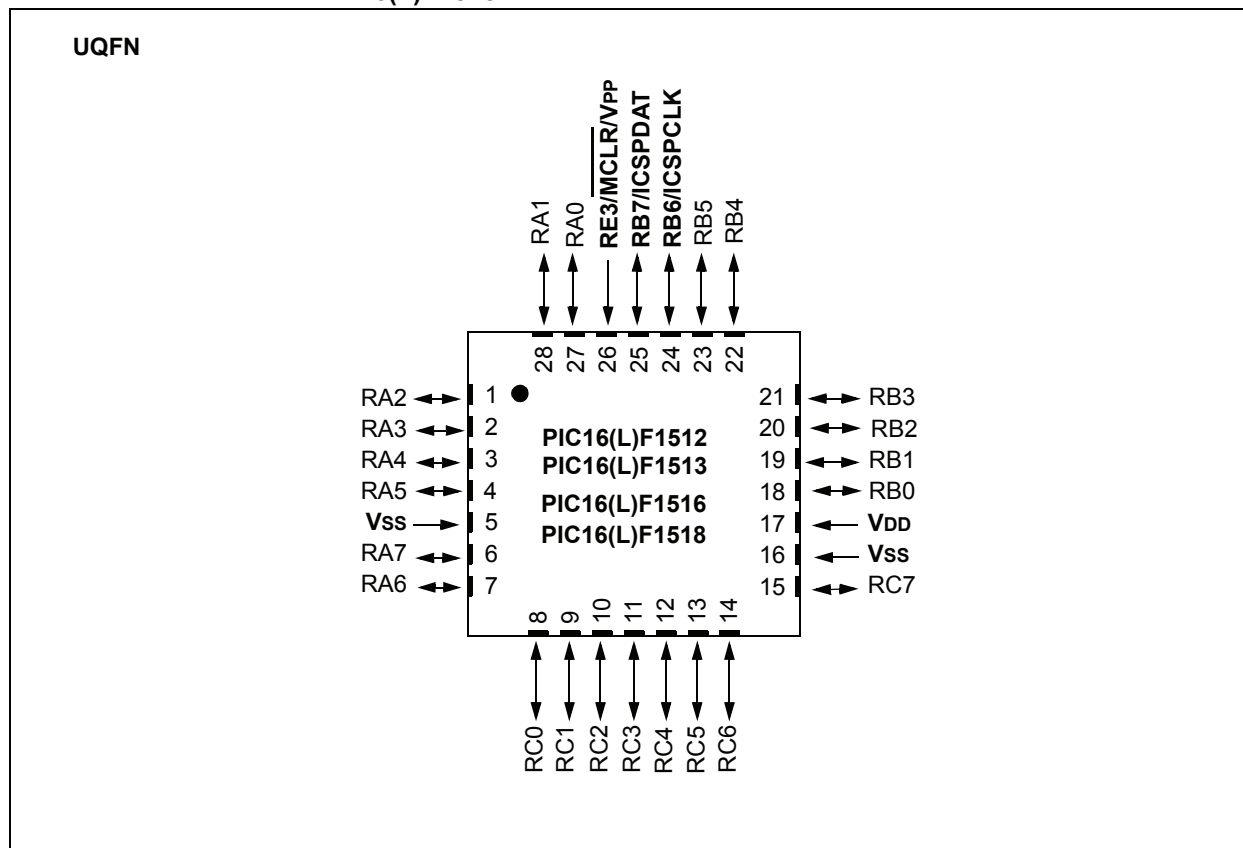
Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RE3/ $\overline{\text{MCLR}}$ /VPP	Program/Verify mode	P ⁽¹⁾	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{\text{MCLR}}$ input. Since the $\overline{\text{MCLR}}$ is used for a level source, $\overline{\text{MCLR}}$ does not draw any significant current.

PIC16(L)F151X/152X

FIGURE 2-2: 28-PIN UQFN DIAGRAM FOR PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516 AND PIC16(L)F1518



PIC16(L)F151X/152X

FIGURE 2-5: 44-PIN TQFP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519

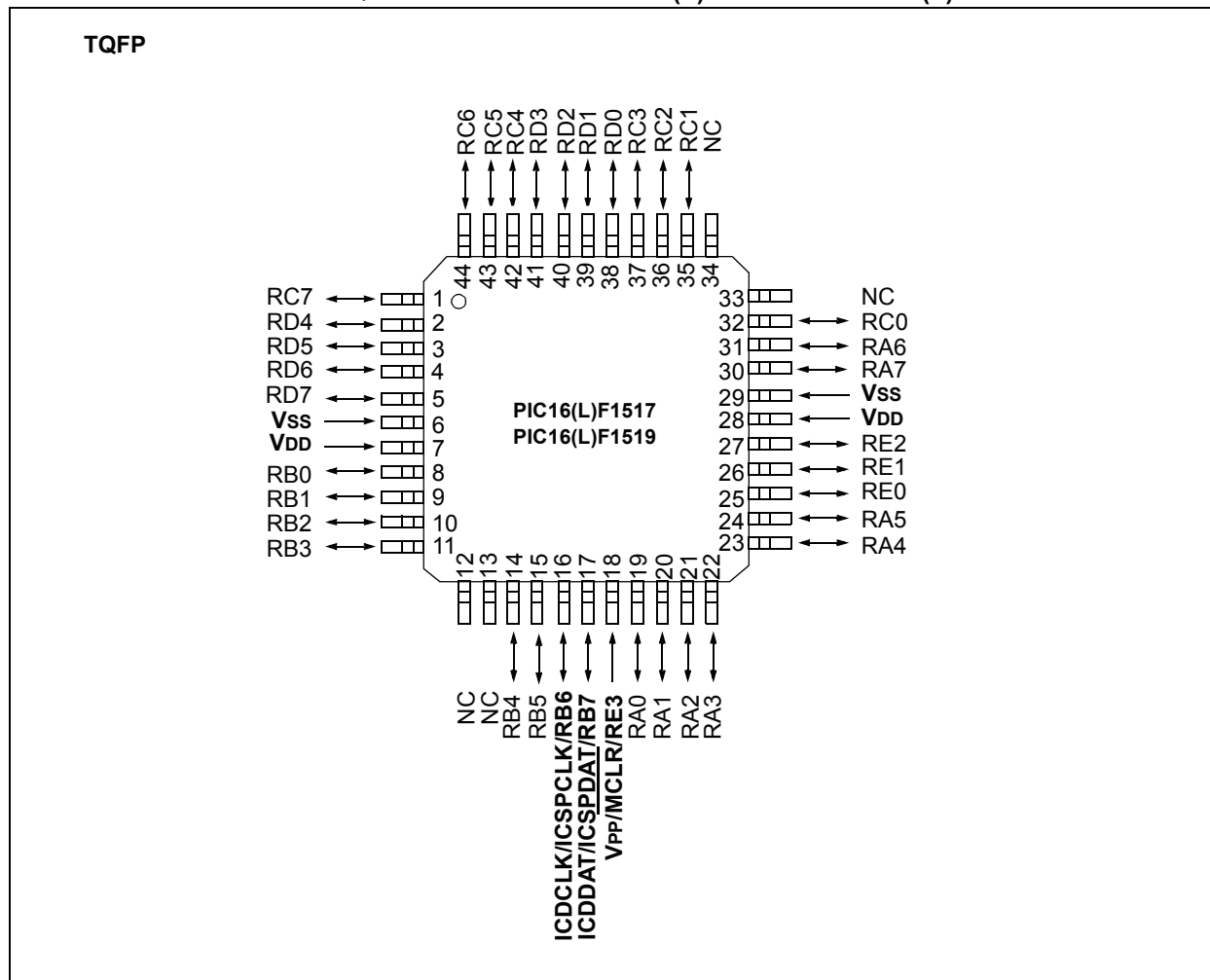
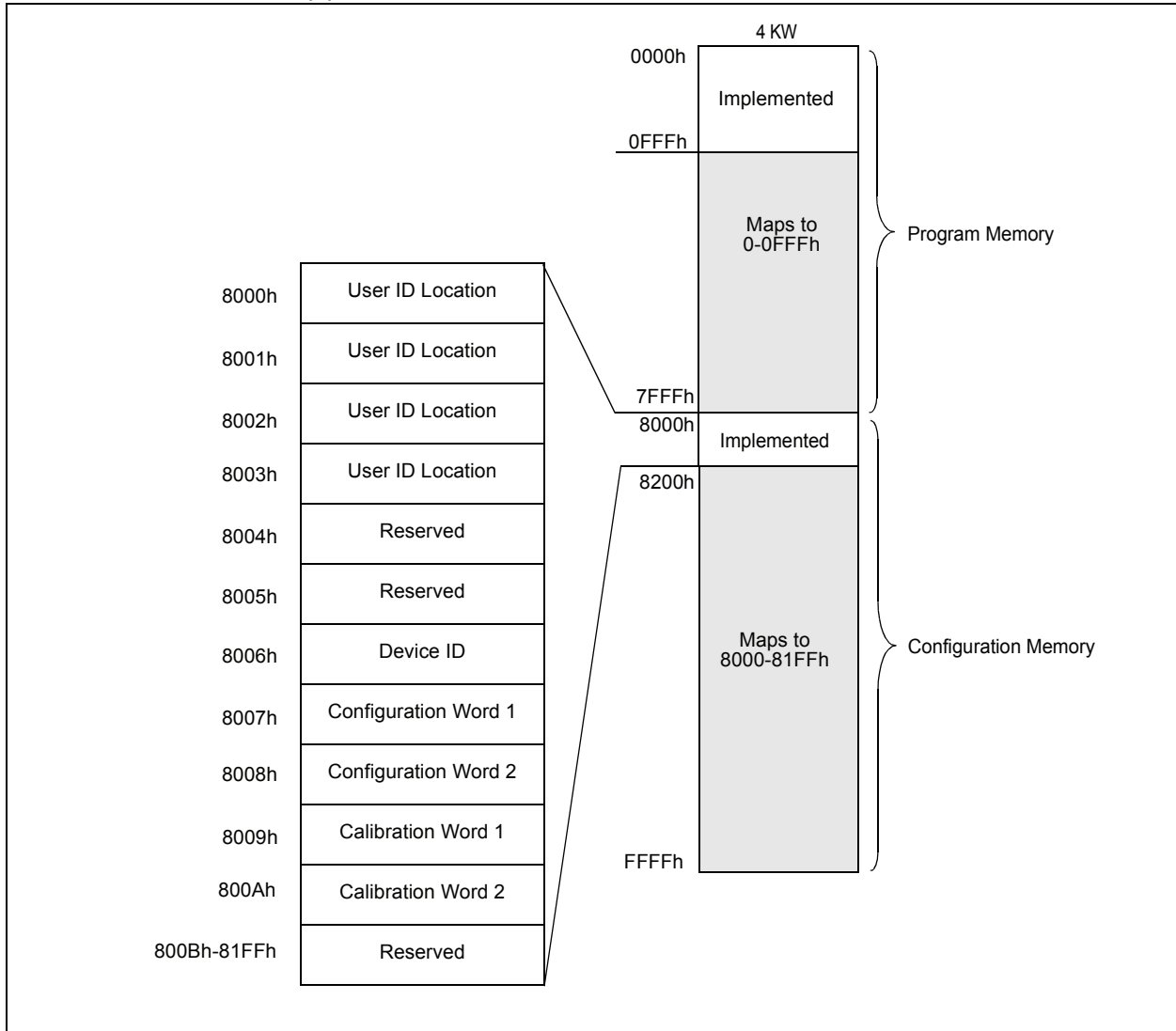


FIGURE 3-2: PIC16(L)F1513 PROGRAM MEMORY MAPPING



PIC16(L)F151X/152X

FIGURE 3-3: PIC16(L)F1526, PIC16(L)F1516 AND PIC16(L)F1517 PROGRAM MEMORY MAPPING

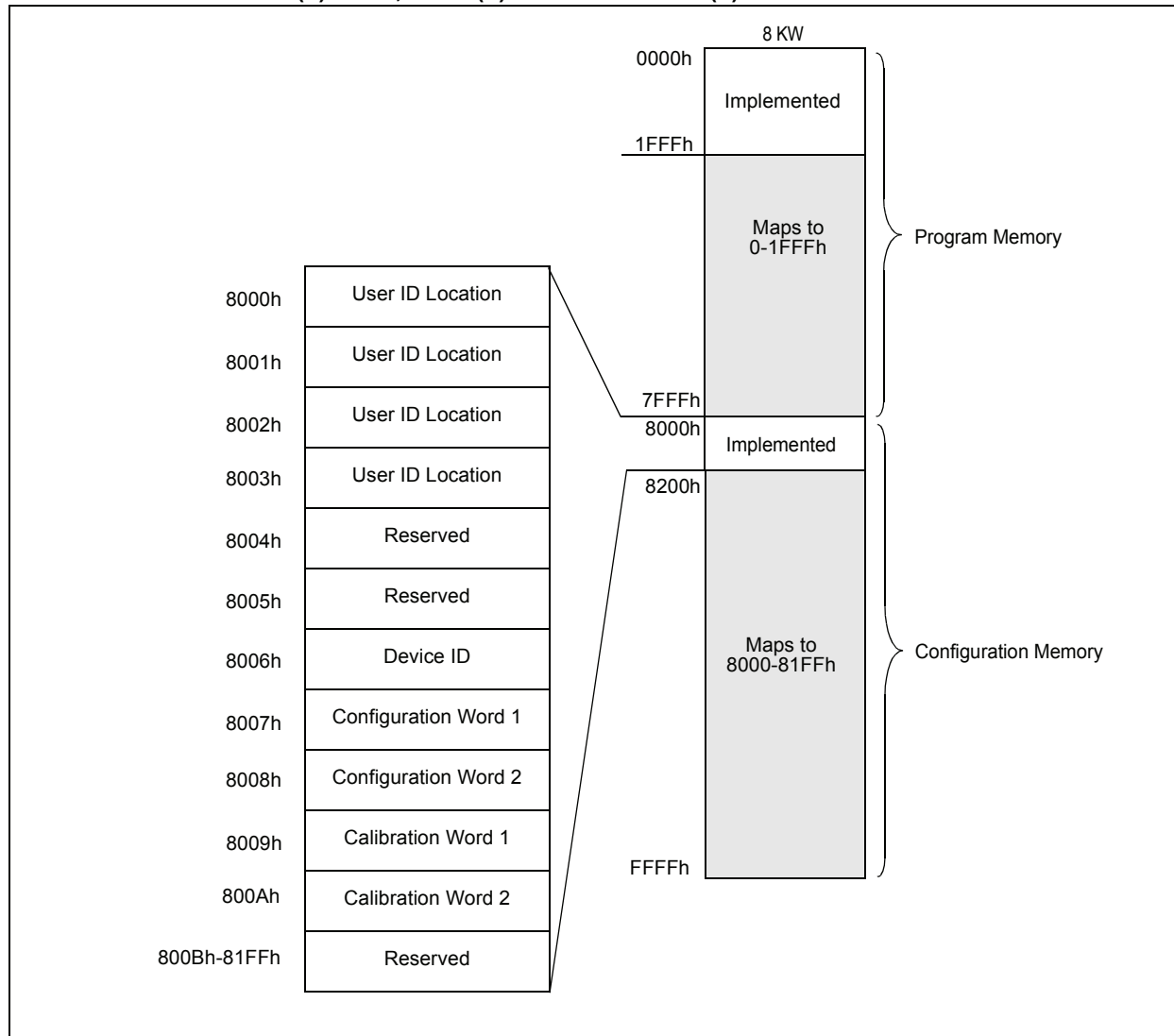
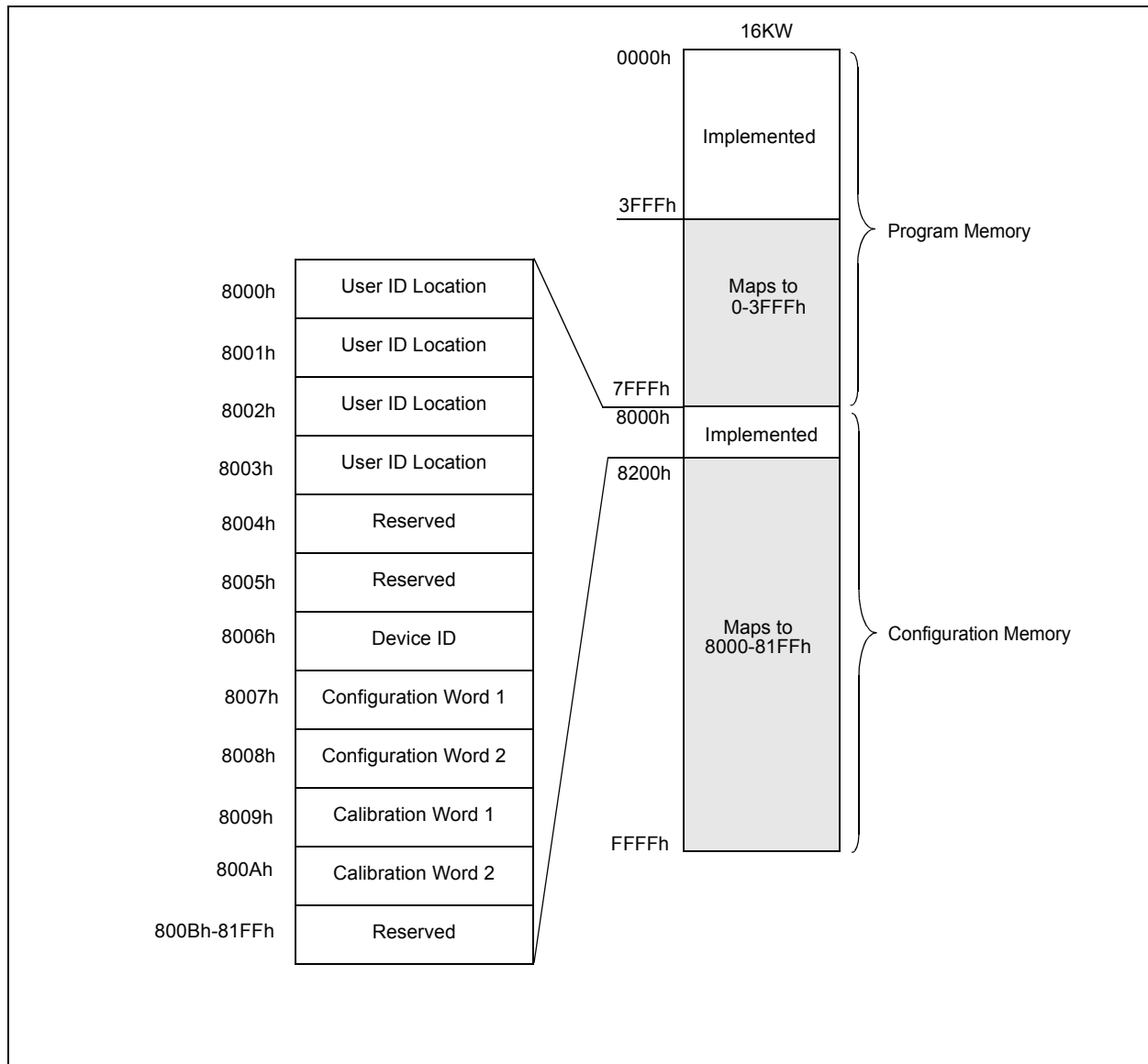


FIGURE 3-4: PIC16(L)F1527, PIC16(L)F1518 AND PIC16(L)F1519 PROGRAM MEMORY MAPPING



REGISTER 3-3: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
LVP	DEBUG	LPBOR	BORV	STVREN	—
bit 13					bit 8

U-1	U-1	U-1	R/P-1	U-1	U-1	R/P-1	R/P-1
—	—	—	VCAPEN ⁽²⁾	—	—	WRT<1:0>	
bit 7							bit 0

Legend:

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '1'

'0' = Bit is cleared

'1' = Bit is set

-n = Value when blank or after Bulk Erase

- bit 13 **LVP:** Low-Voltage Programming Enable bit⁽¹⁾
1 = Low-voltage programming enabled
0 = HV on MCLR/VPP must be used for programming
- bit 12 **DEBUG:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
0 = In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger
- bit 11 **LPBOR:** Low-Power BOR
1 = Low-Power BOR is disabled
0 = Low-Power BOR is enabled
- bit 10 **BORV:** Brown-out Reset Voltage Selection bit
1 = Brown-out Reset voltage (VBOR), low trip point selected
0 = Brown-out Reset voltage (VBOR), high trip point selected
- bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
1 = Stack Overflow or Underflow will cause a Reset
0 = Stack Overflow or Underflow will not cause a Reset
- bit 8-5 **Unimplemented:** Read as '1'
- bit 4 **VCAPEN:** Voltage Regulator Capacitor Enable bits⁽¹⁾
0 = VCAP functionality is enabled on VCAP pin
1 = All VCAP pin functions are disabled
- bit 3-2 **Unimplemented:** Read as '1'
- bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits
2 kW Flash memory (PIC16(L)F1512):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
01 = 000h to FFFh write-protected, 400h to 7FFh may be modified by PMCON control
00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control
4 kW Flash memory (PIC16(L)F1513):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control
01 = 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control
00 = 000h to FFFh write-protected, no addresses may be modified by PMCON control
8 kW Flash memory (PIC16F/LF1516/1517/1526):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 1FFFh may be modified by PMCON control
01 = 000h to FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control
00 = 000h to 1FFFh write-protected, no addresses may be modified by PMCON control
16 kW Flash memory (PIC16F/LF1518/1519/1527):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 3FFFh may be modified by PMCON control
01 = 000h to 1FFFh write-protected, 2000h to 3FFFh may be modified by PMCON control
00 = 000h to 3FFFh write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.

Note 2: Applies to PIC16F151X/152X devices only. On PIC16LF151X/152X, the VCAPEN bit is unimplemented.

PIC16(L)F151X/152X

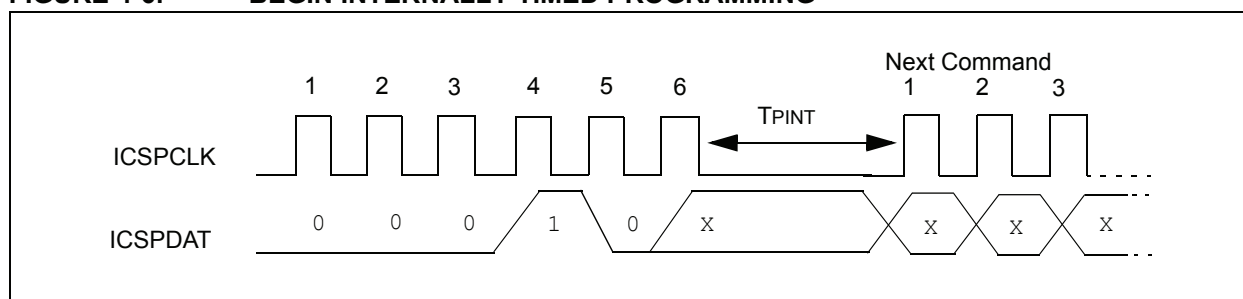
4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, T_{PINT} , for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed.

FIGURE 4-6: BEGIN INTERNALLY TIMED PROGRAMMING

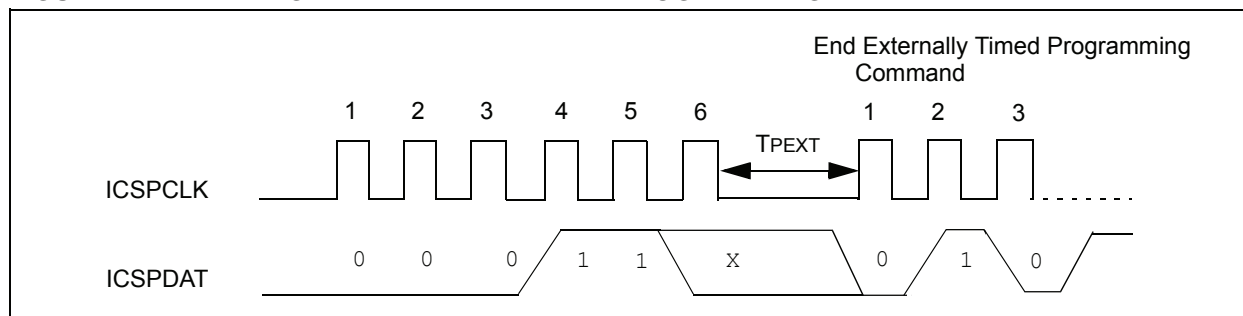


4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming the End Externally Timed Programming command must be sent in the specified time window defined by T_{PEXT} (see [Figure 4-7](#)).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 4-7: BEGIN EXTERNALLY TIMED PROGRAMMING

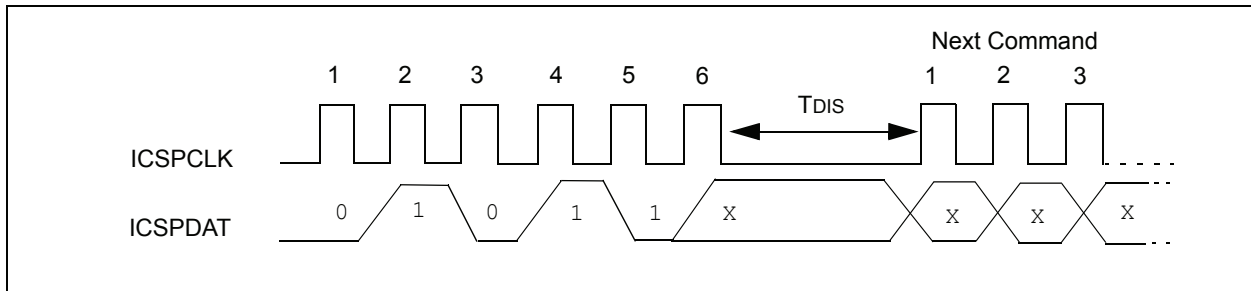


4.3.8 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPEXT after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 4-8).

FIGURE 4-8: END EXTERNALLY TIMED PROGRAMMING



4.3.9 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-7FFFh:

- Program Memory is erased
- Configuration Words are erased

Address 8000h-8008h:

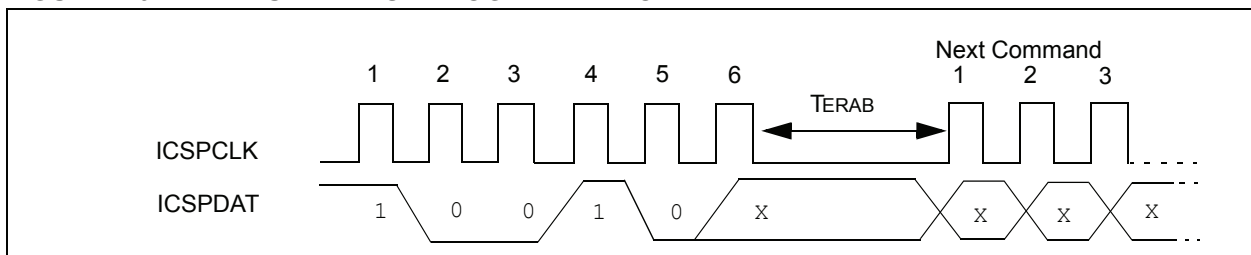
- Program Memory is erased
- Configuration Words are erased
- User ID Locations are erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

After receiving the Bulk Erase Program Memory command the erase will not complete until the time interval, TERAB, has expired.

Note: The code protection Configuration bit (CP) has no effect on the Bulk Erase Program Memory command.

FIGURE 4-9: BULK ERASE PROGRAM MEMORY



5.0 PROGRAMMING ALGORITHMS

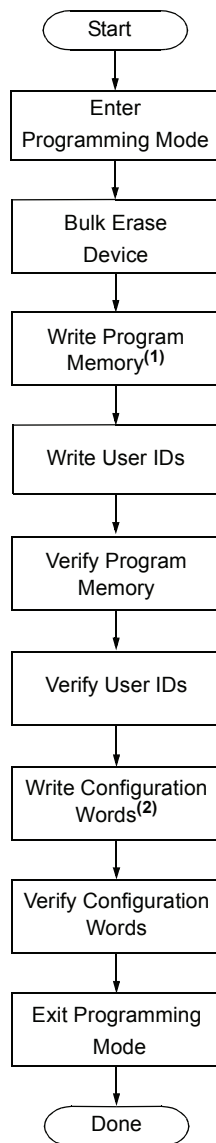
The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to [Table 4-2](#) for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC's address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes cannot cross the physical boundary. For example, with the PIC16F1527, attempting to write from address 0002h-0009h will result in data being written to 0008h-000Fh.

If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

PIC16(L)F151X/152X

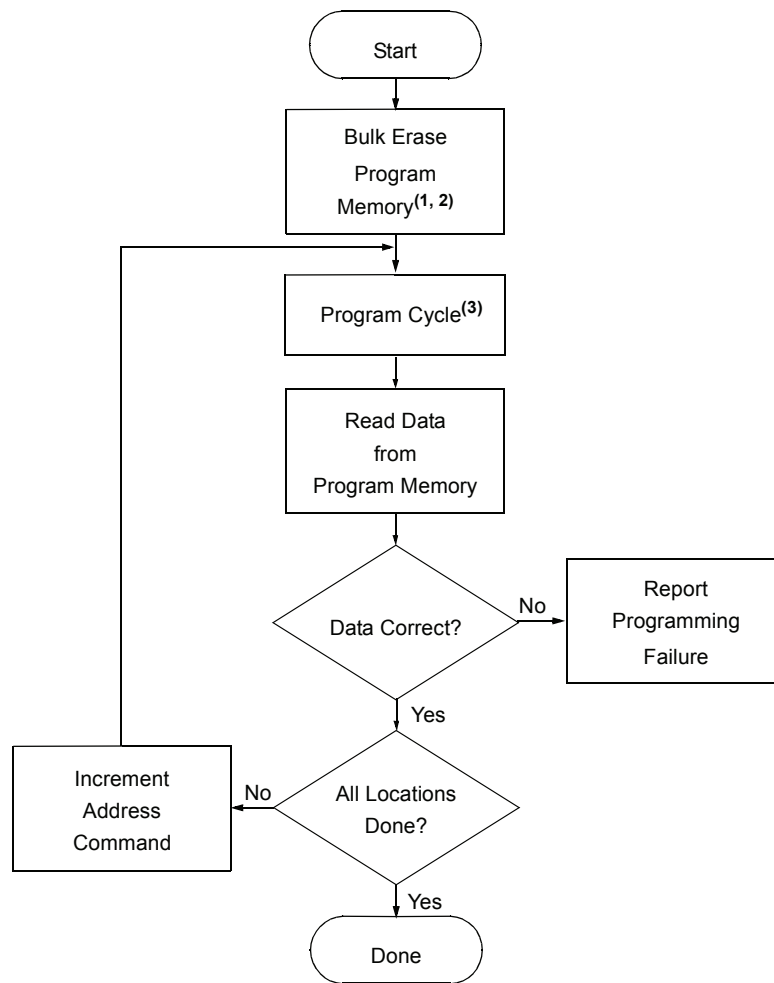
FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART



Note 1: See [Figure 5-2](#).

2: See [Figure 5-5](#).

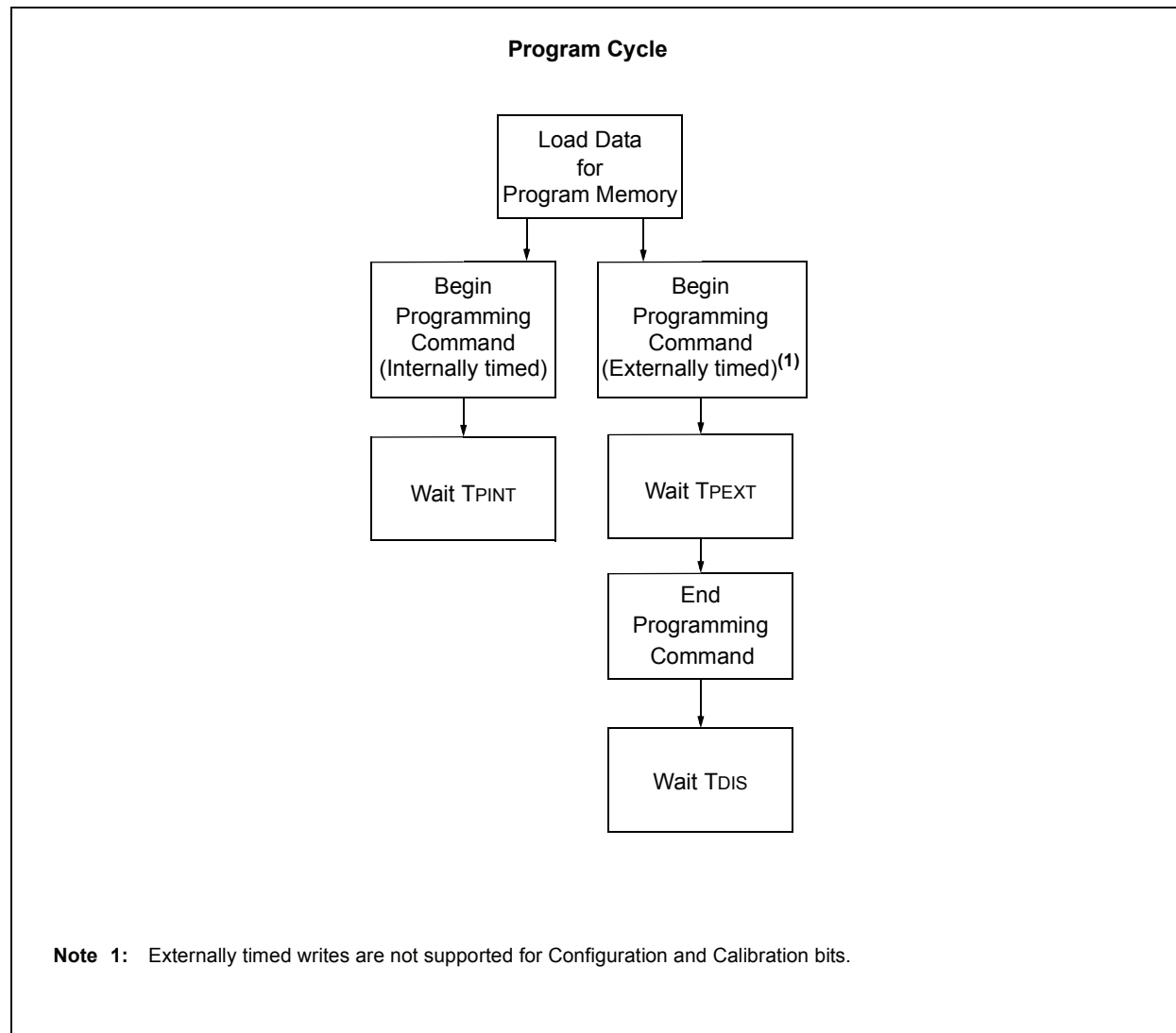
FIGURE 5-2: PROGRAM MEMORY FLOWCHART



- Note 1:** This step is optional if device has already been erased or has not been previously programmed.
Note 2: If the device is code-protected or must be completely erased, then Bulk Erase device per [Figure 5-6](#).
Note 3: See [Figure 5-3](#) or [Figure 5-4](#).

PIC16(L)F151X/152X

FIGURE 5-3: ONE-WORD PROGRAM CYCLE



7.3 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the \overline{CP} Configuration bit.

TABLE 7-1: CONFIGURATION WORD MASK VALUES

Device	Config. Word 1 Mask	Config. Word 2 Mask
PIC16F1512	3EFFh	3E13h
PIC16F1513	3EFFh	3E13h
PIC16F1516	3EFFh	3E13h
PIC16F1517	3EFFh	3E13h
PIC16F1518	3EFFh	3E13h
PIC16F1519	3EFFh	3E13h
PIC16LF1512	3EFFh	3E03h
PIC16LF1513	3EFFh	3E03h
PIC16LF1516	3EFFh	3E03h
PIC16LF1517	3EFFh	3E03h
PIC16LF1518	3EFFh	3E03h
PIC16LF1519	3EFFh	3E03h
PIC16F1526	3EFFh	3E13h
PIC16F1527	3EFFh	3E13h
PIC16LF1526	3EFFh	3E03h
PIC16LF1527	3EFFh	3E03h

7.3.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the PIC16(L)F151X/152X program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location. Any Carry bit exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

PIC16(L)F151X/152X

EXAMPLE 7-1: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED PIC16F1527, BLANK DEVICE

PIC16F1527	Sum of Memory addresses 0000h-3FFFh ⁽¹⁾	C000h
	Configuration Word 1 ⁽²⁾	3FFFh
	Configuration Word 1 mask ⁽³⁾	3EFFh
	Configuration Word 2 ⁽²⁾	3FFFh
	Configuration Word 2 mask ⁽³⁾	3E13h
	Checksum	= C000h + (3FFFh and 3EFFh) + (3FFFh and 3E13h)
		= C000h + 3EFFh + 3E13h
		= 3D12h

- Note 1:** Sum of memory addresses = (Total number of program memory address locations) x (3FFFh) = C000h, truncated to 16 bits.
- 2:** Configuration Word 1 and 2 = all bits are '1'; thus, code-protect is disabled.
- 3:** Configuration Word 1 and 2 Mask = all bits are set to '1', except for unimplemented bits that are '0'.

EXAMPLE 7-2: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED PIC16LF1527, 00AAh AT FIRST AND LAST ADDRESS

PIC16LF1527	Sum of Memory addresses 0000h-3FFFh ⁽¹⁾	4156h
	Configuration Word 1 ⁽²⁾	3FFFh
	Configuration Word 1 mask ⁽³⁾	3EFFh
	Configuration Word 2 ⁽²⁾	3FFFh
	Configuration Word 2 mask ⁽⁴⁾	3E03h
	Checksum	= 4156h + (3FFFh and 3EFFh) + (3FFFh and 3E03h)
		= 4156h + 3EFFh + 3E03h
		= BE58h

- Note 1:** Total number of Program memory address locations: 3FFFh + 1 = 4000h. Then, 4000h - 2 = 3FFEh. Thus, [(3FFEh x 3FFFh) + (2 x 00AAh)] = 4156h, truncated to 16 bits.
- 2:** Configuration Word 1 and 2 = all bits are '1'; thus, code-protect is disabled.
- 3:** Configuration Word 1 Mask = all Configuration Word bits are set to '1', except for unimplemented bits that are '0'.
- 4:** On the PIC16LF1527 device, the $\overline{\text{VCAPEN}}$ bit is not implemented in Configuration Word 2; Thus, all unimplemented bits are '0'.

7.3.2 PROGRAM CODE PROTECTION ENABLED

With the program code protection enabled, the checksum is computed in the following manner: The Least Significant nibble of each user ID is used to create a 16-bit value. The masked value of user ID location 8000h is the Most Significant nibble. This sum of user IDs is summed with the Configuration Words (all unimplemented Configuration bits are masked to '0').

EXAMPLE 7-3: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC16F1527, BLANK DEVICE

PIC16F1527	Configuration Word 1 ⁽²⁾	3F7Fh
	Configuration Word 1 mask ⁽³⁾	3EFFh
	Configuration Word 2 ⁽²⁾	3FFFh
	Configuration Word 2 mask ⁽³⁾	3E13h
	User ID (8000h) ⁽¹⁾	0006h
	User ID (8001h) ⁽¹⁾	0007h
	User ID (8002h) ⁽¹⁾	0001h
	User ID (8003h) ⁽¹⁾	0002h
	Sum of User IDs ⁽⁴⁾	$= (0006h \text{ and } 000Fh) \ll 12 + (0007h \text{ and } 000Fh) \ll 8 +$ $(0001h \text{ and } 000Fh) \ll 4 + (0002h \text{ and } 000Fh)$ $= 6000h + 0700h + 0010h + 0002h$ $= 6712h$
	Checksum	$= (3F7Fh \text{ and } 3EFFh) + (3FFFh \text{ and } 3E13h) + \text{Sum of User IDs}$ $= 3E7Fh + 3713h + 6712h$ $= DCA4h$

Note 1: User ID values in this example are random values.

2: Configuration Word 1 and 2 = all bits are '1' except the code-protect enable bit.

3: Configuration Word 1 and 2 Mask = all Configuration Word bits are set to '1', except for unimplemented bits which read '0'.

4: << = shift left, thus the LSb of the first user ID value is the MSb of the sum of user IDs and so on, until the LSb of the last user ID value becomes the LSb of the sum of user IDs.

PIC16(L)F151X/152X

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
TPINT	Internally timed programming operation time	—	—	2.5 5	ms ms	Program memory Configuration Words
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms	Note 1
TDIS	Time delay from program to compare (HV discharge time)	300	—	—	μs	
TEXT	Time delay when exiting Program/Verify mode	1	—	—	μs	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – VDD FIRST

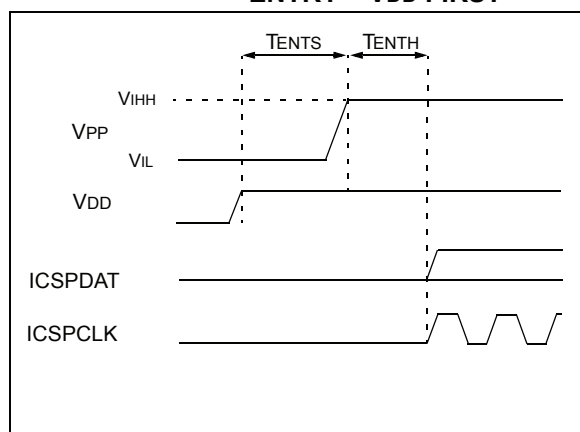


FIGURE 8-2: PROGRAMMING MODE ENTRY – VPP FIRST

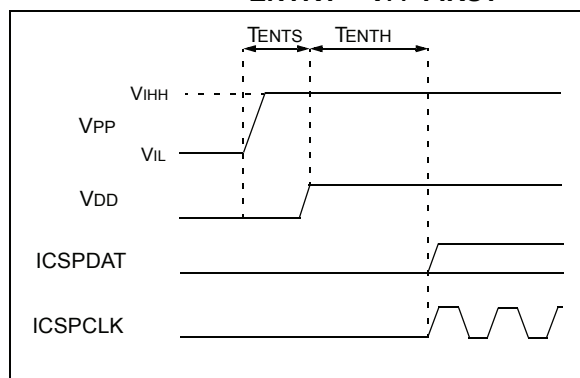


FIGURE 8-3: PROGRAMMING MODE EXIT – VPP LAST

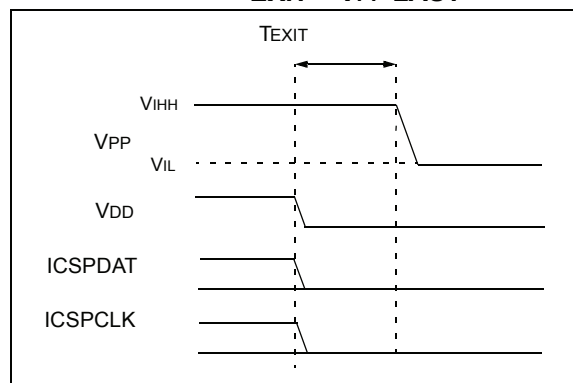
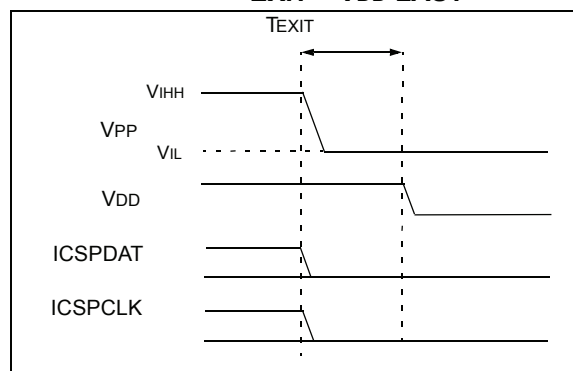


FIGURE 8-4: PROGRAMMING MODE EXIT – VDD LAST



PIC16(L)F151X/152X

FIGURE 8-8: LVP ENTRY (POWERED)

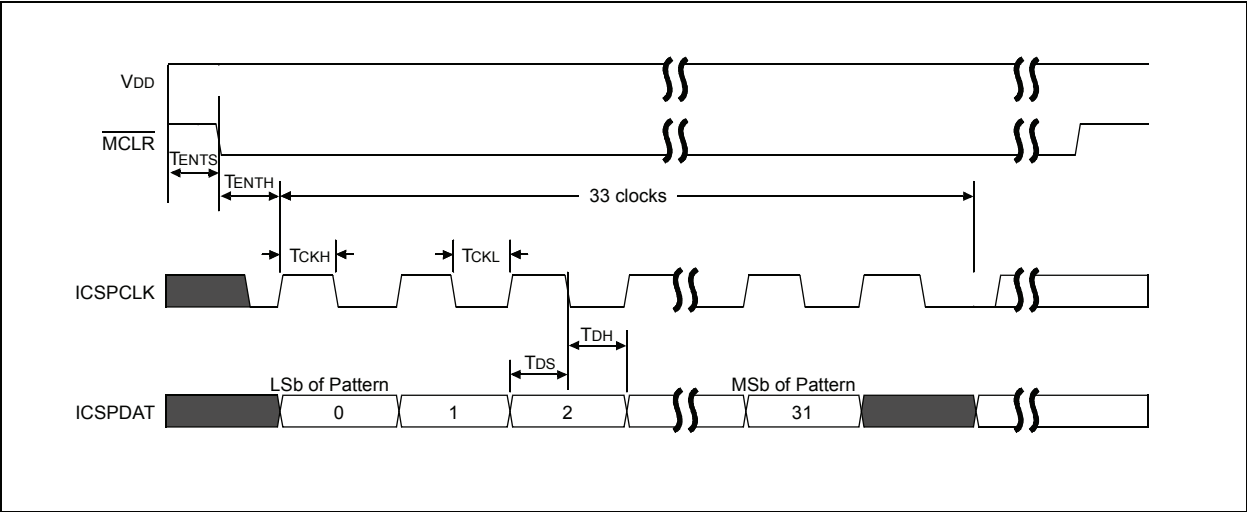
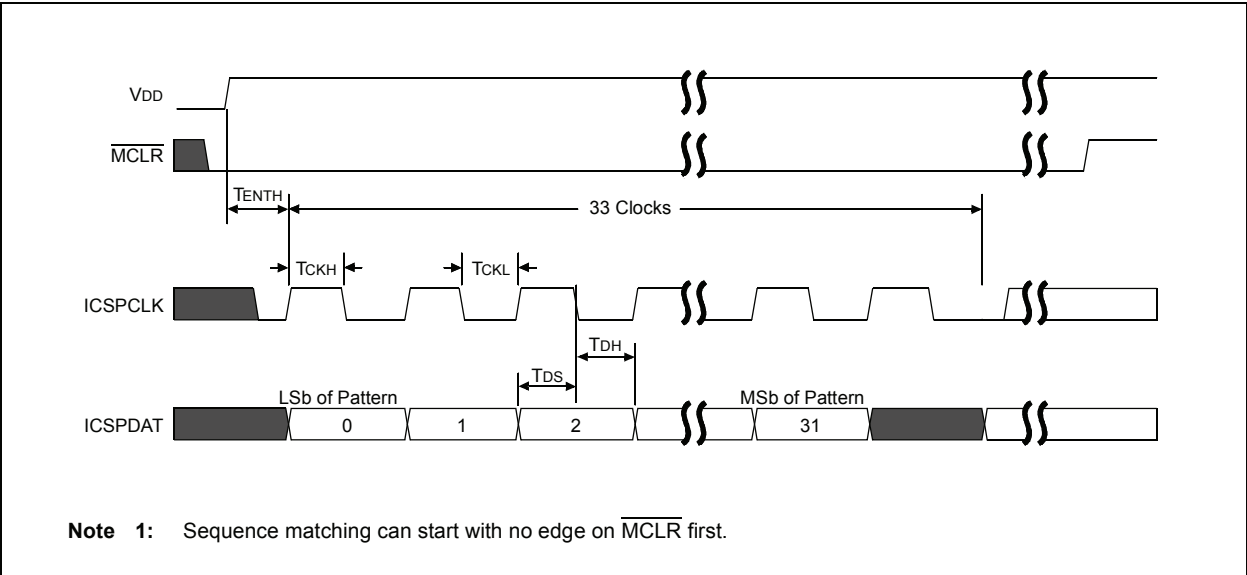


FIGURE 8-9: LVP ENTRY (POWERING UP)



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Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
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Fax: 886-3-5770-955

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Fax: 44-118-921-5820

08/02/11