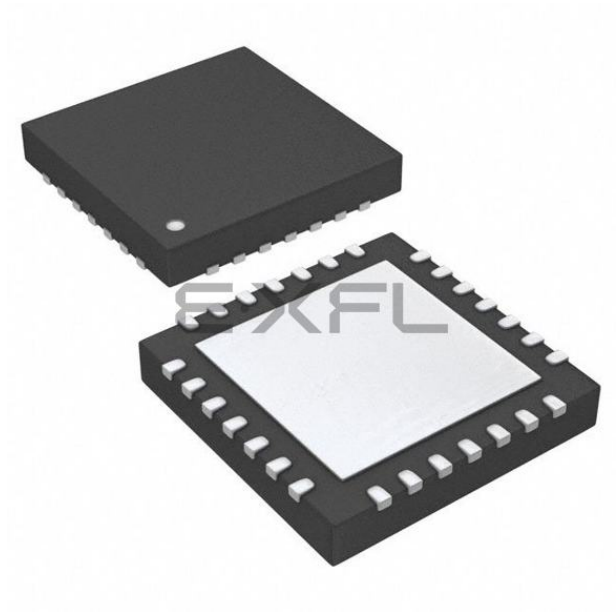

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1516-i-ml

1.2 Pin Utilization

Five pins are needed for ICSP™ programming. The pins are listed in Table 1-1 and Table 1-2.

TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING – PIC16(L)F1526 AND PIC16(L)F1527

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RG5/$\overline{MCLR}$/VPP	Program/Verify mode	P(1)	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

TABLE 1-2: PIN DESCRIPTIONS DURING PROGRAMMING – PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516, PIC16(L)F1517, PIC16(L)F1518 and PIC16(L)F1519

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RE3/$\overline{MCLR}$/VPP	Program/Verify mode	P(1)	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

2.0 DEVICE PINOUTS

The pin diagrams for the PIC16(L)F151X/152X family are shown in Figure 2-1 through Figure 2-7. The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagrams.

FIGURE 2-1: 28-PIN SPDIP, SOIC, SSOP DIAGRAM FOR PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516 AND PIC16(L)F1518

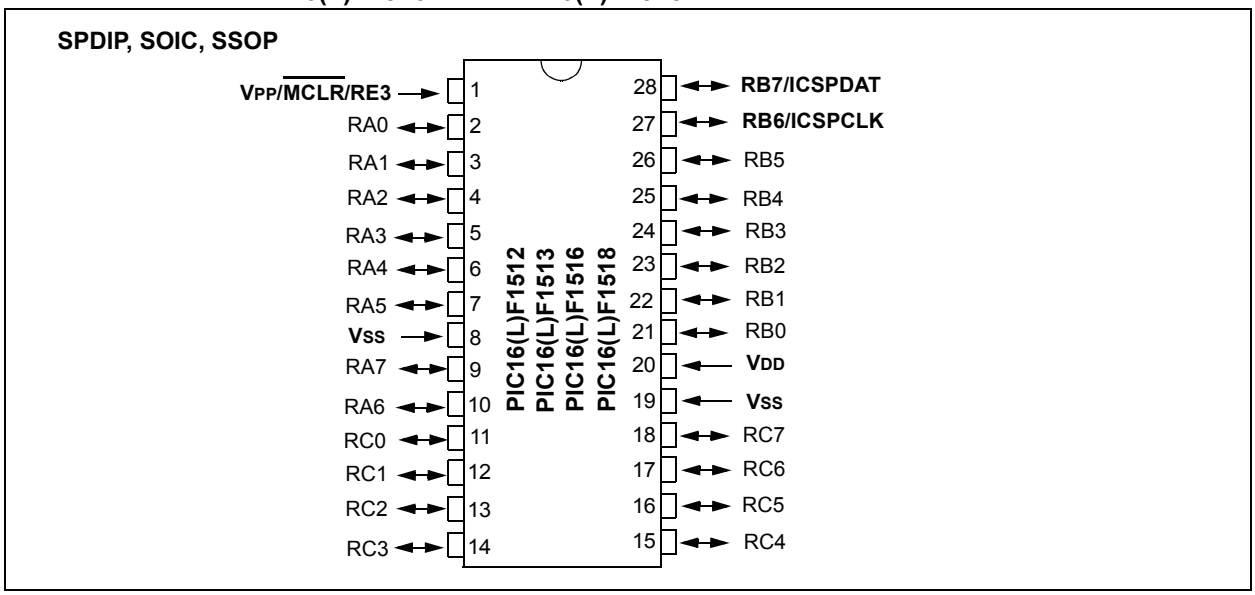


FIGURE 2-3: 40-PIN PDIP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519

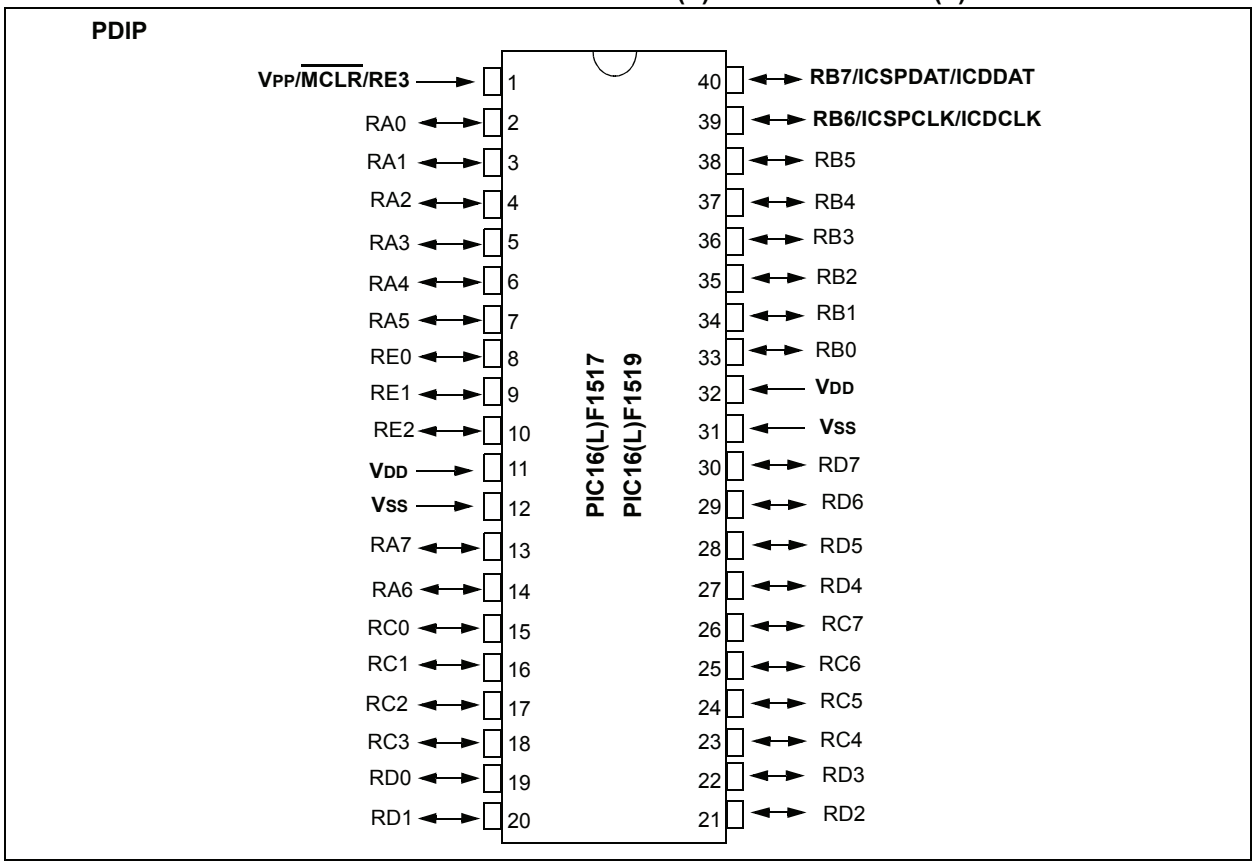


FIGURE 2-4: 40-PIN UQFN DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519

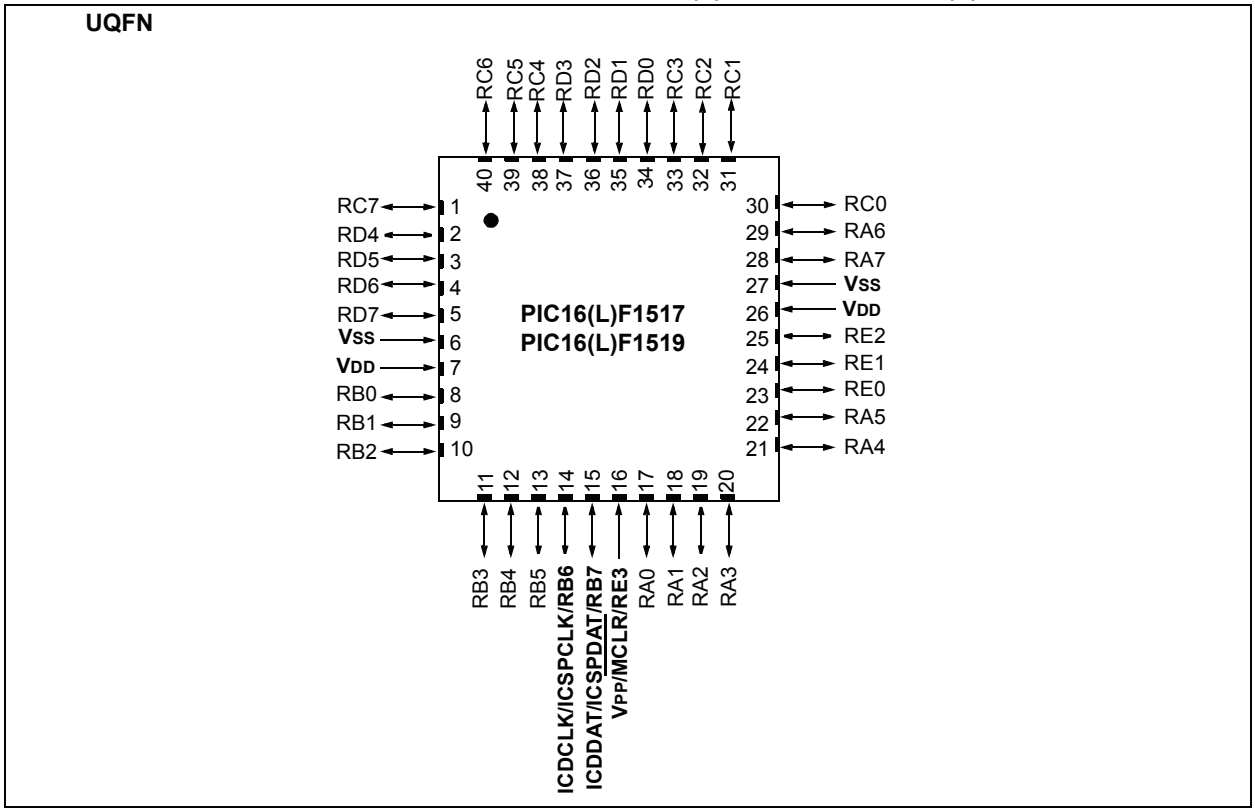


FIGURE 2-5: 44-PIN TQFP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519

TQFP

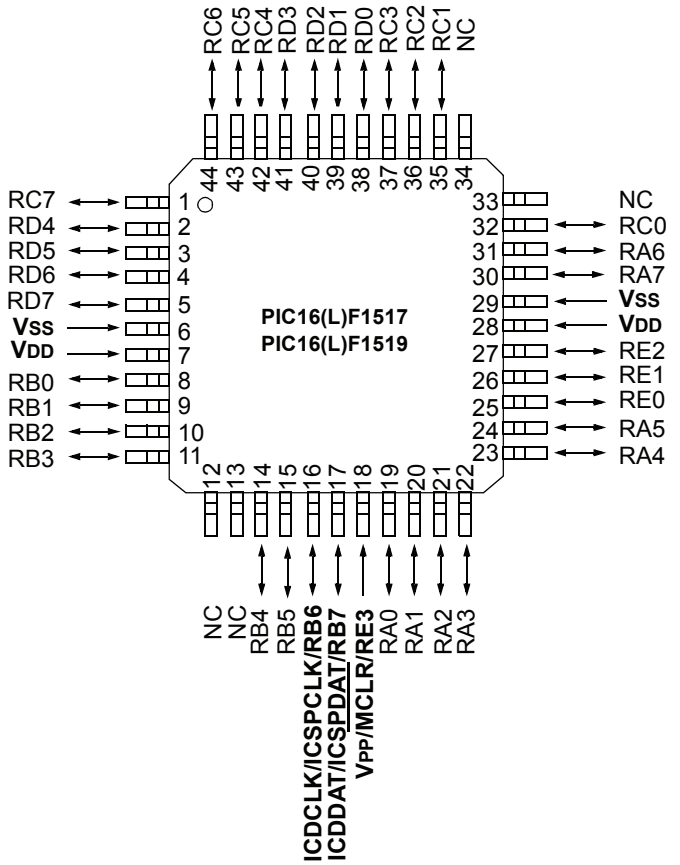


FIGURE 2-6: 64-PIN QFN DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527

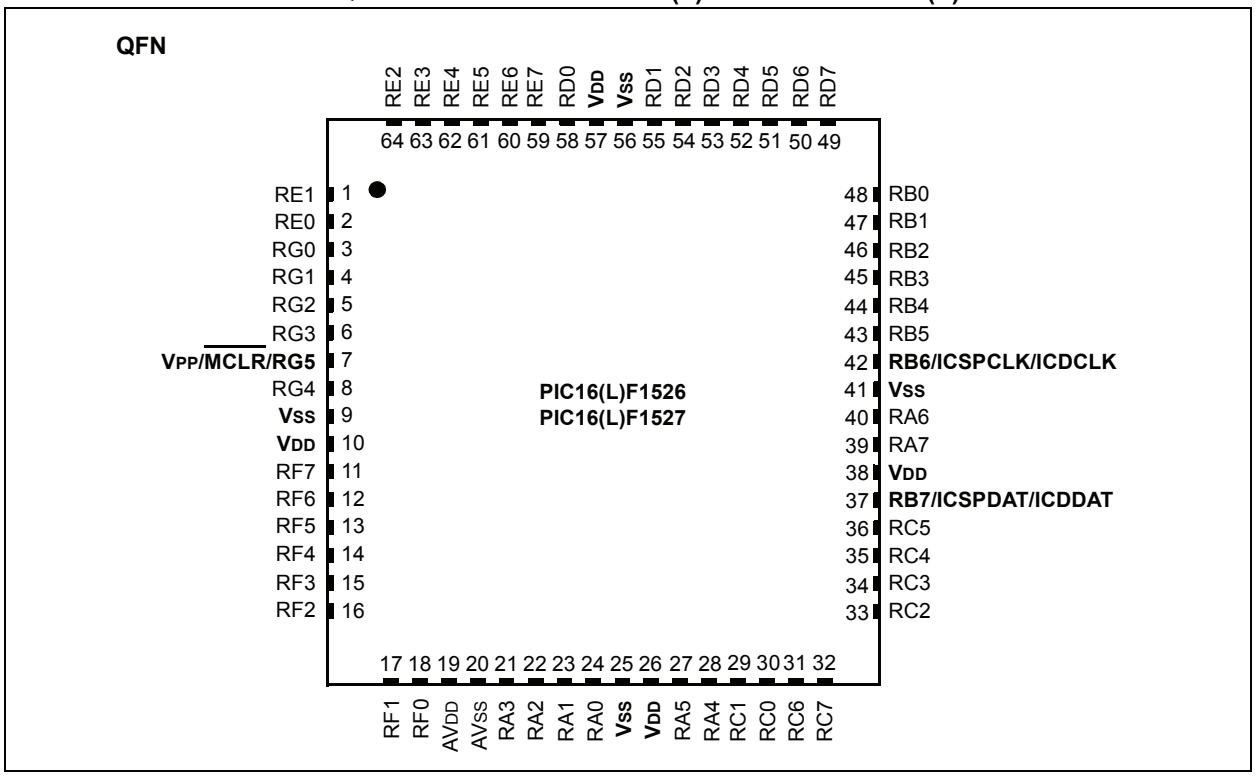


FIGURE 2-7: 64-PIN TQFP DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527

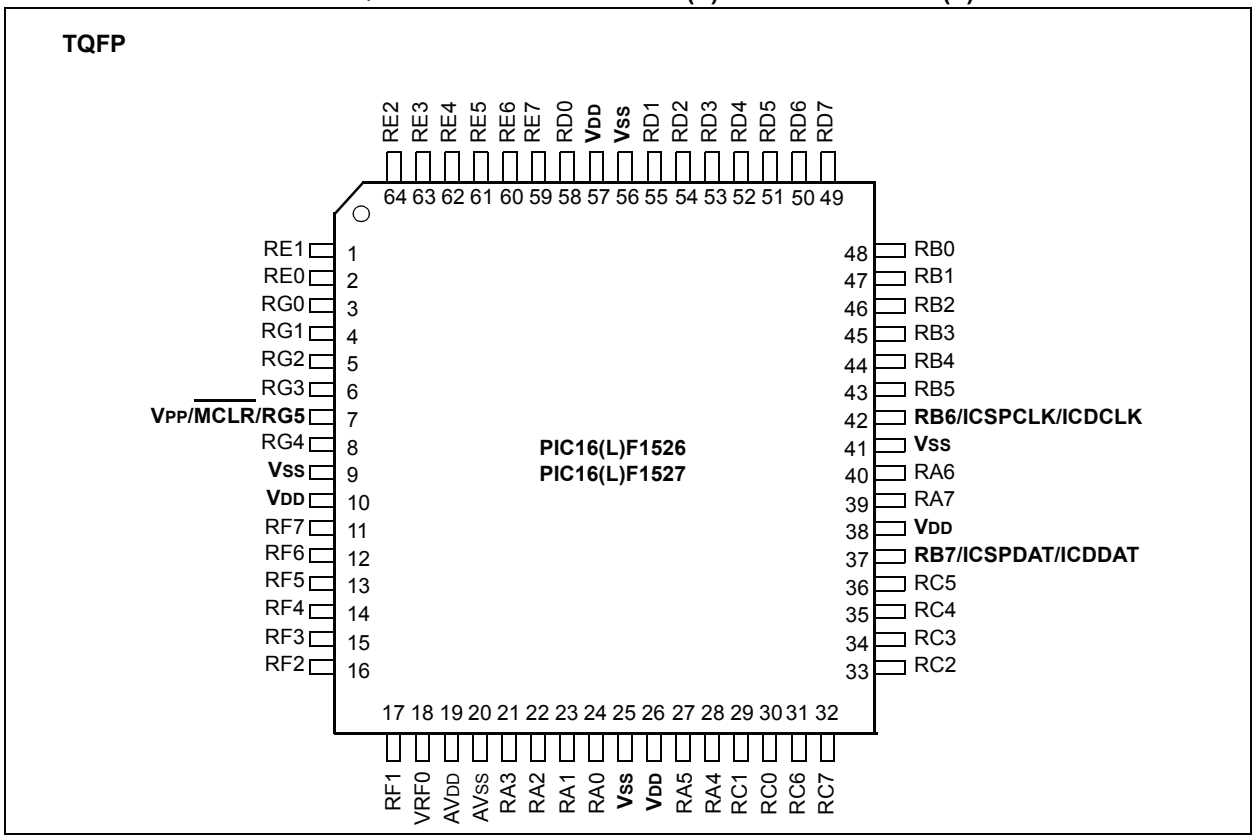
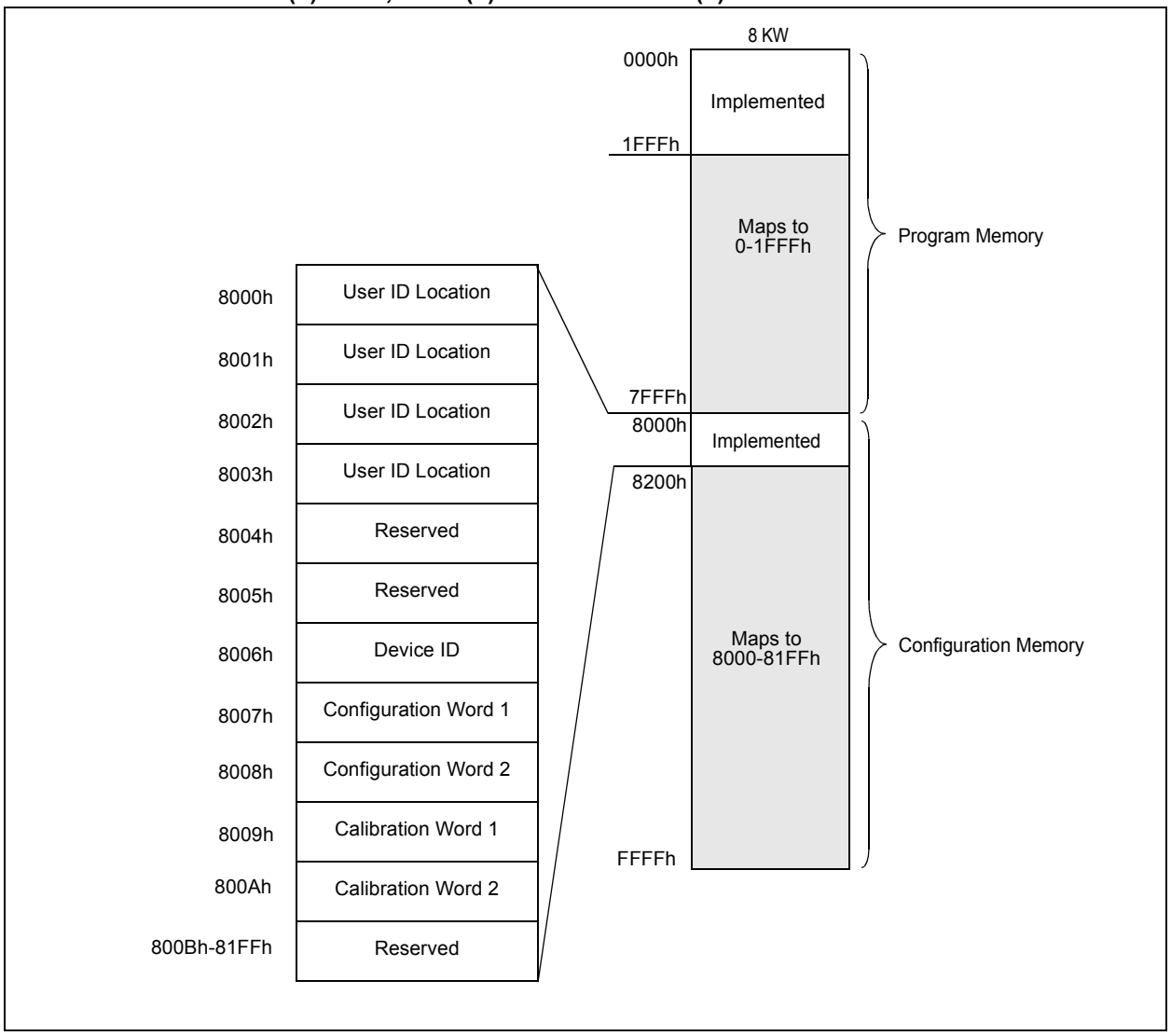


FIGURE 3-3: PIC16(L)F1526, PIC16(L)F1516 AND PIC16(L)F1517 PROGRAM MEMORY MAPPING



3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

Note:	MPLAB® IDE only displays the 7 Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the 7 LSbs be used if MPLAB IDE is the primary tool used to read these addresses.

3.2 Device ID

The device ID word is located at 8006h. This location is read-only and cannot be erased or modified.

REGISTER 3-1: DEVICE ID: DEVICE ID REGISTER(1)

R	R	R	R	R	R
DEV<8:3>					
bit 13					bit 8

R	R	R	R	R	R	R	R
DEV<2:0>			REV<4:0>				
bit 7							bit 0

Legend:	P = Programmable bit	U = Unimplemented bit, read as ‘0’
R = Readable bit	W = Writable bit	‘0’ = Bit is cleared
-n = Value at POR	‘1’ = Bit is set	x = Bit is unknown

bit 13-5 **DEV<8:0>:** Device ID bits
These bits are used to identify the part number.

bit 4-0 **REV<4:0>:** Revision ID bits
These bits are used to identify the revision.

Note 1: This location cannot be written.

REGISTER 3-3: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
LVP	$\overline{\text{DEBUG}}$	$\overline{\text{LPBOR}}$	BORV	STVREN	—
bit 13					bit 8

U-1	U-1	U-1	R/P-1	U-1	U-1	R/P-1	R/P-1
—	—	—	$\overline{\text{VCAPEN}}$(2)	—	—	WRT<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **LVP:** Low-Voltage Programming Enable bit(1)
1 = Low-voltage programming enabled
0 = HV on $\overline{\text{MCLR}}$/VPP must be used for programming

bit 12 **$\overline{\text{DEBUG}}$:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
0 = In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger

bit 11 **$\overline{\text{LPBOR}}$:** Low-Power BOR
1 = Low-Power BOR is disabled
0 = Low-Power BOR is enabled

bit 10 **BORV:** Brown-out Reset Voltage Selection bit
1 = Brown-out Reset voltage (VBOR), low trip point selected
0 = Brown-out Reset voltage (VBOR), high trip point selected

bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
1 = Stack Overflow or Underflow will cause a Reset
0 = Stack Overflow or Underflow will not cause a Reset

bit 8-5 **Unimplemented:** Read as '1'

bit 4 **$\overline{\text{VCAPEN}}$:** Voltage Regulator Capacitor Enable bits(1)
0 = VCAP functionality is enabled on VCAP pin
1 = All VCAP pin functions are disabled

bit 3-2 **Unimplemented:** Read as '1'

bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits
2 kW Flash memory (PIC16(L)F1512):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
01 = 000h to FFFh write-protected, 400h to 7FFh may be modified by PMCON control
00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control
4 kW Flash memory (PIC16(L)F1513):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control
01 = 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control
00 = 000h to FFFh write-protected, no addresses may be modified by PMCON control
8 kW Flash memory (PIC16F/LF1516/1517/1526):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 1FFFh may be modified by PMCON control
01 = 000h to FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control
00 = 000h to 1FFFh write-protected, no addresses may be modified by PMCON control
16 kW Flash memory (PIC16F/LF1518/1519/1527):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 3FFFh may be modified by PMCON control
01 = 000h to 1FFFh write-protected, 2000h to 3FFFh may be modified by PMCON control
00 = 000h to 3FFFh write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.
2: Applies to PIC16F151X/152X devices only. On PIC16LF151X/152X, the $\overline{\text{VCAPEN}}$ bit is unimplemented.

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to VIHH.
3. Raise the voltage on VDD FROM 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when Configuration Word 1 has $\overline{\text{MCLR}}$ disabled (MCLRE = 0), the power-up time is disabled ($\overline{\text{PWRTE}}$ = 0), the internal oscillator is selected (FOSC = 100), and ICSPCLK and ICSPDAT pins are driven by the user application, the device will execute code. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in Figure 8-2.

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from VDD or below to VIHH.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-1.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower (VIL). See Figures 8-3 and 8-4.

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the PIC16(L)F151X/152X devices to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 8-8 and Figure 8-9.

Exiting Program/Verify mode is done by no longer driving $\overline{\text{MCLR}}$ to VIL. See Figure 8-8 and Figure 8-9.

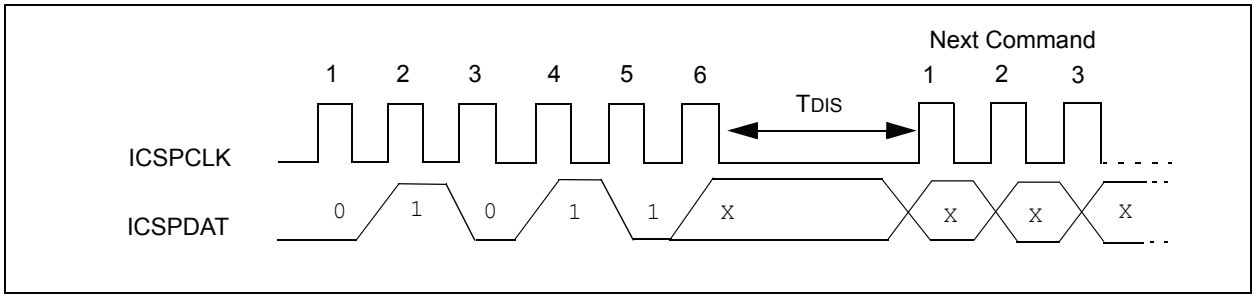
Note:	To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

4.3.8 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPEXT after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 4-8).

FIGURE 4-8: END EXTERNALLY TIMED PROGRAMMING



4.3.9 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-7FFFh:

- Program Memory is erased
- Configuration Words are erased

Address 8000h-8008h:

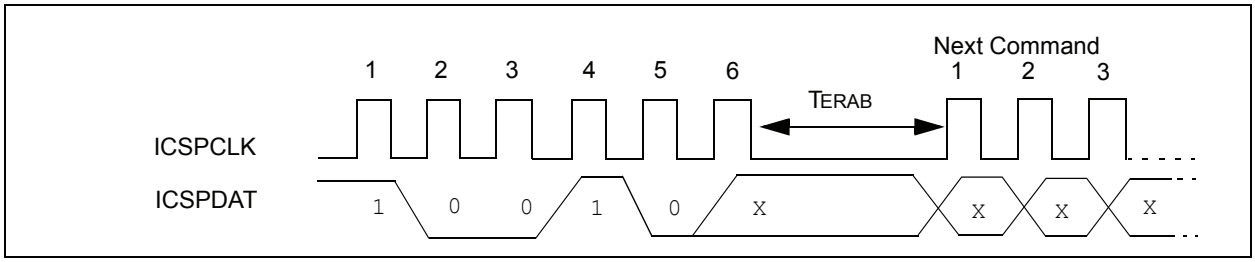
- Program Memory is erased
- Configuration Words are erased
- User ID Locations are erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

After receiving the Bulk Erase Program Memory command the erase will not complete until the time interval, TERAB, has expired.

Note:	The code protection Configuration bit ($\overline{CP}$) has no effect on the Bulk Erase Program Memory command.

FIGURE 4-9: BULK ERASE PROGRAM MEMORY



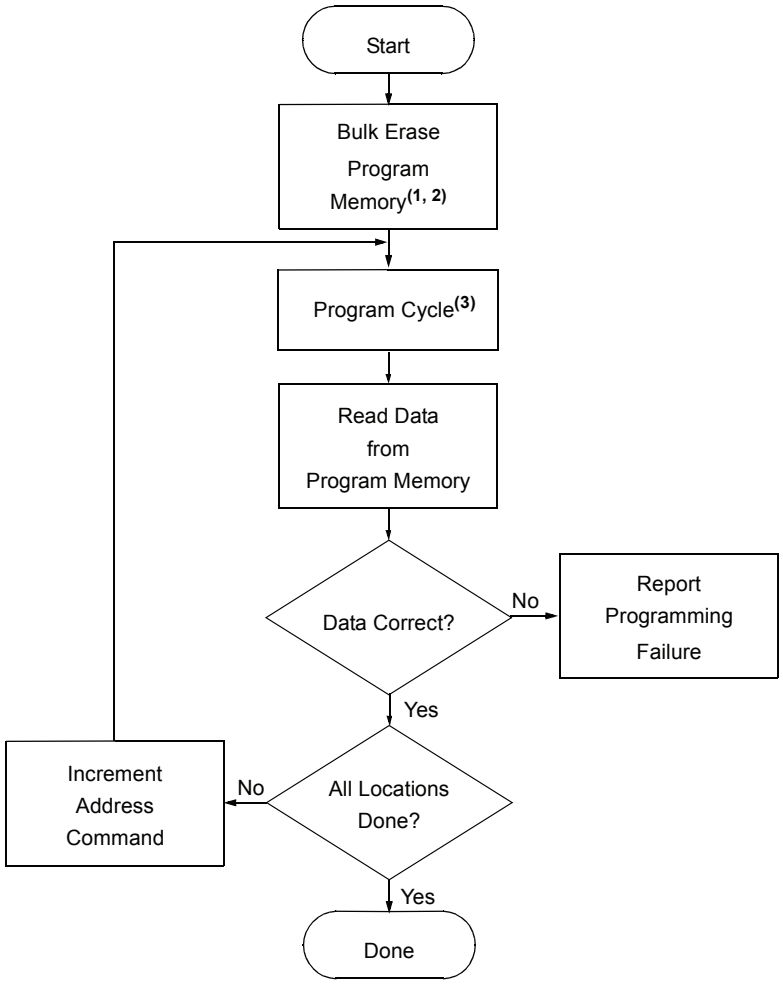
5.0 PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to Table 4-2 for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC's address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes cannot cross the physical boundary. For example, with the PIC16F1527, attempting to write from address 0002h-0009h will result in data being written to 0008h-000Fh.

If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

FIGURE 5-2: PROGRAM MEMORY FLOWCHART



Note 1: This step is optional if device has already been erased or has not been previously programmed.

2: If the device is code-protected or must be completely erased, then Bulk Erase device per Figure 5-6.

3: See Figure 5-3 or Figure 5-4.

FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

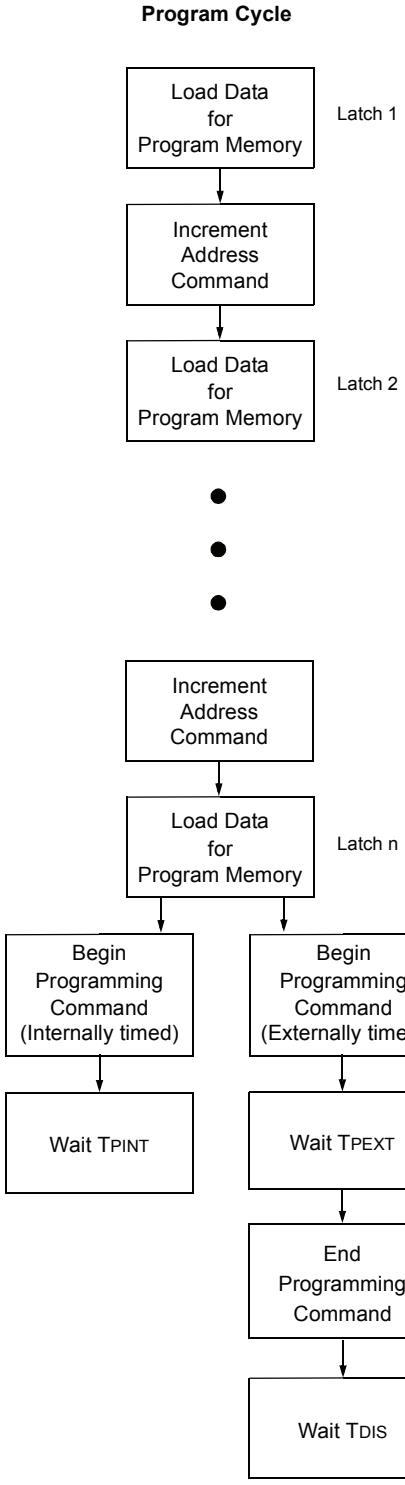
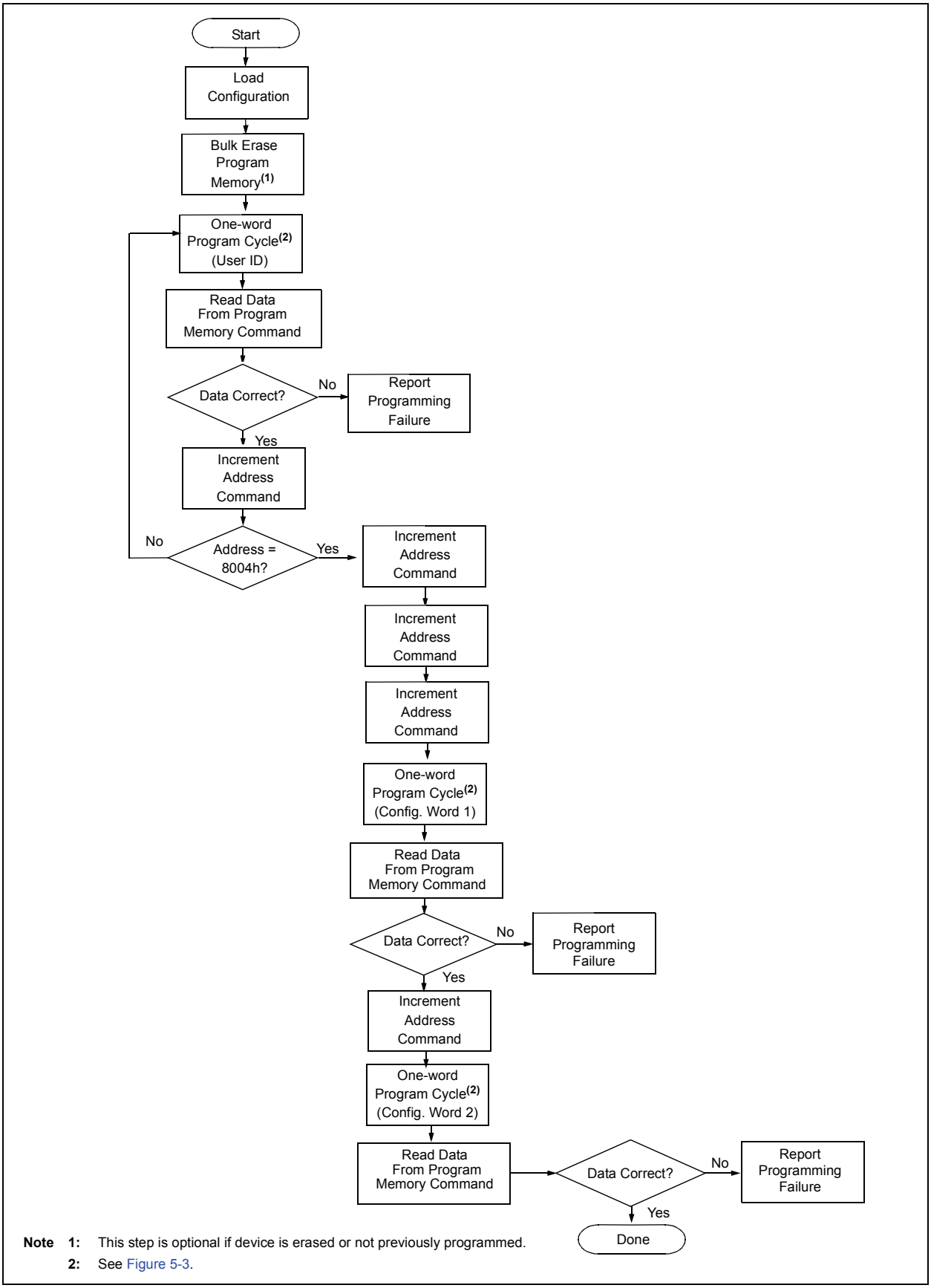


FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART



Note 1: This step is optional if device is erased or not previously programmed.

2: See Figure 5-3.

6.0 CODE PROTECTION

Code protection is controlled using the $\overline{CP}$ bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFFh) read as all '0'. Further programming is disabled for the program memory (0000h-7FFFh).

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Program Memory

Code protection is enabled by programming the $\overline{CP}$ bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: Configuration Word 1 is stored at 8007h on the PIC16(L)F151X/152X. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID and Revision

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID (excluding the revision) against the value read from the part. On a mismatch condition the programmer should generate a warning message.

EXAMPLE 7-4: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC16LF1527, 00AAh AT FIRST AND LAST ADDRESS

PIC16LF1527	Configuration Word 1(2)	3F7Fh
	Configuration Word 1 mask(3)	3EFFh
	Configuration Word 2(2)	3FFFh
	Configuration Word 2 mask(3), (5)	3E03h
	User ID (8000h)(1)	000Eh
	User ID (8001h)(1)	0008h
	User ID (8002h)(1)	0005h
	User ID (8003h)(1)	0008h
	Sum of User IDs(4)	= (000Eh and 000Fh) << 12 + (0008h and 000Fh) << 8 + (0005h and 000Fh) << 4 + (0008h and 000Fh) = E000h + 0800h + 0050h + 0008h = E858h
	Checksum	= (3F7Fh and 3EFFh) + (3FFFh and 3E03h) + Sum of User IDs = 3E7Fh +3E03h + E858h = 64DAh

Note 1: User ID values in this example are random values.

2: Configuration Word 1 and 2 = all bits are '1' except the code-protect enable bit.

3: Configuration Word 1 and 2 Mask = all Configuration Word bits are set to '1', except for unimplemented bits which read '0'.

4: << = shift left, thus the LSb of the first user ID value is the MSb of the sum of user IDs and so on, until the LSb of the last user ID value becomes the LSb of the sum of user IDs.

5: On the PIC16LF1527 device, the $\overline{\text{VCAPEN}}$ bit is not implemented in Configuration Word 2; thus, all unimplemented bits are '0'.

8.0 ELECTRICAL SPECIFICATIONS

Refer to device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS			Standard Operating Conditions Production tested at 25°C				
Sym.	**Characteristics**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
Supply Voltages and Currents							
V_{DD}	Supply Voltage (V_{DDMIN}, V_{DDMAX})	PIC16F151X PIC16F152X	2.3	—	5.5	V	
		PIC16LF151X PIC16LF152X	1.8	—	3.6	V	
V_{PEW}	Read/Write and Row Erase operations		V_{DDMIN}	—	V_{DDMAX}	V	
V_{PBE}	Bulk Erase operations		2.7	—	V_{DDMAX}	V	
I_{DDI}	Current on V_{DD}, Idle		—	—	1.0	mA	
I_{DDP}	Current on V_{DD}, Programming		—	—	3.0	mA	
	V_{PP}						
I_{PP}	Current on $\overline{MCLR}/V_{PP}$		—	—	600	μA	
V_{IHH}	High voltage on $\overline{MCLR}/V_{PP}$ for Program/Verify mode entry		8.0	—	9.0	V	
T_{VHHR}	$\overline{MCLR}$ rise time (V_{IL} to V_{IHH}) for Program/Verify mode entry		—	—	1.0	μs	
	I/O pins						
V_{IH}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) input high level		0.8 V_{DD}	—	—	V	
V_{IL}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) input low level		—	—	0.2 V_{DD}	V	
V_{OH}	ICSPDAT output high level		V_{DD}-0.7 V_{DD}-0.7 V_{DD}-0.7	—	—	V	I_{OH} = 3.5 mA, V_{DD} = 5V I_{OH} = 3 mA, V_{DD} = 3.3V I_{OH} = 2 mA, V_{DD} = 1.8V
V_{OL}	ICSPDAT output low level		—	—	V_{SS}+0.6 V_{SS}+0.6 V_{SS}+0.6	V	I_{OH} = 8 mA, V_{DD} = 5V I_{OH} = 6 mA, V_{DD} = 3.3V I_{OH} = 3 mA, V_{DD} = 1.8V
Programming Mode Entry and Exit							
T_{ENTS}	Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before V_{DD} or $\overline{MCLR}$↑		100	—	—	ns	
T_{ENTH}	Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after V_{DD} or $\overline{MCLR}$↑		250	—	—	μs	
Serial Program/Verify							
T_{CKL}	Clock Low Pulse Width		100	—	—	ns	
T_{CKH}	Clock High Pulse Width		100	—	—	ns	
T_{DS}	Data in setup time before clock↓		100	—	—	ns	
T_{DH}	Data in hold time after clock↓		100	—	—	ns	
T_{CO}	Clock↑ to data out valid (during a Read Data command)		0	—	80	ns	
T_{LZD}	Clock↓ to data low-impedance (during a Read Data command)		0	—	80	ns	
T_{HZD}	Clock↓ to data high-impedance (during a Read Data command)		0	—	80	ns	
T_{DLY}	Data input not driven to next clock input (delay required between command/data or command/command)		1.0	—	—	μs	
T_{ERAB}	Bulk Erase cycle time		—	—	5	ms	
T_{ERAR}	Row Erase cycle time		—	—	2.5	ms	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
TPINT	Internally timed programming operation time	— —	— —	2.5 5	ms ms	Program memory Configuration Words
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms	**Note 1**
TDIS	Time delay from program to compare (HV discharge time)	300	—	—	μs	
TEXIT	Time delay when exiting Program/Verify mode	1	—	—	μs	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – VDD FIRST

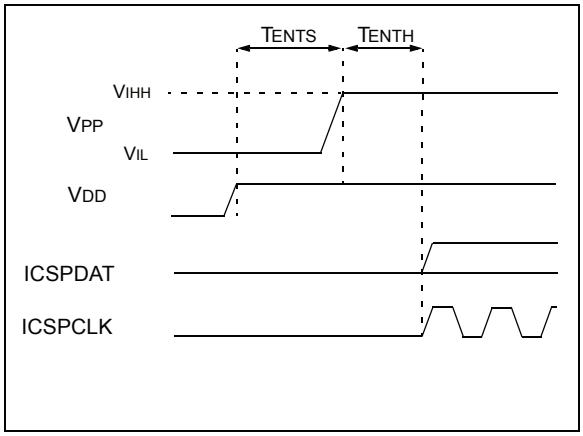


FIGURE 8-2: PROGRAMMING MODE ENTRY – VPP FIRST

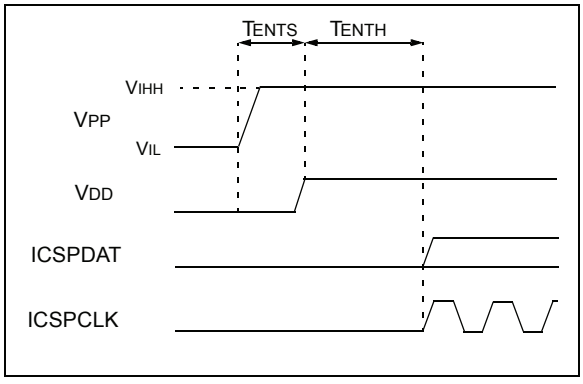


FIGURE 8-3: PROGRAMMING MODE EXIT – VPP LAST

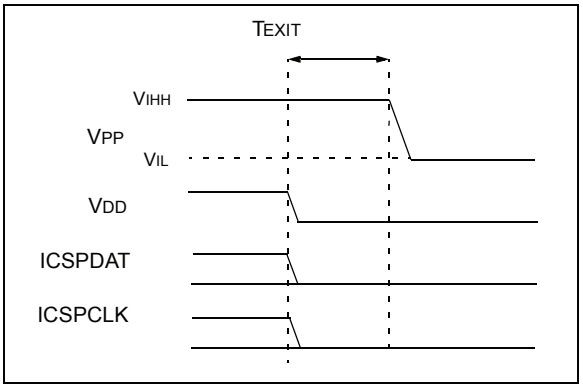


FIGURE 8-4: PROGRAMMING MODE EXIT – VDD LAST

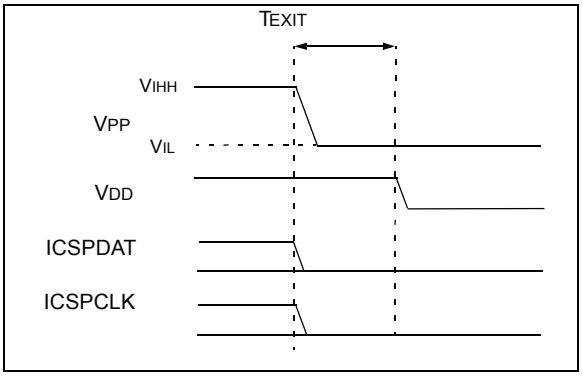


FIGURE 8-5: CLOCK AND DATA TIMING

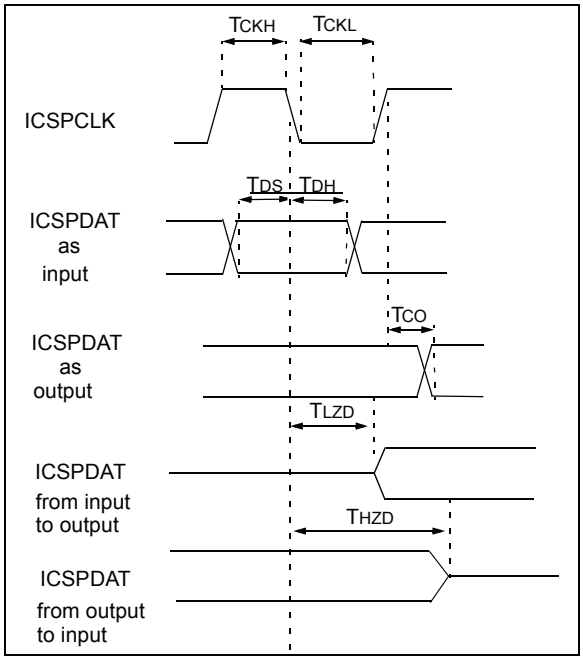


FIGURE 8-6: WRITE COMMAND-PAYLOAD TIMING

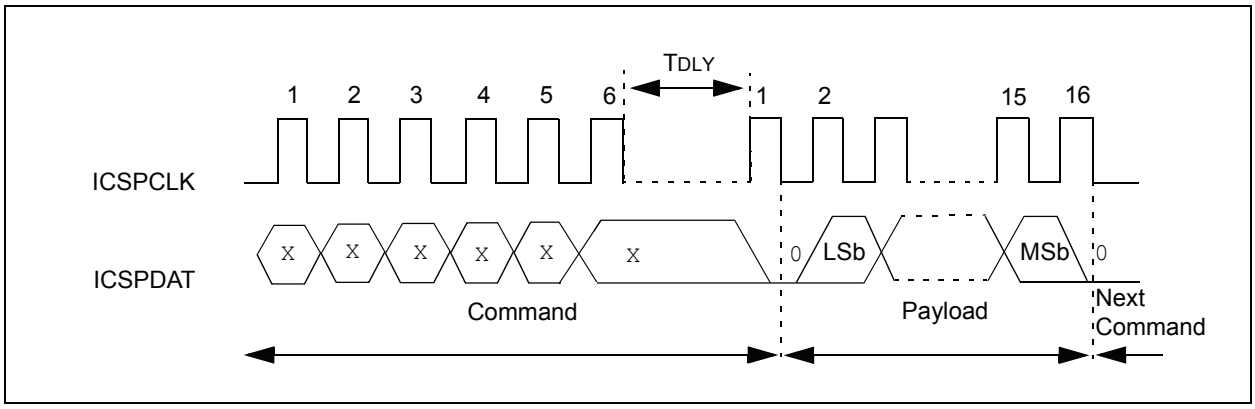


FIGURE 8-7: READ COMMAND-PAYLOAD TIMING

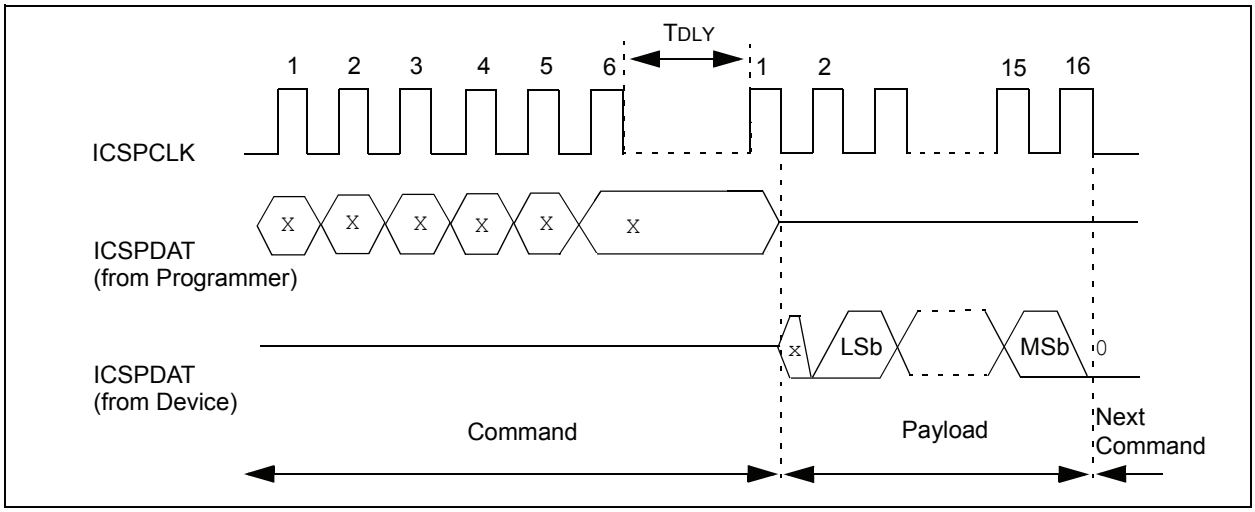


FIGURE 8-8: LVP ENTRY (POWERED)

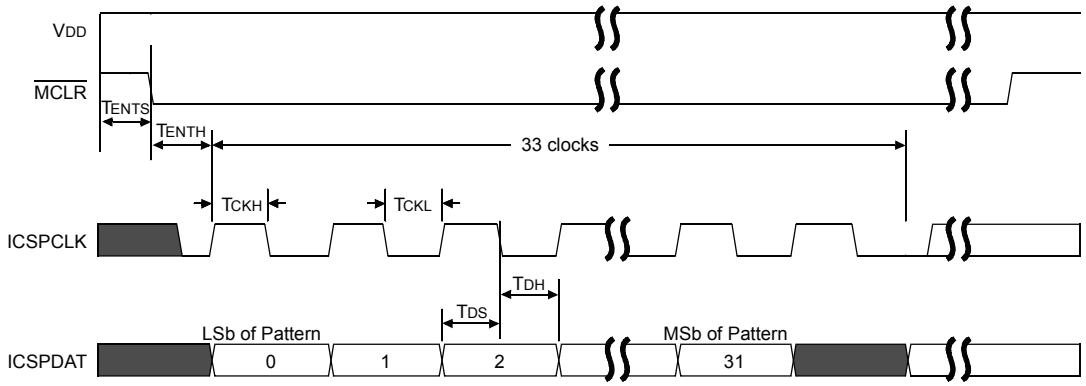
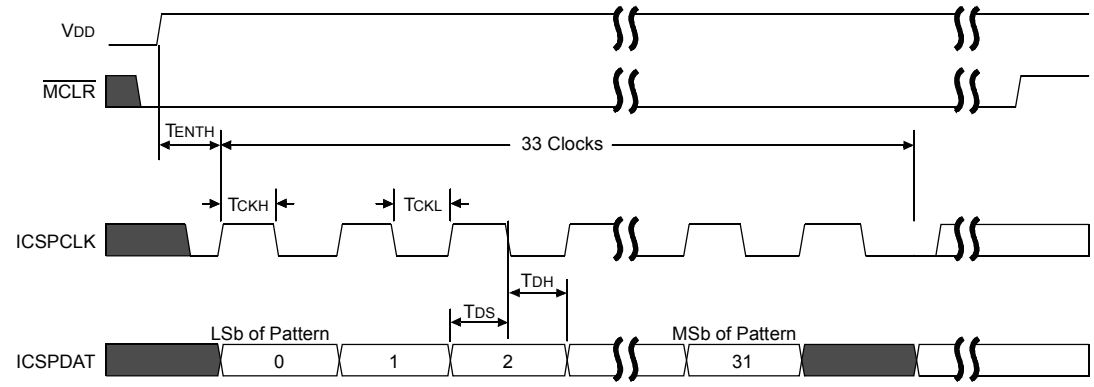


FIGURE 8-9: LVP ENTRY (POWERING UP)



Note 1: Sequence matching can start with no edge on $\overline{MCLR}$ first.

