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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1516-i-mv

PIC16(L)F151X/152X

1.2 Pin Utilization

Five pins are needed for ICSP™ programming. The pins are listed in [Table 1-1](#) and [Table 1-2](#).

TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING – PIC16(L)F1526 AND PIC16(L)F1527

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RG5/ $\overline{\text{MCLR}}$ /VPP	Program/Verify mode	P ⁽¹⁾	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{\text{MCLR}}$ input. Since the $\overline{\text{MCLR}}$ is used for a level source, $\overline{\text{MCLR}}$ does not draw any significant current.

TABLE 1-2: PIN DESCRIPTIONS DURING PROGRAMMING – PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516, PIC16(L)F1517, PIC16(L)F1518 and PIC16(L)F1519

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RE3/ $\overline{\text{MCLR}}$ /VPP	Program/Verify mode	P ⁽¹⁾	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{\text{MCLR}}$ input. Since the $\overline{\text{MCLR}}$ is used for a level source, $\overline{\text{MCLR}}$ does not draw any significant current.

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FIGURE 2-3: 40-PIN PDIP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519

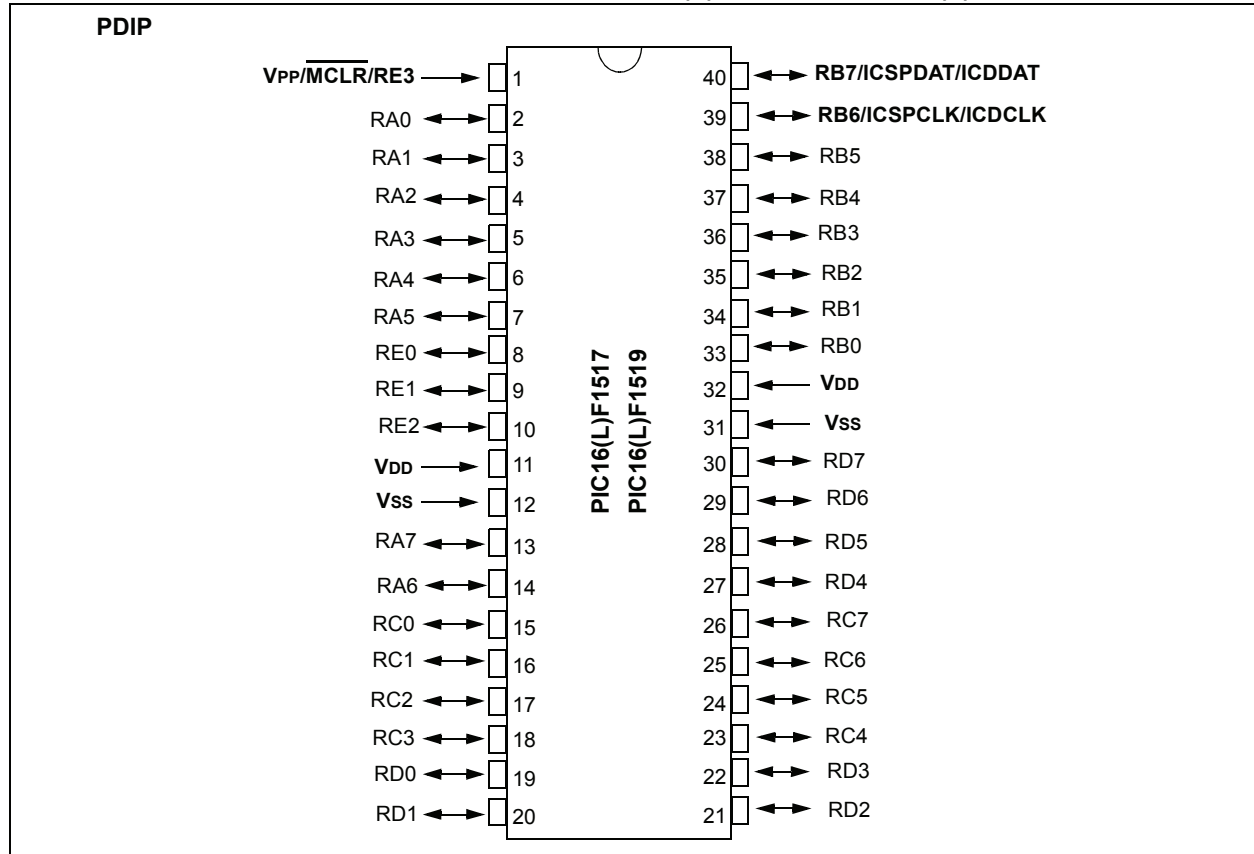
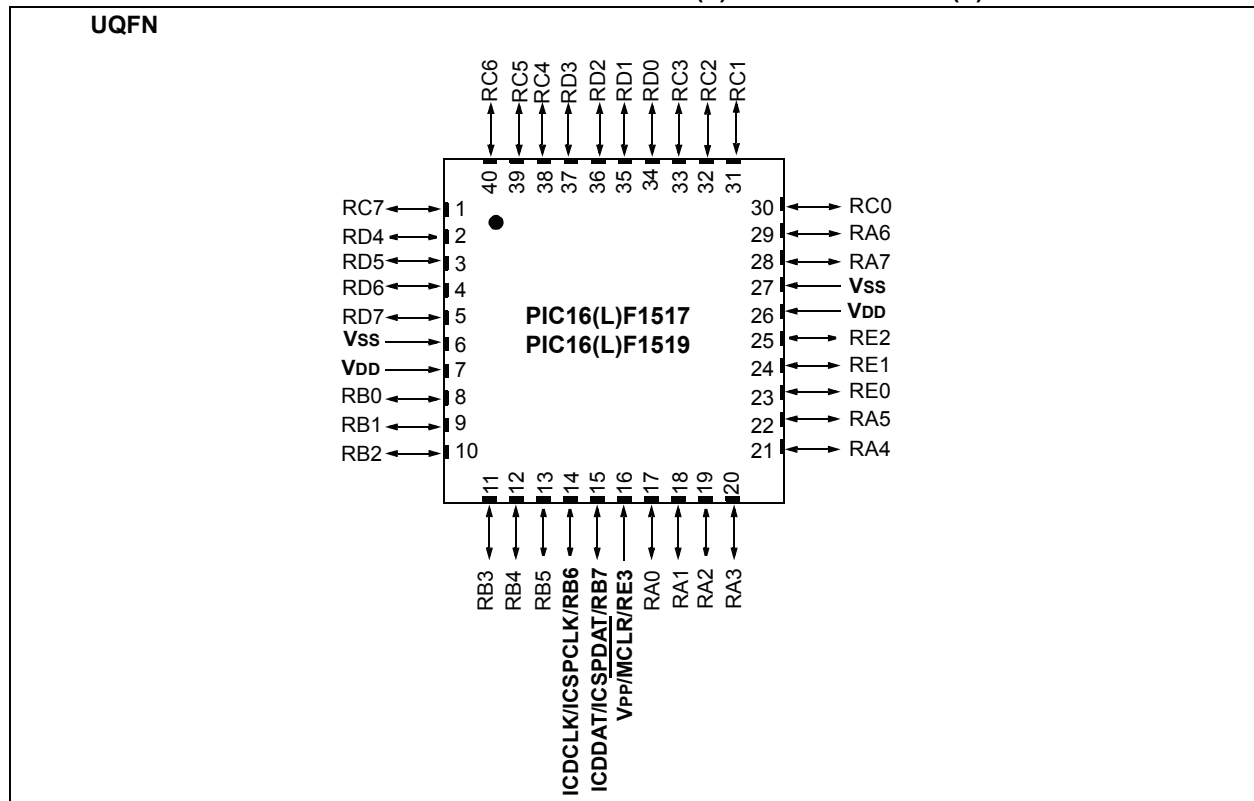


FIGURE 2-4: 40-PIN UQFN DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519



PIC16(L)F151X/152X

FIGURE 2-6: 64-PIN QFN DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527

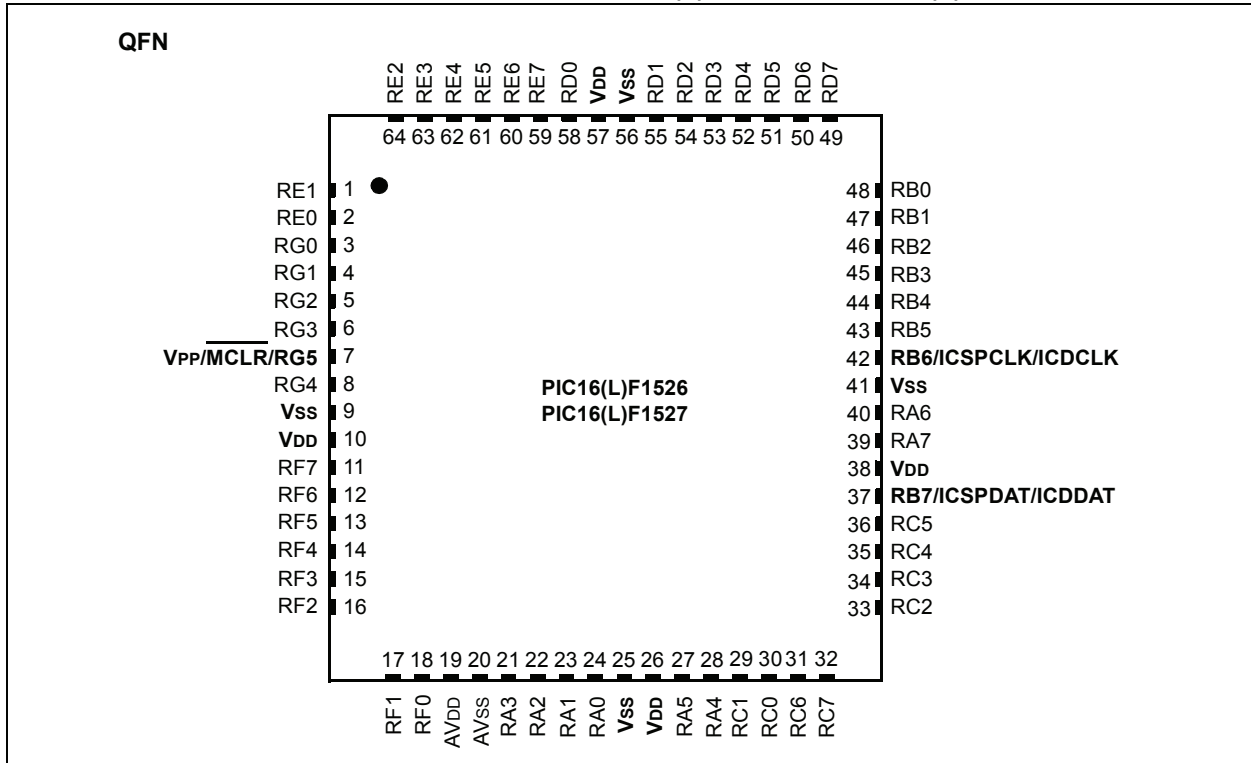


FIGURE 2-7: 64-PIN TQFP DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527

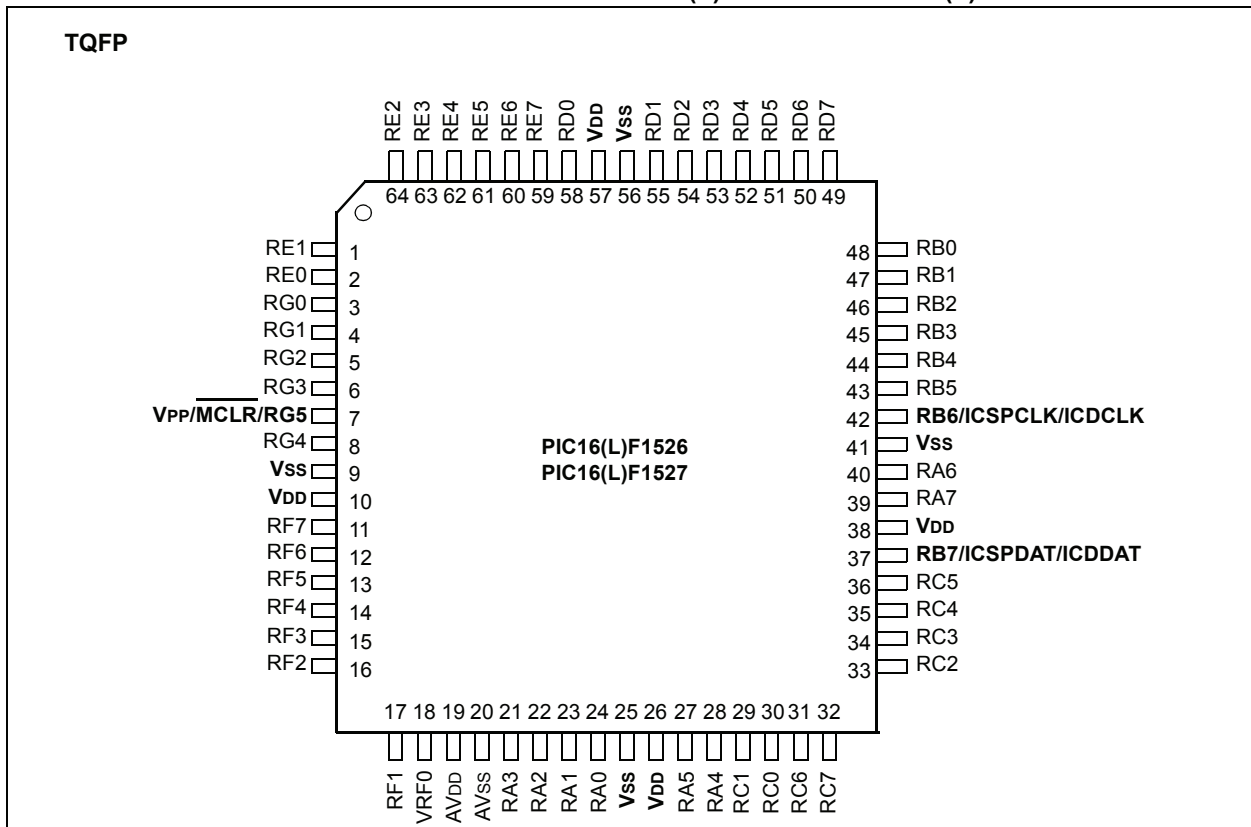
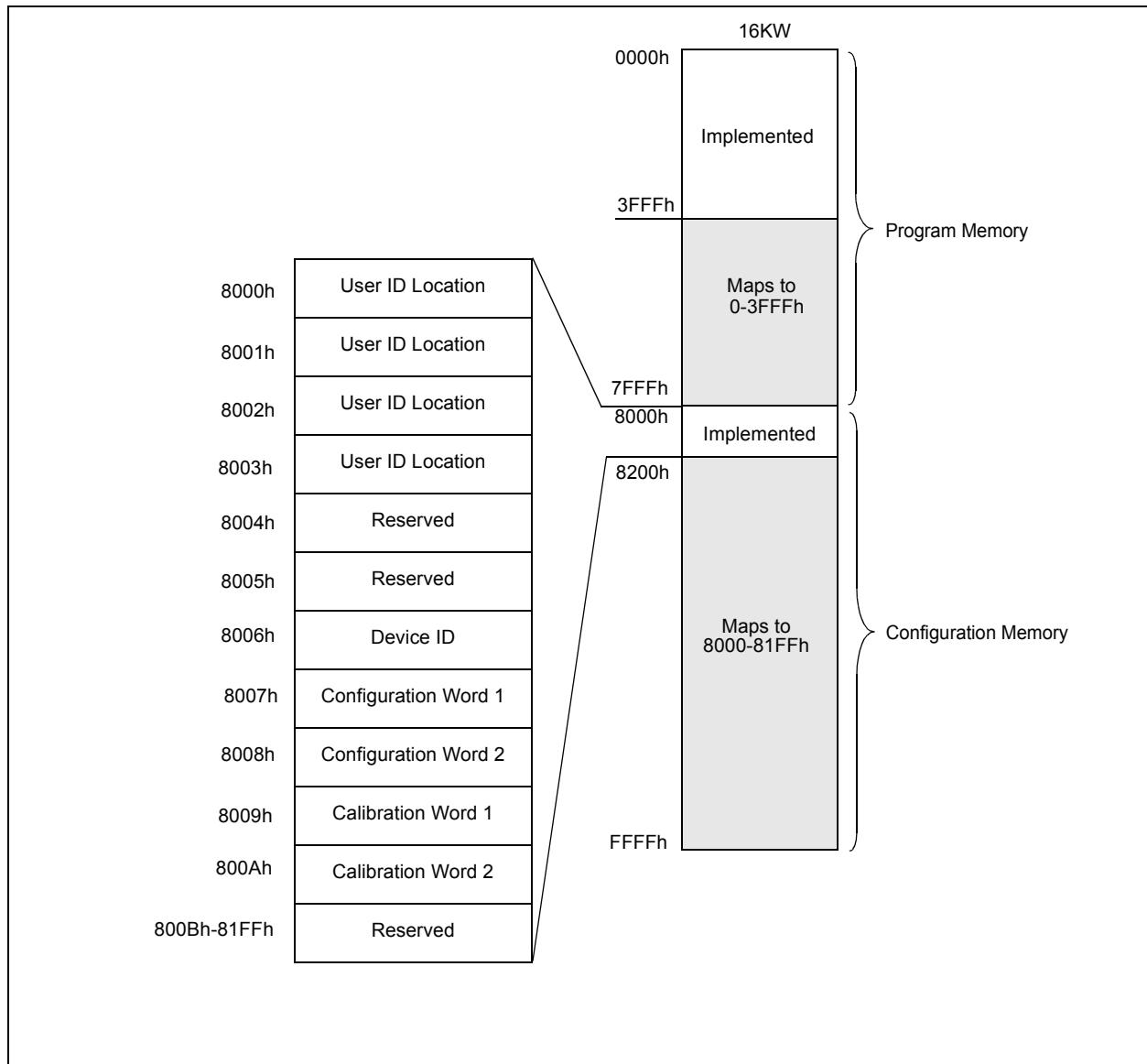


FIGURE 3-4: PIC16(L)F1527, PIC16(L)F1518 AND PIC16(L)F1519 PROGRAM MEMORY MAPPING



PIC16(L)F151X/152X

3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

Note: MPLAB® IDE only displays the 7 Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the 7 LSbs be used if MPLAB IDE is the primary tool used to read these addresses.

3.2 Device ID

The device ID word is located at 8006h. This location is read-only and cannot be erased or modified.

REGISTER 3-1: DEVICE ID: DEVICE ID REGISTER⁽¹⁾

R	R	R	R	R	R
DEV<8:3>					
bit 13			bit 8		

R	R	R	R	R	R	R	R
DEV<2:0>				REV<4:0>			
bit 7				bit 0			

Legend:	P = Programmable bit	U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit	'0' = Bit is cleared
-n = Value at POR	'1' = Bit is set	x = Bit is unknown

bit 13-5 **DEV<8:0>**: Device ID bits
These bits are used to identify the part number.

bit 4-0 **REV<4:0>**: Revision ID bits
These bits are used to identify the revision.

Note 1: This location cannot be written.

TABLE 3-1: DEVICE ID VALUES

DEVICE	DEVICE ID VALUES	
	DEV	REV
PIC16F1527	0001 0101 101	x xxxx
PIC16F1526	0001 0101 100	x xxxx
PIC16LF1527	0001 0101 111	x xxxx
PIC16LF1526	0001 0101 110	x xxxx
PIC16F1519	0001 0110 111	x xxxx
PIC16F1518	0001 0110 110	x xxxx
PIC16F1517	0001 0110 101	x xxxx
PIC16F1516	0001 0110 100	x xxxx
PIC16F1513	0001 0110 010	x xxxx
PIC16F1512	0001 0111 000	x xxxx
PIC16LF1519	0001 0111 111	x xxxx
PIC16LF1518	0001 0111 110	x xxxx
PIC16LF1517	0001 0111 101	x xxxx
PIC16LF1516	0001 0111 100	x xxxx
PIC16LF1513	0001 0111 010	x xxxx
PIC16LF1512	0001 0111 001	x xxxx

3.3 Configuration Words

There are two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

The internal calibration values are factory calibrated and stored in Calibration Words 1 and 2 (8009h, 800Ah).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

PIC16(L)F151X/152X

REGISTER 3-2: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
FCMEN	IESO	CLKOUTEN	BOREN<1:0>	—	
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP	MCLRE	PWRTÉ	WDTE<1:0>	FOSC<2:0>			
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '1'
 '0' = Bit is cleared '1' = Bit is set -n = Value when blank or after Bulk Erase

- bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
 1 = Fail-Safe Clock Monitor is enabled
 0 = Fail-Safe Clock Monitor is disabled
- bit 12 **IESO:** Internal External Switchover bit
 1 = Internal/External Switchover mode is enabled
 0 = Internal/External Switchover mode is disabled
- bit 11 **CLKOUTEN:** Clock Out Enable bit
 1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
 0 = CLKOUT function is enabled on CLKOUT pin
- bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits⁽¹⁾
 11 = BOR enabled
 10 = BOR enabled during operation and disabled in Sleep
 01 = BOR controlled by SBOREN bit of the PCON register
 00 = BOR disabled
- bit 8 **Unimplemented:** Read as '1'
- bit 7 **CP:** Code Protection bit⁽²⁾
 1 = Program memory code protection is disabled
 0 = Program memory code protection is enabled
- bit 6 **MCLRE:** MCLR/VPP Pin Function Select bit
 If LVP bit = 1:
 This bit is ignored.
 If LVP bit = 0:
 1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
 0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUA register.
- bit 5 **PWRTÉ:** Power-up Timer Enable bit⁽¹⁾
 1 = PWRT disabled
 0 = PWRT enabled
- bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
 11 = WDT enabled
 10 = WDT enabled while running and disabled in Sleep
 01 = WDT controlled by the SWDTEN bit in the WDTCON register
 00 = WDT disabled
- bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
 111 = ECH: External Clock, High-Power mode: on CLKIN pin
 110 = ECM: External Clock, Medium-Power mode: on CLKIN pin
 101 = ECL: External Clock, Low-Power mode: on CLKIN pin
 100 = INTOSC oscillator: I/O function on OSC1 pin
 011 = EXTRC oscillator: RC function on OSC1 pin
 010 = HS oscillator: High-speed crystal/resonator on OSC2 pin and OSC1 pin
 001 = XT oscillator: Crystal/resonator on OSC2 pin and OSC1 pin
 000 = LP oscillator: Low-power crystal on OSC2 pin and OSC1 pin

- Note** 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
 2: The entire program memory will be erased when the code protection is turned off.

REGISTER 3-3: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
LVP	DEBUG	LPBOR	BORV	STVREN	—
bit 13					bit 8

U-1	U-1	U-1	R/P-1	U-1	U-1	R/P-1	R/P-1
—	—	—	VCAPEN ⁽²⁾	—	—	WRT<1:0>	
bit 7							bit 0

Legend:

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '1'

'0' = Bit is cleared

'1' = Bit is set

-n = Value when blank or after Bulk Erase

- bit 13 **LVP:** Low-Voltage Programming Enable bit⁽¹⁾
 1 = Low-voltage programming enabled
 0 = HV on MCLR/VPP must be used for programming
- bit 12 **DEBUG:** In-Circuit Debugger Mode bit
 1 = In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
 0 = In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger
- bit 11 **LPBOR:** Low-Power BOR
 1 = Low-Power BOR is disabled
 0 = Low-Power BOR is enabled
- bit 10 **BORV:** Brown-out Reset Voltage Selection bit
 1 = Brown-out Reset voltage (VBOR), low trip point selected
 0 = Brown-out Reset voltage (VBOR), high trip point selected
- bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
 1 = Stack Overflow or Underflow will cause a Reset
 0 = Stack Overflow or Underflow will not cause a Reset
- bit 8-5 **Unimplemented:** Read as '1'
- bit 4 **VCAPEN:** Voltage Regulator Capacitor Enable bits⁽¹⁾
 0 = VCAP functionality is enabled on VCAP pin
 1 = All VCAP pin functions are disabled
- bit 3-2 **Unimplemented:** Read as '1'
- bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits
2 kW Flash memory (PIC16(L)F1512):
 11 = Write protection off
 10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
 01 = 000h to FFFh write-protected, 400h to 7FFh may be modified by PMCON control
 00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control
4 kW Flash memory (PIC16(L)F1513):
 11 = Write protection off
 10 = 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control
 01 = 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control
 00 = 000h to FFFh write-protected, no addresses may be modified by PMCON control
8 kW Flash memory (PIC16F/LF1516/1517/1526):
 11 = Write protection off
 10 = 000h to 1FFh write-protected, 200h to 1FFFh may be modified by PMCON control
 01 = 000h to FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control
 00 = 000h to 1FFFh write-protected, no addresses may be modified by PMCON control
16 kW Flash memory (PIC16F/LF1518/1519/1527):
 11 = Write protection off
 10 = 000h to 1FFh write-protected, 200h to 3FFFh may be modified by PMCON control
 01 = 000h to 1FFFh write-protected, 2000h to 3FFFh may be modified by PMCON control
 00 = 000h to 3FFFh write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.

Note 2: Applies to PIC16F151X/152X devices only. On PIC16LF151X/152X, the VCAPEN bit is unimplemented.

PIC16(L)F151X/152X

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSB first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to V_{IH} .
3. Raise the voltage on VDD FROM 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when Configuration Word 1 has $\overline{\text{MCLR}}$ disabled ($\text{MCLRE} = 0$), the power-up time is disabled ($\text{PWRT} = 0$), the internal oscillator is selected ($\text{FOSC} = 100$), and ICSPCLK and ICSPDAT pins are driven by the user application, the device will execute code. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in [Figure 8-2](#).

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from VDD or below to V_{IH} .

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in [Figure 8-1](#).

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower (V_{IL}). See [Figures 8-3](#) and [8-4](#).

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the PIC16(L)F151X/152X devices to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to V_{IL} .
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at V_{IL} for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see [Figure 8-8](#) and [Figure 8-9](#).

Exiting Program/Verify mode is done by no longer driving $\overline{\text{MCLR}}$ to V_{IL} . See [Figure 8-8](#) and [Figure 8-9](#).

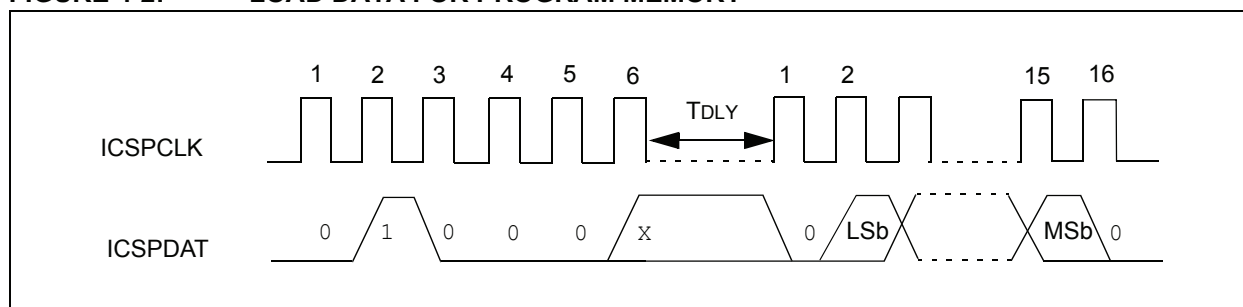
Note: To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

PIC16(L)F151X/152X

4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

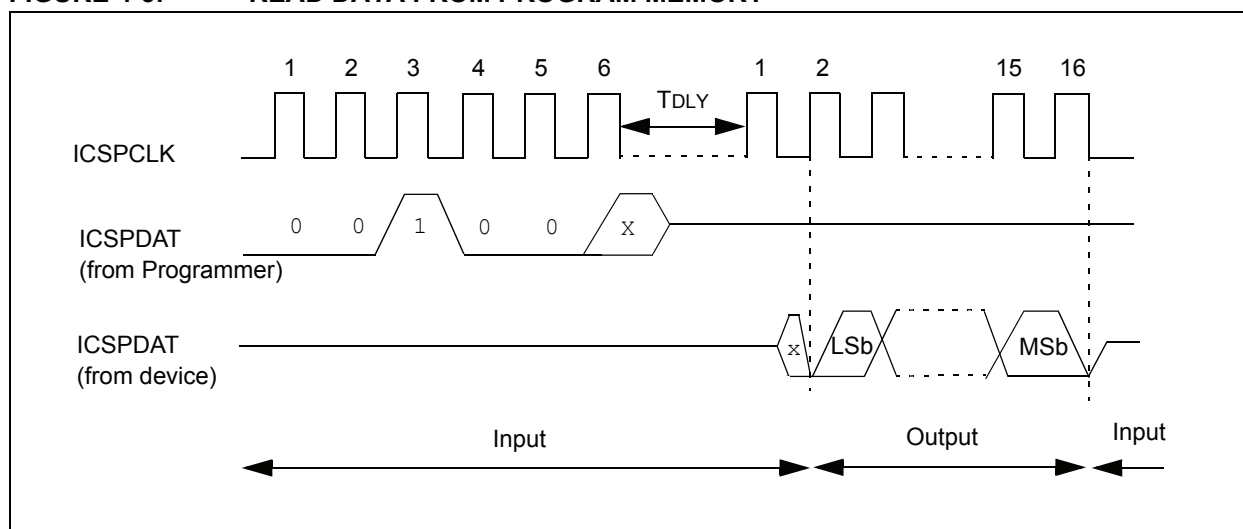
FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY



4.3.3 READ DATA FROM PROGRAM MEMORY

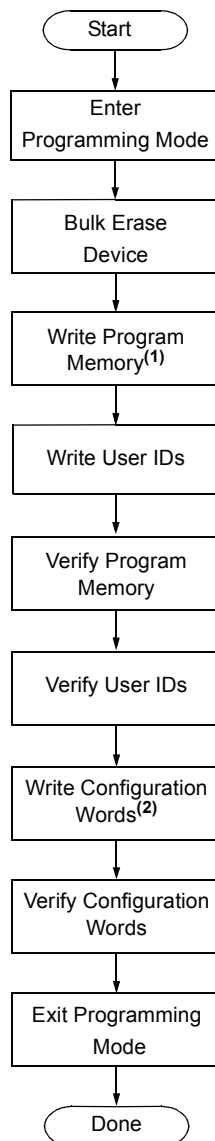
The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected (\overline{CP}), the data will be read as zeros (see Figure 4-3).

FIGURE 4-3: READ DATA FROM PROGRAM MEMORY



PIC16(L)F151X/152X

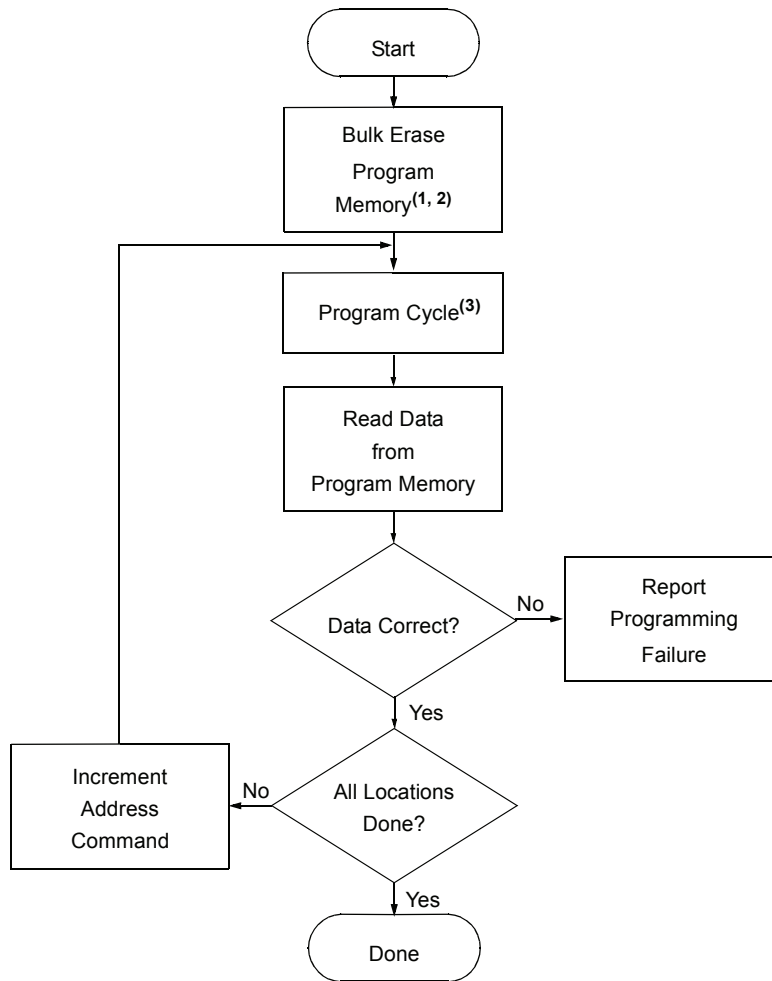
FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART



Note 1: See [Figure 5-2](#).

2: See [Figure 5-5](#).

FIGURE 5-2: PROGRAM MEMORY FLOWCHART



Note 1: This step is optional if device has already been erased or has not been previously programmed.

Note 2: If the device is code-protected or must be completely erased, then Bulk Erase device per [Figure 5-6](#).

Note 3: See [Figure 5-3](#) or [Figure 5-4](#).

PIC16(L)F151X/152X

FIGURE 5-3: ONE-WORD PROGRAM CYCLE

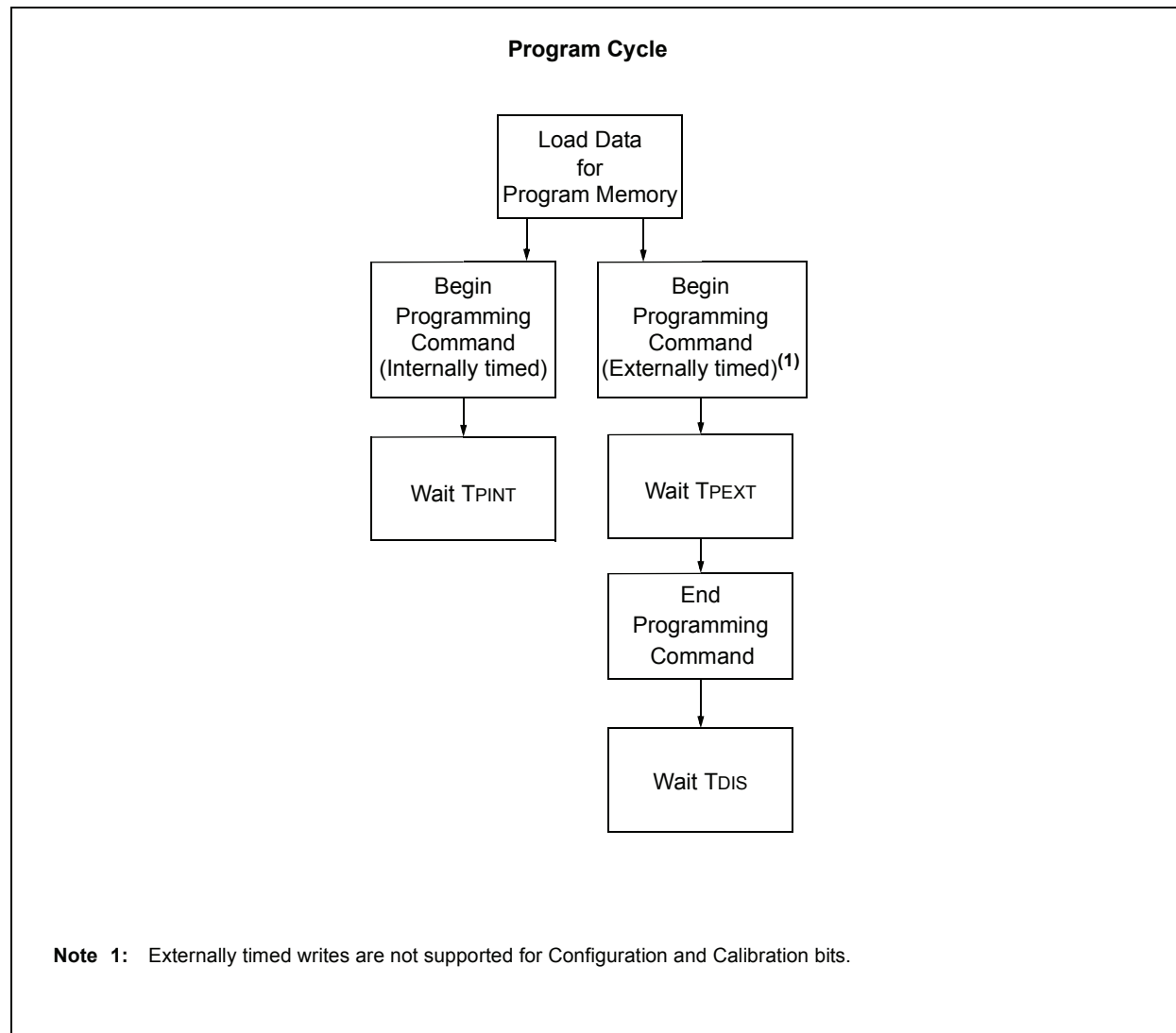
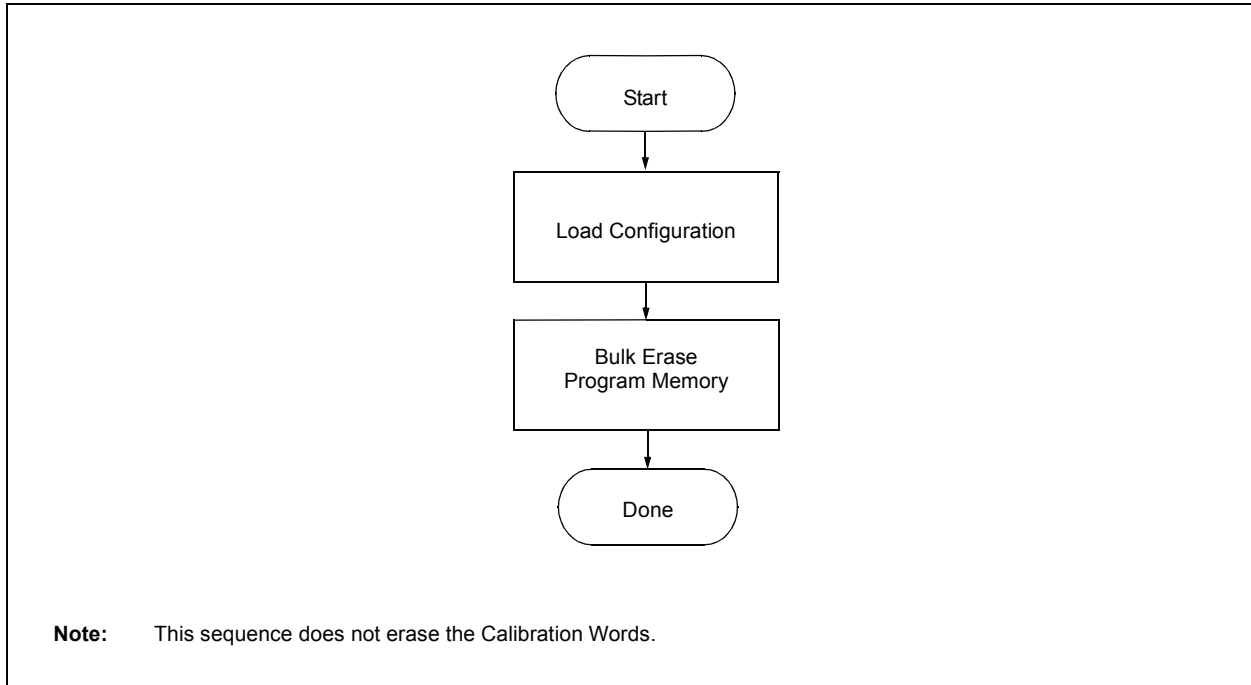


FIGURE 5-6: ERASE FLOWCHART



PIC16(L)F151X/152X

6.0 CODE PROTECTION

Code protection is controlled using the $\overline{\text{CP}}$ bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFFh) read as all '0'. Further programming is disabled for the program memory (0000h-7FFFh).

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Program Memory

Code protection is enabled by programming the $\overline{\text{CP}}$ bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: Configuration Word 1 is stored at 8007h on the PIC16(L)F151X/152X. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID and Revision

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID (excluding the revision) against the value read from the part. On a mismatch condition the programmer should generate a warning message.

PIC16(L)F151X/152X

EXAMPLE 7-4: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC16LF1527, 00AAh AT FIRST AND LAST ADDRESS

PIC16LF1527	Configuration Word 1 ⁽²⁾	3F7Fh
	Configuration Word 1 mask ⁽³⁾	3EFFh
	Configuration Word 2 ⁽²⁾	3FFFh
	Configuration Word 2 mask ^{(3), (5)}	3E03h
	User ID (8000h) ⁽¹⁾	000Eh
	User ID (8001h) ⁽¹⁾	0008h
	User ID (8002h) ⁽¹⁾	0005h
	User ID (8003h) ⁽¹⁾	0008h
	Sum of User IDs ⁽⁴⁾	$= (000Eh \text{ and } 000Fh) \ll 12 + (0008h \text{ and } 000Fh) \ll 8 +$ $(0005h \text{ and } 000Fh) \ll 4 + (0008h \text{ and } 000Fh)$ $= E000h + 0800h + 0050h + 0008h$ $= E858h$
	Checksum	$= (3F7Fh \text{ and } 3EFFh) + (3FFFh \text{ and } 3E03h) + \text{Sum of User IDs}$ $= 3E7Fh + 3E03h + E858h$ $= 64DAh$

- Note 1:** User ID values in this example are random values.
- 2:** Configuration Word 1 and 2 = all bits are '1' except the code-protect enable bit.
- 3:** Configuration Word 1 and 2 Mask = all Configuration Word bits are set to '1', except for unimplemented bits which read '0'.
- 4:** \ll = shift left, thus the LSb of the first user ID value is the MSb of the sum of user IDs and so on, until the LSb of the last user ID value becomes the LSb of the sum of user IDs.
- 5:** On the PIC16LF1527 device, the $\overline{\text{VCAPEN}}$ bit is not implemented in Configuration Word 2; thus, all unimplemented bits are '0'.

PIC16(L)F151X/152X

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
TPINT	Internally timed programming operation time	—	—	2.5	ms	Program memory
		—	—	5	ms	Configuration Words
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms	Note 1
TDIS	Time delay from program to compare (HV discharge time)	300	—	—	μs	
TEXT	Time delay when exiting Program/Verify mode	1	—	—	μs	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – VDD FIRST

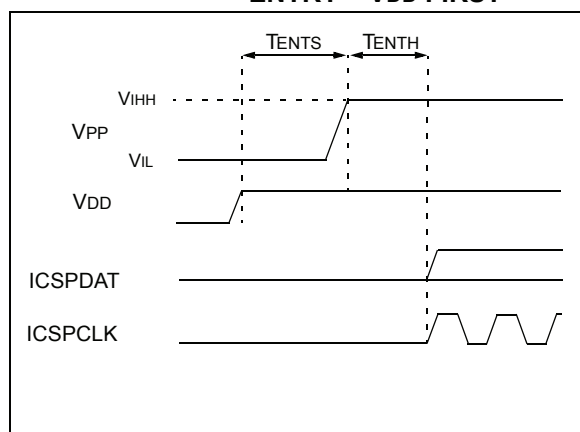


FIGURE 8-2: PROGRAMMING MODE ENTRY – VPP FIRST

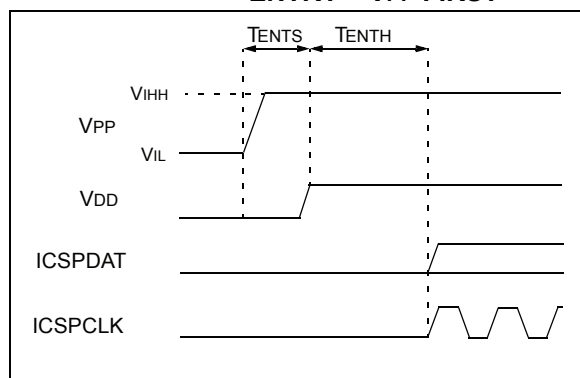


FIGURE 8-3: PROGRAMMING MODE EXIT – VPP LAST

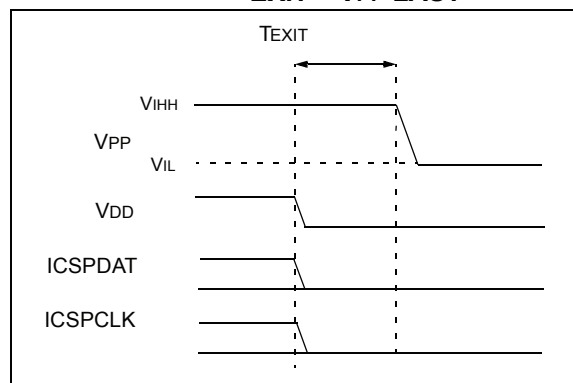
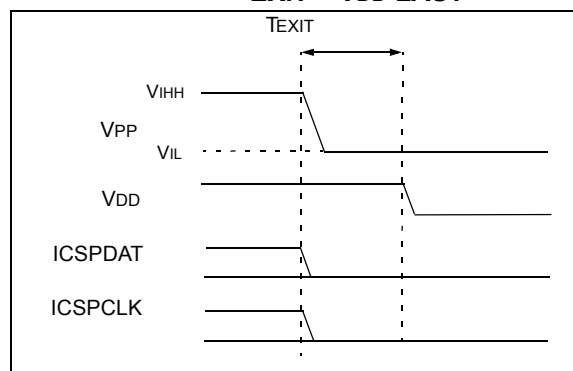


FIGURE 8-4: PROGRAMMING MODE EXIT – VDD LAST



PIC16(L)F151X/152X

FIGURE 8-8: LVP ENTRY (POWERED)

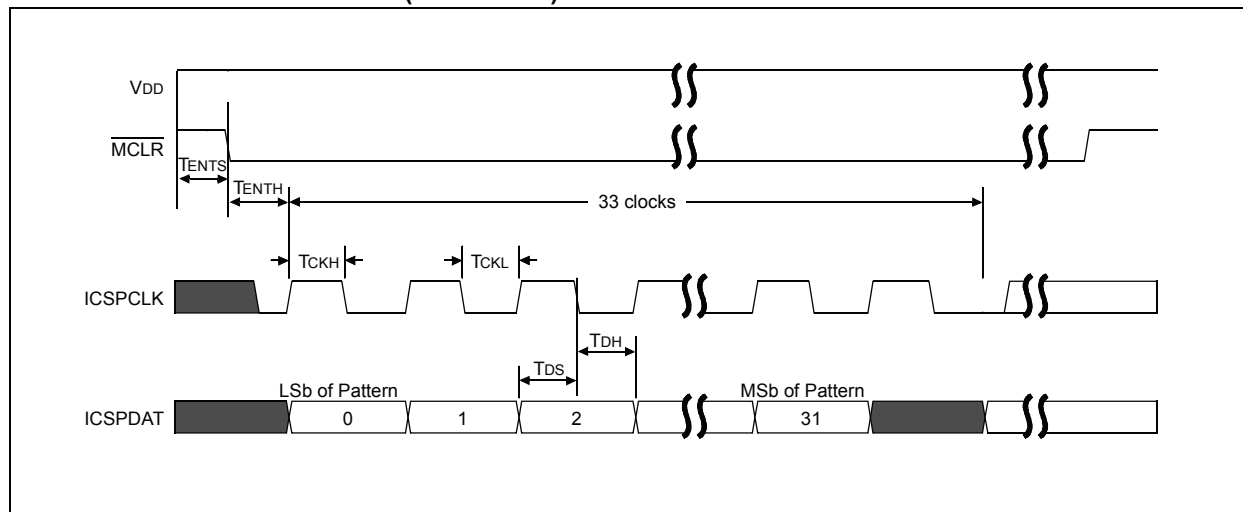
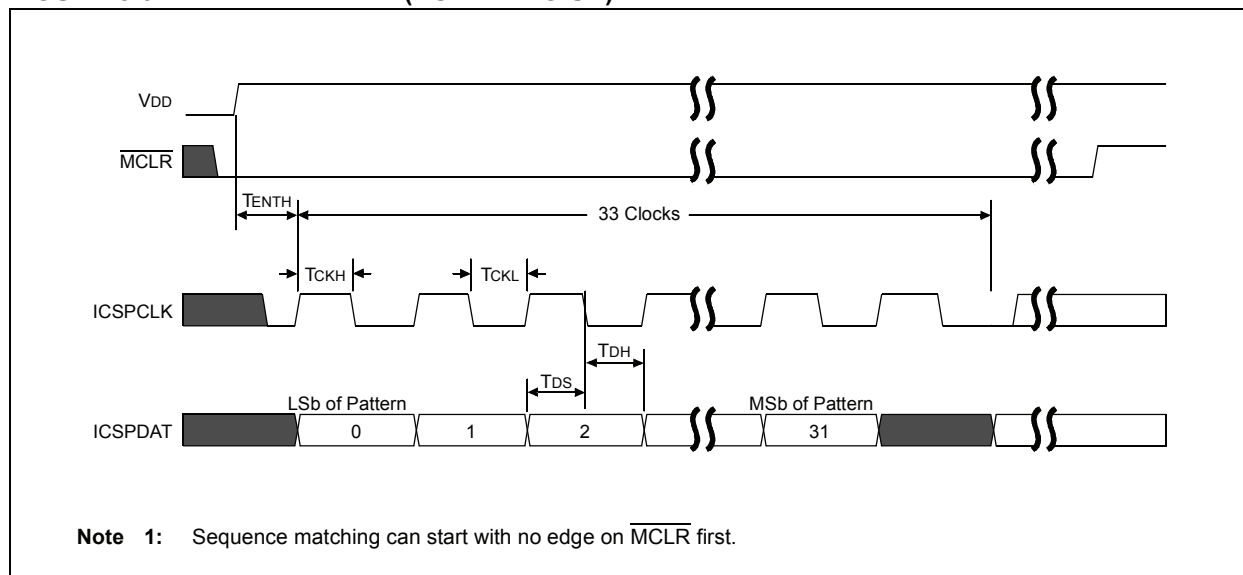


FIGURE 8-9: LVP ENTRY (POWERING UP)



PIC16(L)F151X/152X

NOTES:

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ISBN: 978-1-61341-635-8

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