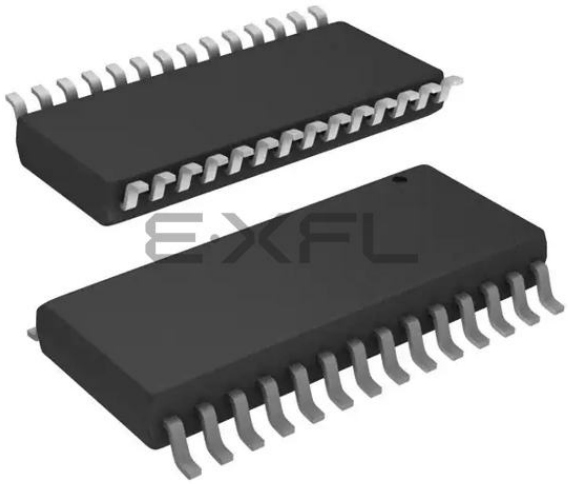

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1516-i-so

FIGURE 2-2: 28-PIN UQFN DIAGRAM FOR PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516 AND PIC16(L)F1518

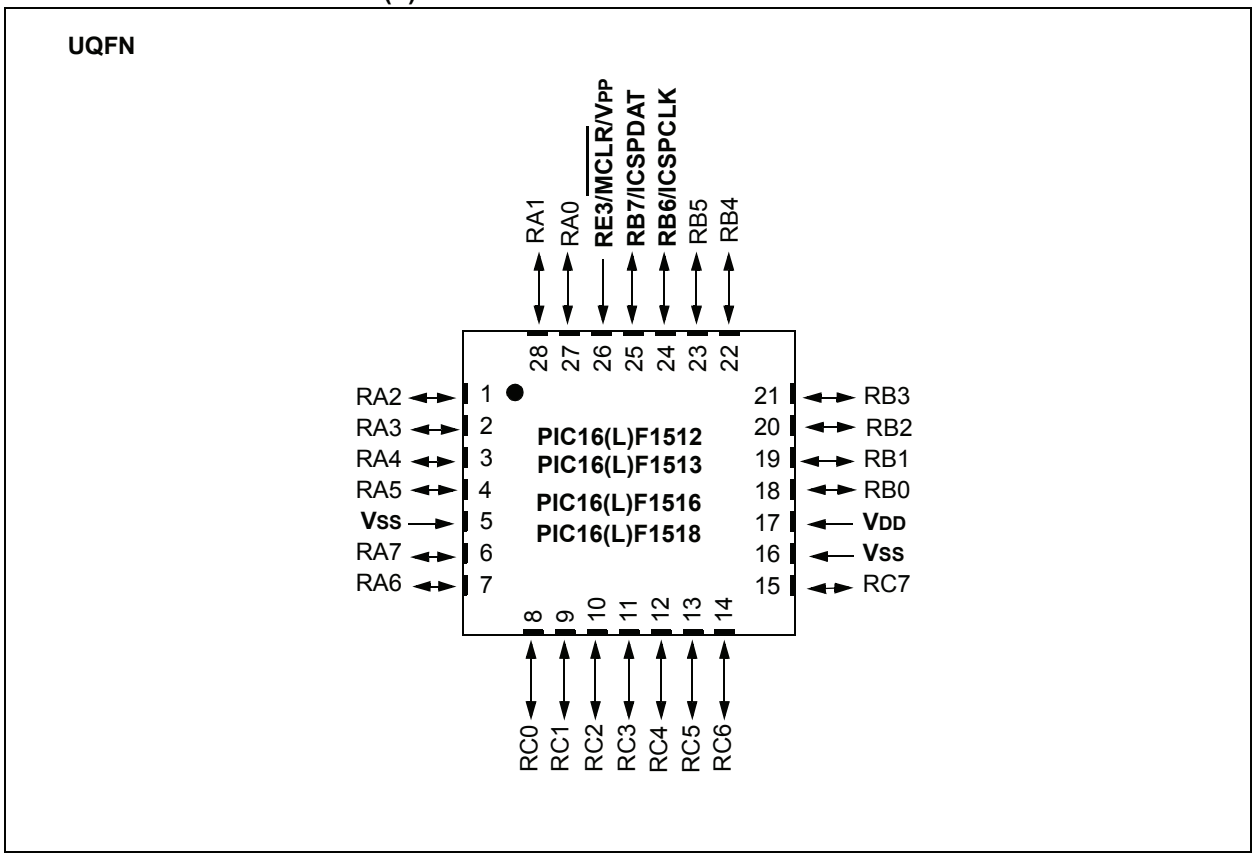


FIGURE 2-3: 40-PIN PDIP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519

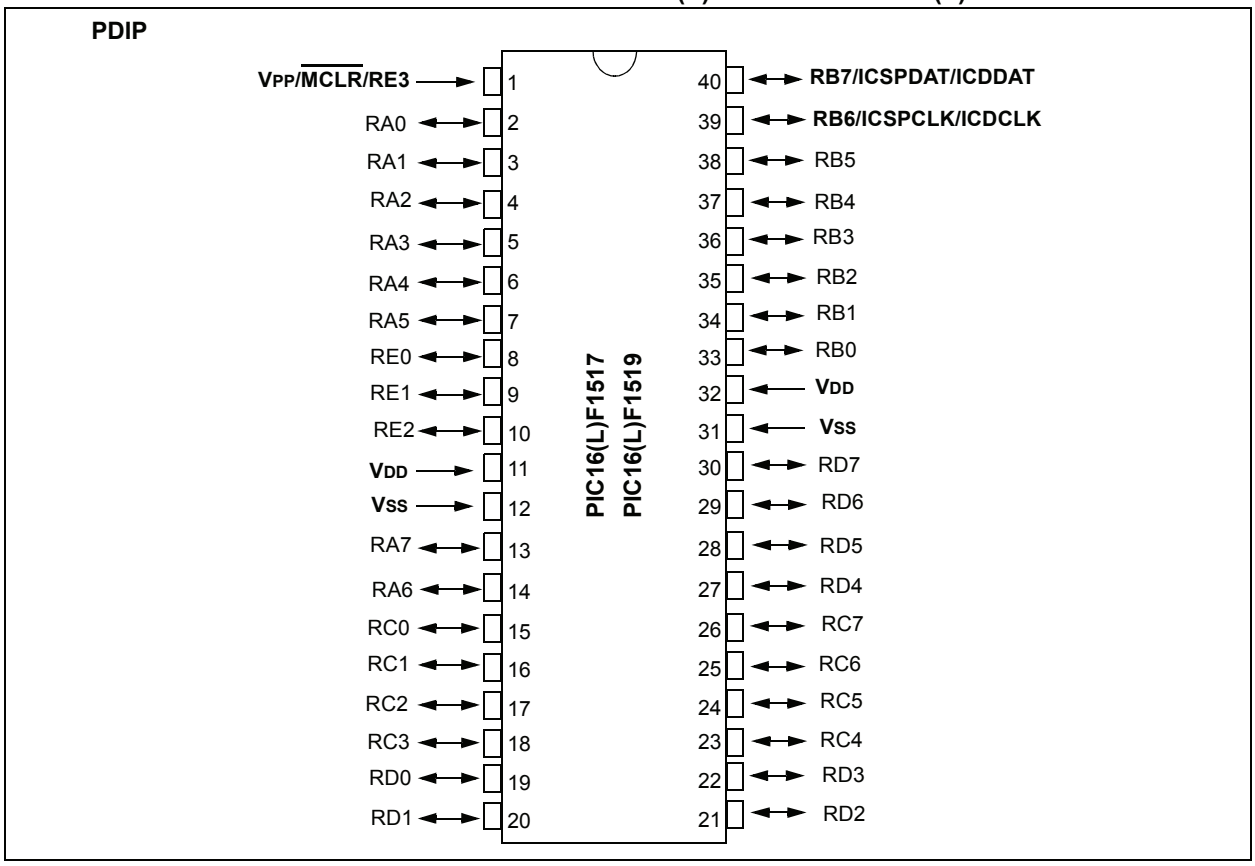
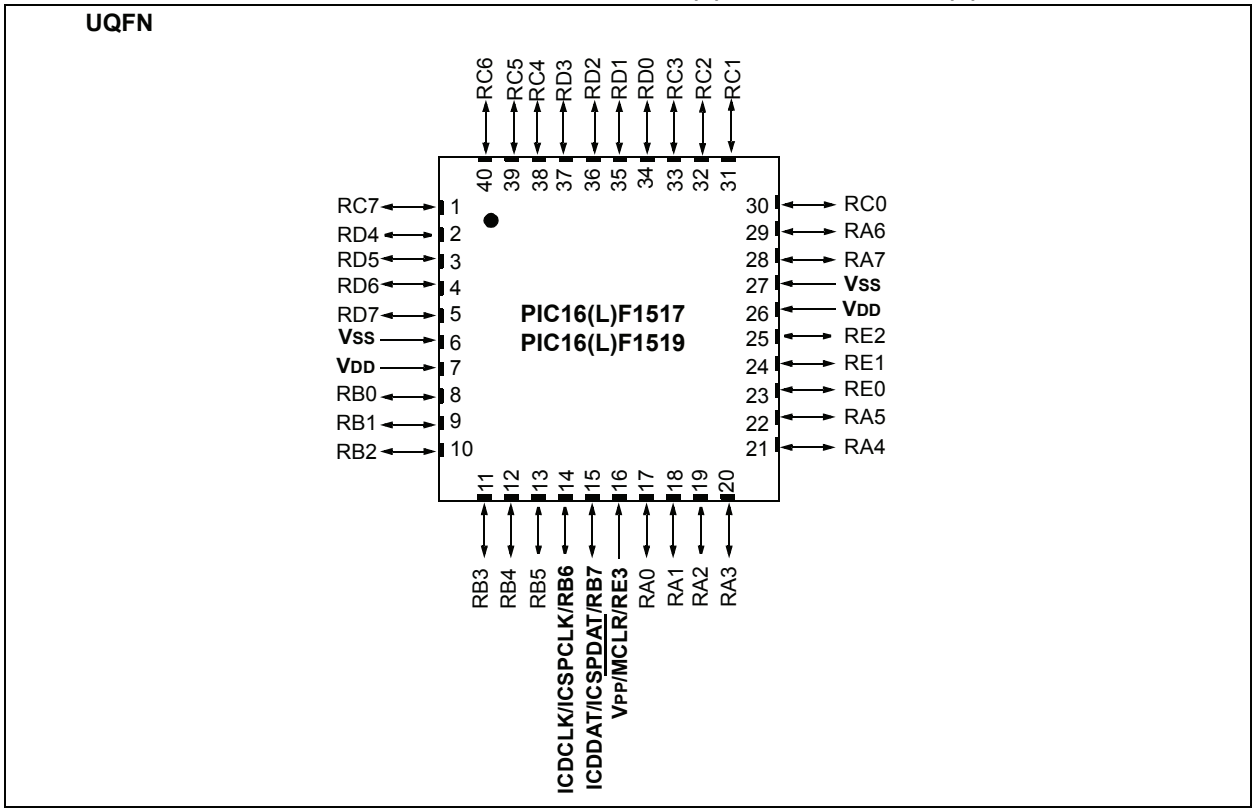


FIGURE 2-4: 40-PIN UQFN DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519



3.0 MEMORY MAP

The memory for the PIC16(L)F151X/152X devices is broken into two sections: program memory and configuration memory. Only the size of the program memory changes between devices, the configuration memory remains the same.

FIGURE 3-1: PIC16(L)F1512 PROGRAM MEMORY MAPPING

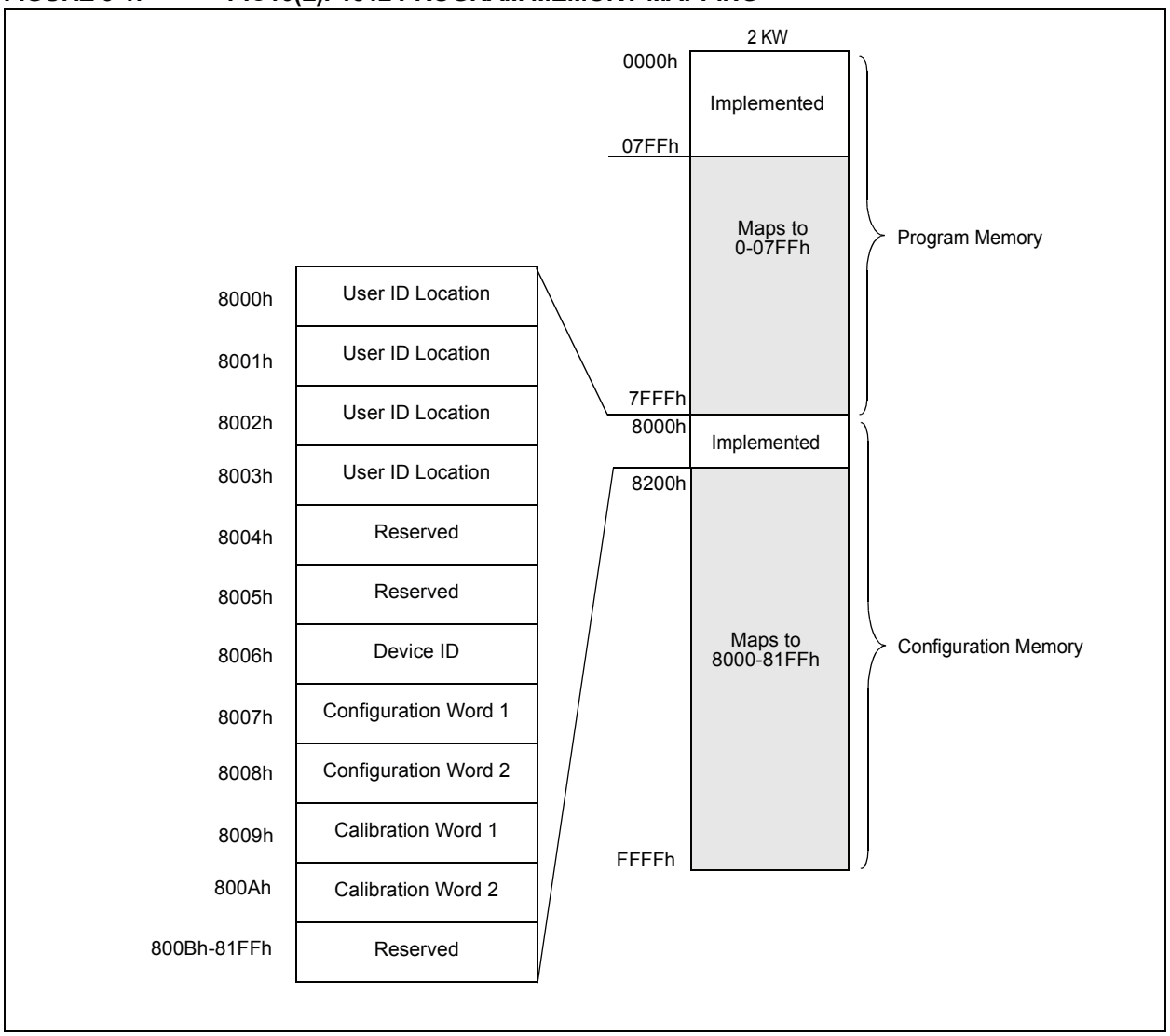


FIGURE 3-2: PIC16(L)F1513 PROGRAM MEMORY MAPPING

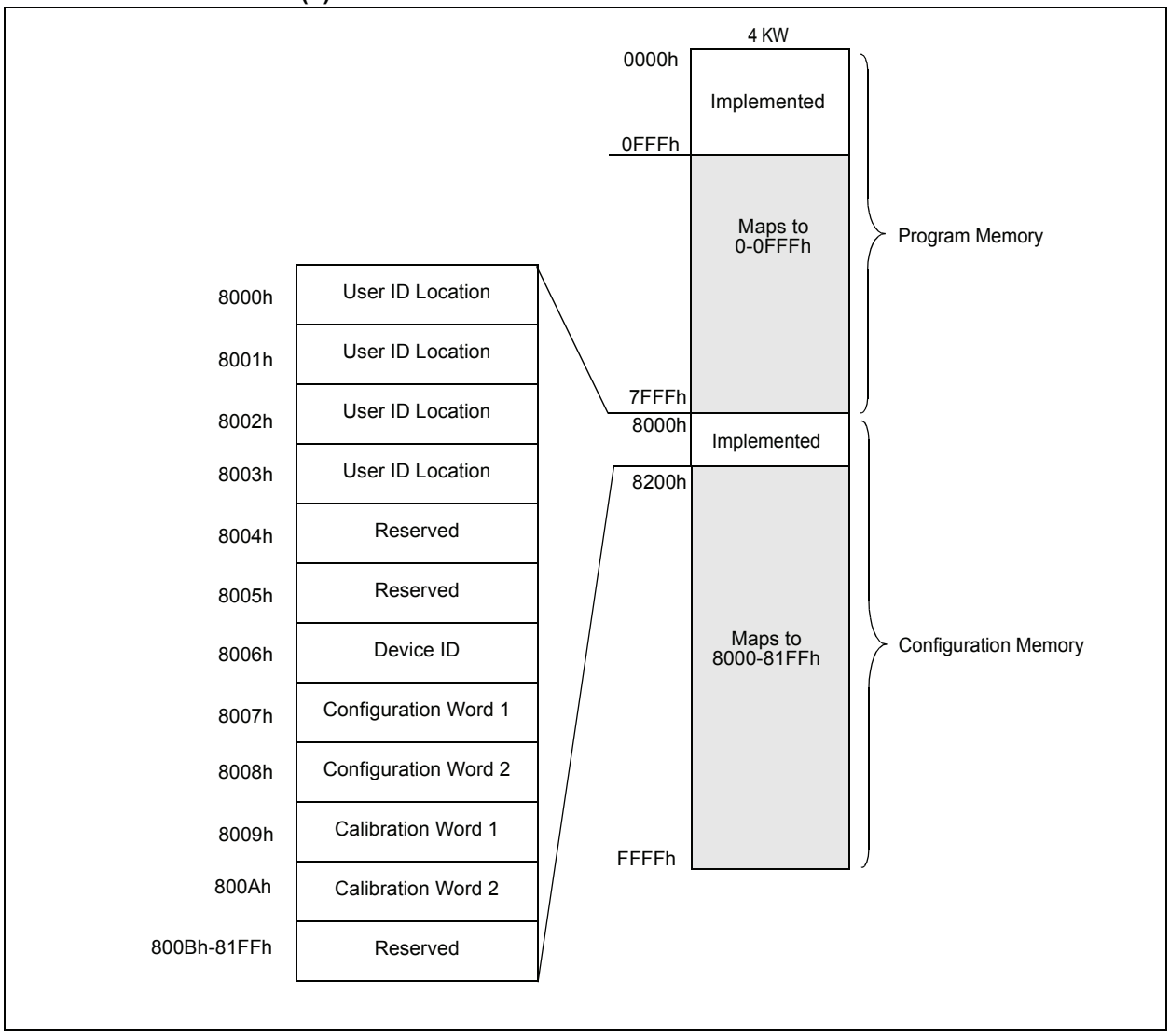


FIGURE 3-3: PIC16(L)F1526, PIC16(L)F1516 AND PIC16(L)F1517 PROGRAM MEMORY MAPPING

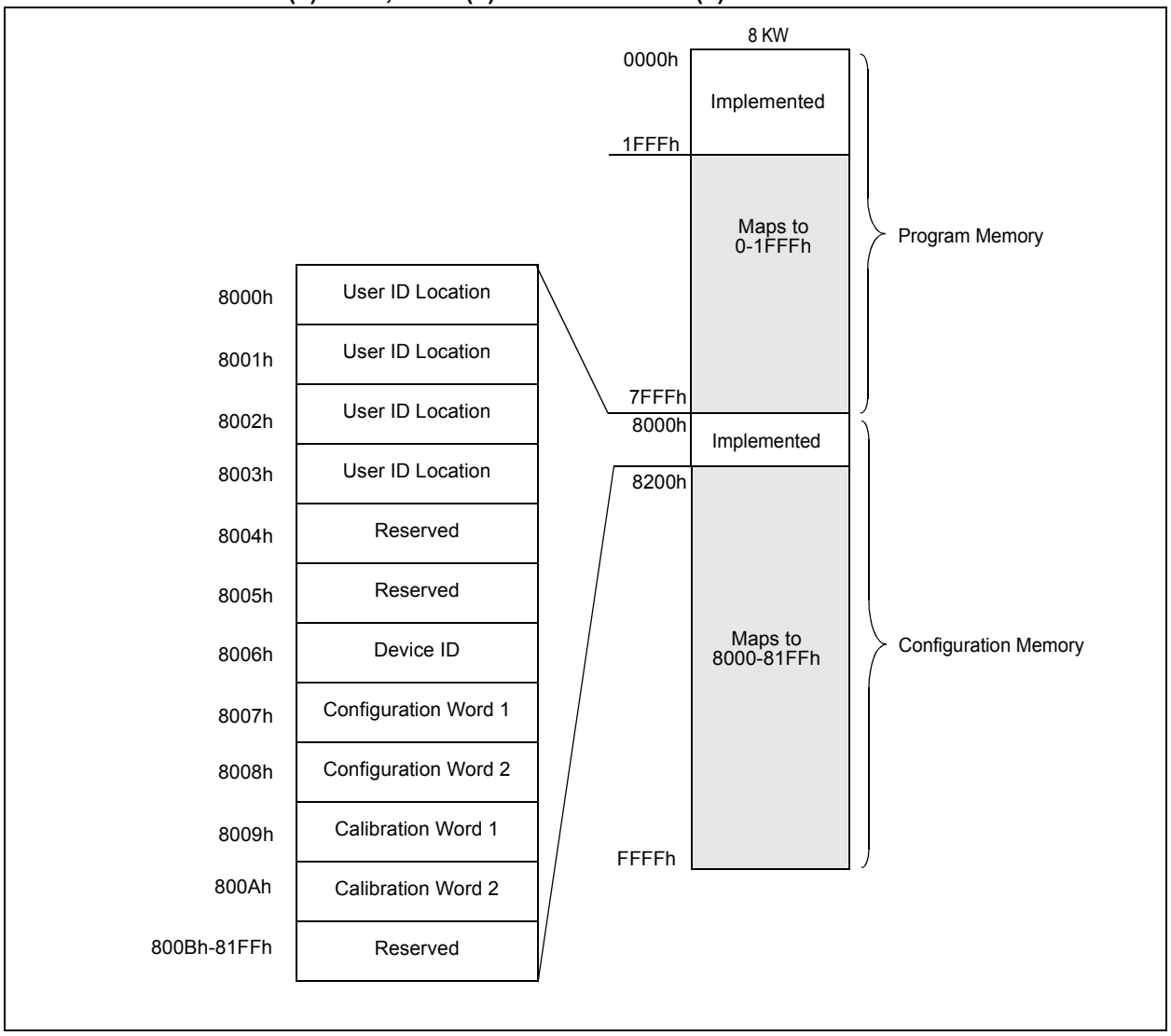
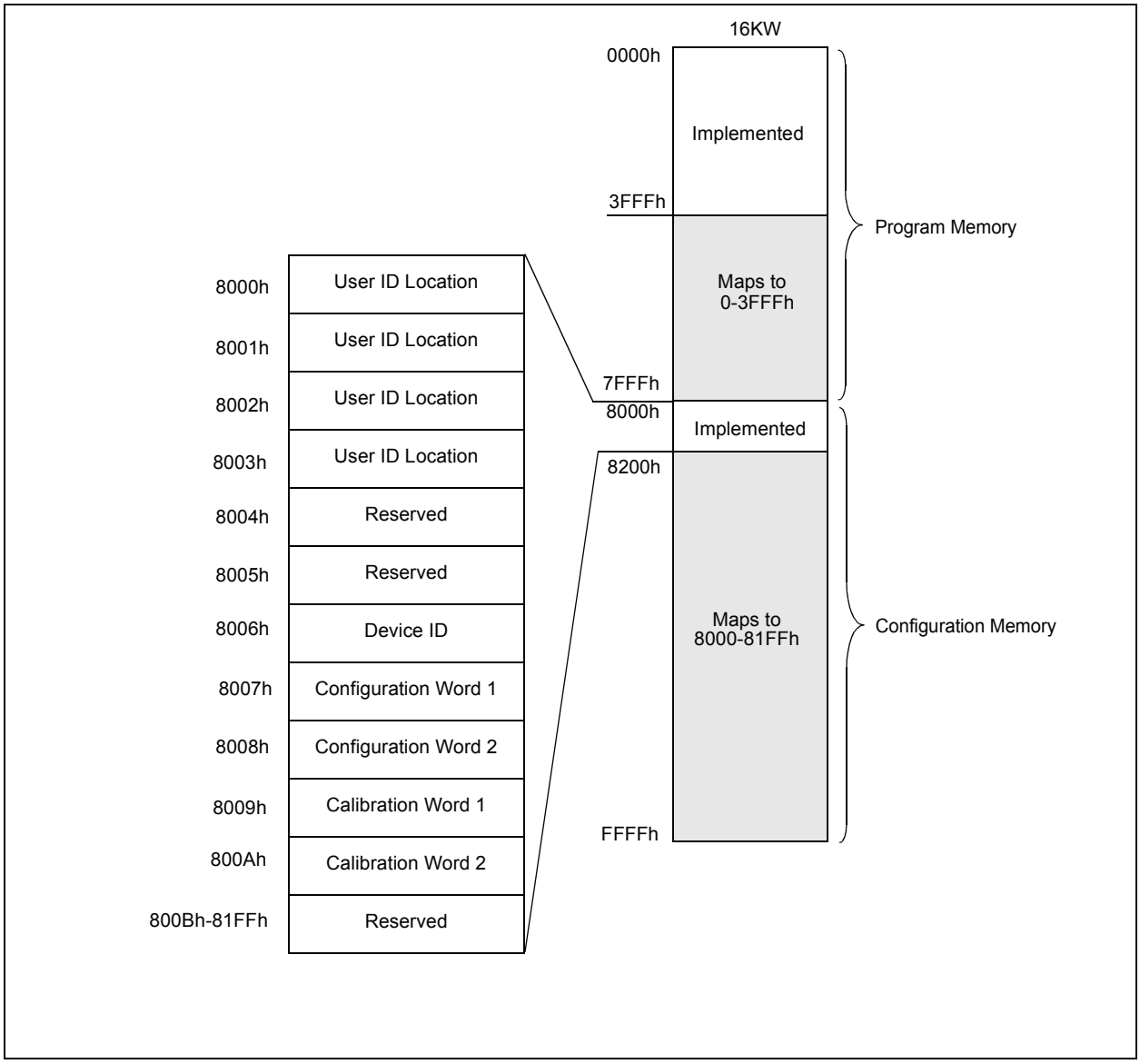


FIGURE 3-4: PIC16(L)F1527, PIC16(L)F1518 AND PIC16(L)F1519 PROGRAM MEMORY MAPPING



3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

Note:	MPLAB® IDE only displays the 7 Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the 7 LSbs be used if MPLAB IDE is the primary tool used to read these addresses.

3.2 Device ID

The device ID word is located at 8006h. This location is read-only and cannot be erased or modified.

REGISTER 3-1: DEVICE ID: DEVICE ID REGISTER(1)

R	R	R	R	R	R
DEV<8:3>					
bit 13					bit 8

R	R	R	R	R	R	R	R
DEV<2:0>			REV<4:0>				
bit 7							bit 0

Legend:	P = Programmable bit	U = Unimplemented bit, read as ‘0’
R = Readable bit	W = Writable bit	‘0’ = Bit is cleared
-n = Value at POR	‘1’ = Bit is set	x = Bit is unknown

bit 13-5 **DEV<8:0>:** Device ID bits
These bits are used to identify the part number.

bit 4-0 **REV<4:0>:** Revision ID bits
These bits are used to identify the revision.

Note 1: This location cannot be written.

TABLE 3-1: DEVICE ID VALUES

DEVICE	DEVICE ID VALUES	
	DEV	REV
PIC16F1527	0001 0101 101	x xxxx
PIC16F1526	0001 0101 100	x xxxx
PIC16LF1527	0001 0101 111	x xxxx
PIC16LF1526	0001 0101 110	x xxxx
PIC16F1519	0001 0110 111	x xxxx
PIC16F1518	0001 0110 110	x xxxx
PIC16F1517	0001 0110 101	x xxxx
PIC16F1516	0001 0110 100	x xxxx
PIC16F1513	0001 0110 010	x xxxx
PIC16F1512	0001 0111 000	x xxxx
PIC16LF1519	0001 0111 111	x xxxx
PIC16LF1518	0001 0111 110	x xxxx
PIC16LF1517	0001 0111 101	x xxxx
PIC16LF1516	0001 0111 100	x xxxx
PIC16LF1513	0001 0111 010	x xxxx
PIC16LF1512	0001 0111 001	x xxxx

3.3 Configuration Words

There are two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

The internal calibration values are factory calibrated and stored in Calibration Words 1 and 2 (8009h, 800Ah).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

REGISTER 3-3: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
LVP	$\overline{\text{DEBUG}}$	$\overline{\text{LPBOR}}$	BORV	STVREN	—
bit 13					bit 8

U-1	U-1	U-1	R/P-1	U-1	U-1	R/P-1	R/P-1
—	—	—	$\overline{\text{VCAPEN}}$(2)	—	—	WRT<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **LVP:** Low-Voltage Programming Enable bit(1)
1 = Low-voltage programming enabled
0 = HV on $\overline{\text{MCLR}}$/VPP must be used for programming

bit 12 **$\overline{\text{DEBUG}}$:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
0 = In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger

bit 11 **$\overline{\text{LPBOR}}$:** Low-Power BOR
1 = Low-Power BOR is disabled
0 = Low-Power BOR is enabled

bit 10 **BORV:** Brown-out Reset Voltage Selection bit
1 = Brown-out Reset voltage (VBOR), low trip point selected
0 = Brown-out Reset voltage (VBOR), high trip point selected

bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
1 = Stack Overflow or Underflow will cause a Reset
0 = Stack Overflow or Underflow will not cause a Reset

bit 8-5 **Unimplemented:** Read as '1'

bit 4 **$\overline{\text{VCAPEN}}$:** Voltage Regulator Capacitor Enable bits(1)
0 = VCAP functionality is enabled on VCAP pin
1 = All VCAP pin functions are disabled

bit 3-2 **Unimplemented:** Read as '1'

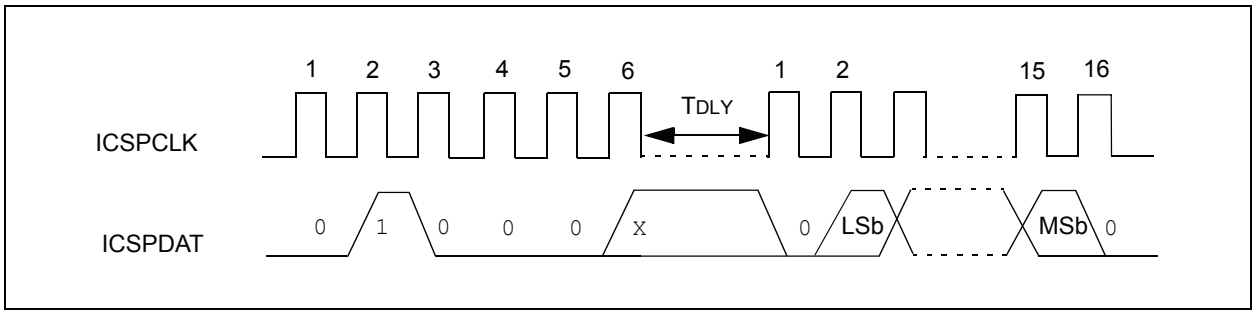
bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits
2 kW Flash memory (PIC16(L)F1512):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
01 = 000h to FFFh write-protected, 400h to 7FFh may be modified by PMCON control
00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control
4 kW Flash memory (PIC16(L)F1513):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control
01 = 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control
00 = 000h to FFFh write-protected, no addresses may be modified by PMCON control
8 kW Flash memory (PIC16F/LF1516/1517/1526):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 1FFFh may be modified by PMCON control
01 = 000h to FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control
00 = 000h to 1FFFh write-protected, no addresses may be modified by PMCON control
16 kW Flash memory (PIC16F/LF1518/1519/1527):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 3FFFh may be modified by PMCON control
01 = 000h to 1FFFh write-protected, 2000h to 3FFFh may be modified by PMCON control
00 = 000h to 3FFFh write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.
2: Applies to PIC16F151X/152X devices only. On PIC16LF151X/152X, the $\overline{\text{VCAPEN}}$ bit is unimplemented.

4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

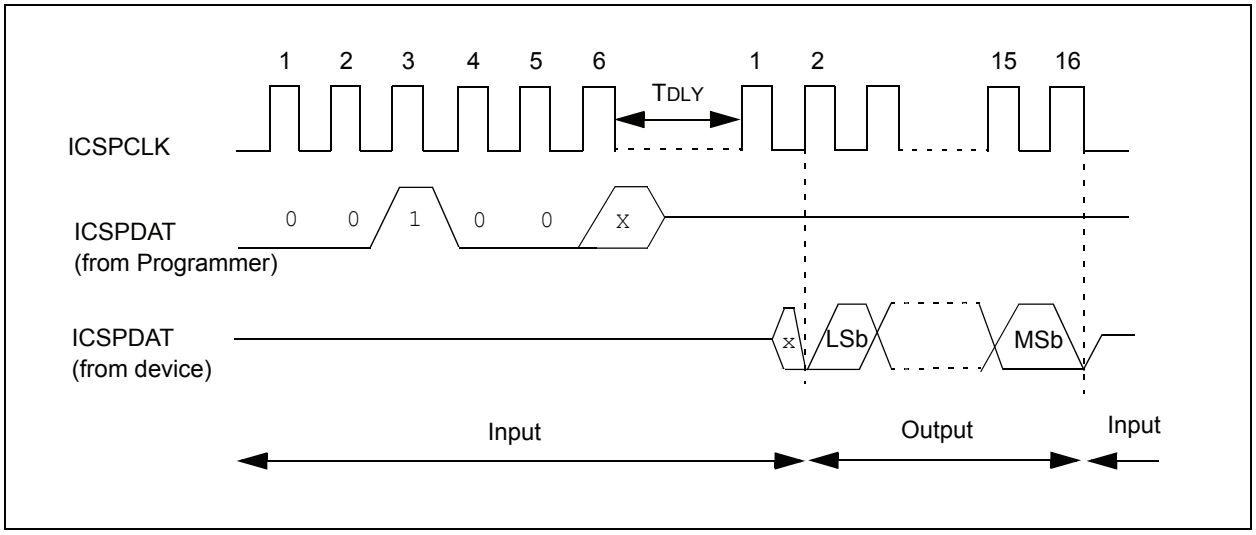
FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY



4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros (see Figure 4-3).

FIGURE 4-3: READ DATA FROM PROGRAM MEMORY



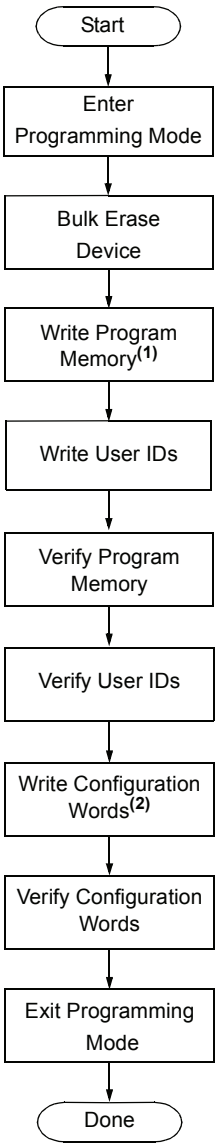
5.0 PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to Table 4-2 for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC's address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes cannot cross the physical boundary. For example, with the PIC16F1527, attempting to write from address 0002h-0009h will result in data being written to 0008h-000Fh.

If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART



Note 1: See Figure 5-2.

2: See Figure 5-5.

FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

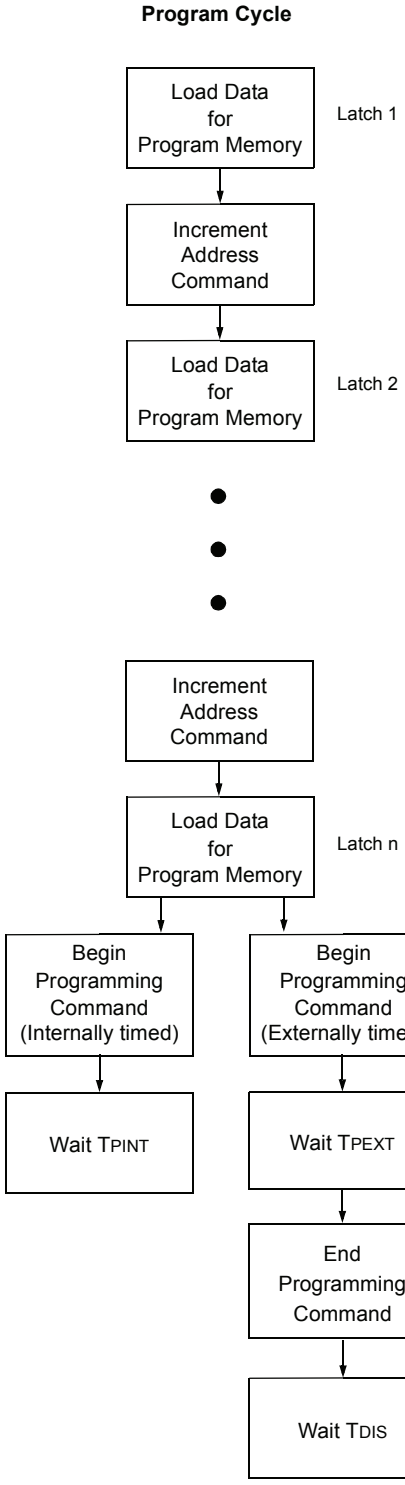
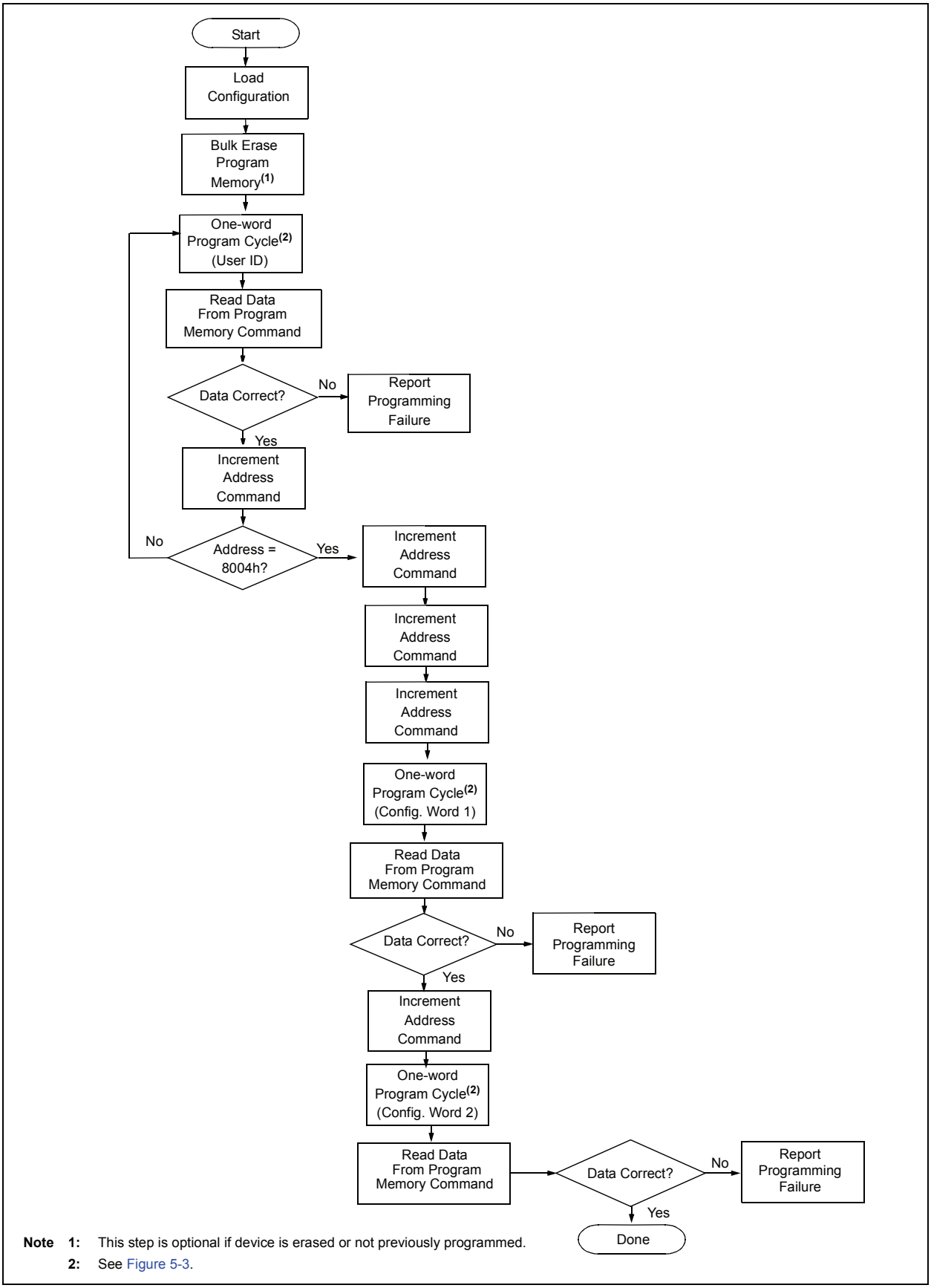


FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART



Note 1: This step is optional if device is erased or not previously programmed.

2: See Figure 5-3.

7.3.2 PROGRAM CODE PROTECTION ENABLED

With the program code protection enabled, the checksum is computed in the following manner: The Least Significant nibble of each user ID is used to create a 16-bit value. The masked value of user ID location 8000h is the Most Significant nibble. This sum of user IDs is summed with the Configuration Words (all unimplemented Configuration bits are masked to '0').

EXAMPLE 7-3: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC16F1527, BLANK DEVICE

PIC16F1527	Configuration Word 1(2)	3F7Fh
	Configuration Word 1 mask(3)	3EFFh
	Configuration Word 2(2)	3FFFh
	Configuration Word 2 mask(3)	3E13h
	User ID (8000h)(1)	0006h
	User ID (8001h)(1)	0007h
	User ID (8002h)(1)	0001h
	User ID (8003h)(1)	0002h
	Sum of User IDs(4)	= (0006h and 000Fh) << 12 + (0007h and 000Fh) << 8 + (0001h and 000Fh) << 4 + (0002h and 000Fh)
		= 6000h + 0700h + 0010h + 0002h
		= 6712h
	Checksum	= (3F7Fh and 3EFFh) + (3FFFh and 3E13h) + Sum of User IDs
		= 3E7Fh +3713h + 6712h
		= DCA4h

Note 1: User ID values in this example are random values.

2: Configuration Word 1 and 2 = all bits are '1' except the code-protect enable bit.

3: Configuration Word 1 and 2 Mask = all Configuration Word bits are set to '1', except for unimplemented bits which read '0'.

4: << = shift left, thus the LSb of the first user ID value is the MSb of the sum of user IDs and so on, until the LSb of the last user ID value becomes the LSb of the sum of user IDs.

EXAMPLE 7-4: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC16LF1527, 00AAh AT FIRST AND LAST ADDRESS

PIC16LF1527	Configuration Word 1(2)	3F7Fh
	Configuration Word 1 mask(3)	3EFFh
	Configuration Word 2(2)	3FFFh
	Configuration Word 2 mask(3), (5)	3E03h
	User ID (8000h)(1)	000Eh
	User ID (8001h)(1)	0008h
	User ID (8002h)(1)	0005h
	User ID (8003h)(1)	0008h
	Sum of User IDs(4)	= (000Eh and 000Fh) << 12 + (0008h and 000Fh) << 8 + (0005h and 000Fh) << 4 + (0008h and 000Fh) = E000h + 0800h + 0050h + 0008h = E858h
	Checksum	= (3F7Fh and 3EFFh) + (3FFFh and 3E03h) + Sum of User IDs = 3E7Fh +3E03h + E858h = 64DAh

Note 1: User ID values in this example are random values.

2: Configuration Word 1 and 2 = all bits are '1' except the code-protect enable bit.

3: Configuration Word 1 and 2 Mask = all Configuration Word bits are set to '1', except for unimplemented bits which read '0'.

4: << = shift left, thus the LSb of the first user ID value is the MSb of the sum of user IDs and so on, until the LSb of the last user ID value becomes the LSb of the sum of user IDs.

5: On the PIC16LF1527 device, the $\overline{\text{VCAPEN}}$ bit is not implemented in Configuration Word 2; thus, all unimplemented bits are '0'.

8.0 ELECTRICAL SPECIFICATIONS

Refer to device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS			Standard Operating Conditions Production tested at 25°C				
Sym.	**Characteristics**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
Supply Voltages and Currents							
V_{DD}	Supply Voltage (V_{DDMIN}, V_{DDMAX})	PIC16F151X PIC16F152X	2.3	—	5.5	V	
		PIC16LF151X PIC16LF152X	1.8	—	3.6	V	
V_{PEW}	Read/Write and Row Erase operations		V_{DDMIN}	—	V_{DDMAX}	V	
V_{PBE}	Bulk Erase operations		2.7	—	V_{DDMAX}	V	
I_{DDI}	Current on V_{DD}, Idle		—	—	1.0	mA	
I_{DDP}	Current on V_{DD}, Programming		—	—	3.0	mA	
	V_{PP}						
I_{PP}	Current on $\overline{MCLR}/V_{PP}$		—	—	600	μA	
V_{IHH}	High voltage on $\overline{MCLR}/V_{PP}$ for Program/Verify mode entry		8.0	—	9.0	V	
T_{VHHR}	$\overline{MCLR}$ rise time (V_{IL} to V_{IHH}) for Program/Verify mode entry		—	—	1.0	μs	
	I/O pins						
V_{IH}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) input high level		0.8 V_{DD}	—	—	V	
V_{IL}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) input low level		—	—	0.2 V_{DD}	V	
V_{OH}	ICSPDAT output high level		V_{DD}-0.7 V_{DD}-0.7 V_{DD}-0.7	—	—	V	I_{OH} = 3.5 mA, V_{DD} = 5V I_{OH} = 3 mA, V_{DD} = 3.3V I_{OH} = 2 mA, V_{DD} = 1.8V
V_{OL}	ICSPDAT output low level		—	—	V_{SS}+0.6 V_{SS}+0.6 V_{SS}+0.6	V	I_{OH} = 8 mA, V_{DD} = 5V I_{OH} = 6 mA, V_{DD} = 3.3V I_{OH} = 3 mA, V_{DD} = 1.8V
Programming Mode Entry and Exit							
T_{ENTS}	Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before V_{DD} or $\overline{MCLR}$↑		100	—	—	ns	
T_{ENTH}	Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after V_{DD} or $\overline{MCLR}$↑		250	—	—	μs	
Serial Program/Verify							
T_{CKL}	Clock Low Pulse Width		100	—	—	ns	
T_{CKH}	Clock High Pulse Width		100	—	—	ns	
T_{DS}	Data in setup time before clock↓		100	—	—	ns	
T_{DH}	Data in hold time after clock↓		100	—	—	ns	
T_{CO}	Clock↑ to data out valid (during a Read Data command)		0	—	80	ns	
T_{LZD}	Clock↓ to data low-impedance (during a Read Data command)		0	—	80	ns	
T_{HZD}	Clock↓ to data high-impedance (during a Read Data command)		0	—	80	ns	
T_{DLY}	Data input not driven to next clock input (delay required between command/data or command/command)		1.0	—	—	μs	
T_{ERAB}	Bulk Erase cycle time		—	—	5	ms	
T_{ERAR}	Row Erase cycle time		—	—	2.5	ms	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

FIGURE 8-8: LVP ENTRY (POWERED)

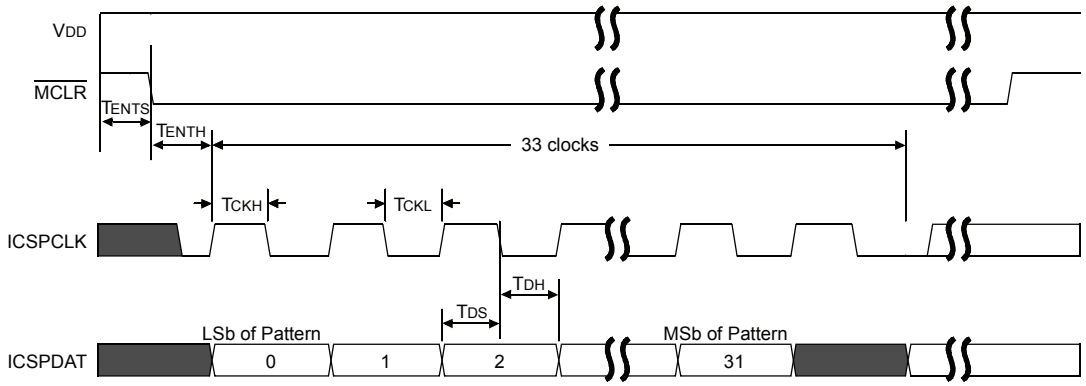
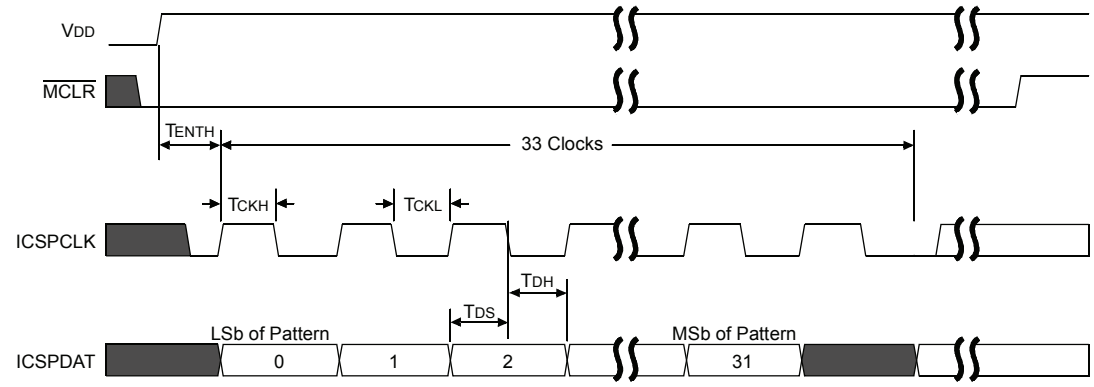


FIGURE 8-9: LVP ENTRY (POWERING UP)



Note 1: Sequence matching can start with no edge on $\overline{MCLR}$ first.

APPENDIX A: REVISION HISTORY

Revision A (08/2010)

Original release of this document.

Revision B (09/2011)

Added PIC16(L)F1512/1513 devices; Added new Figures 3-1 and 3-2; Updated Registers 3-1, 3-2 and 3-3 to new format; Updated Register 3-3 to add 2 kW and 4 kW Flash memory; Added Notes to Examples 7-1 to 7-4; Updated Table 8-1; Other minor corrections.

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