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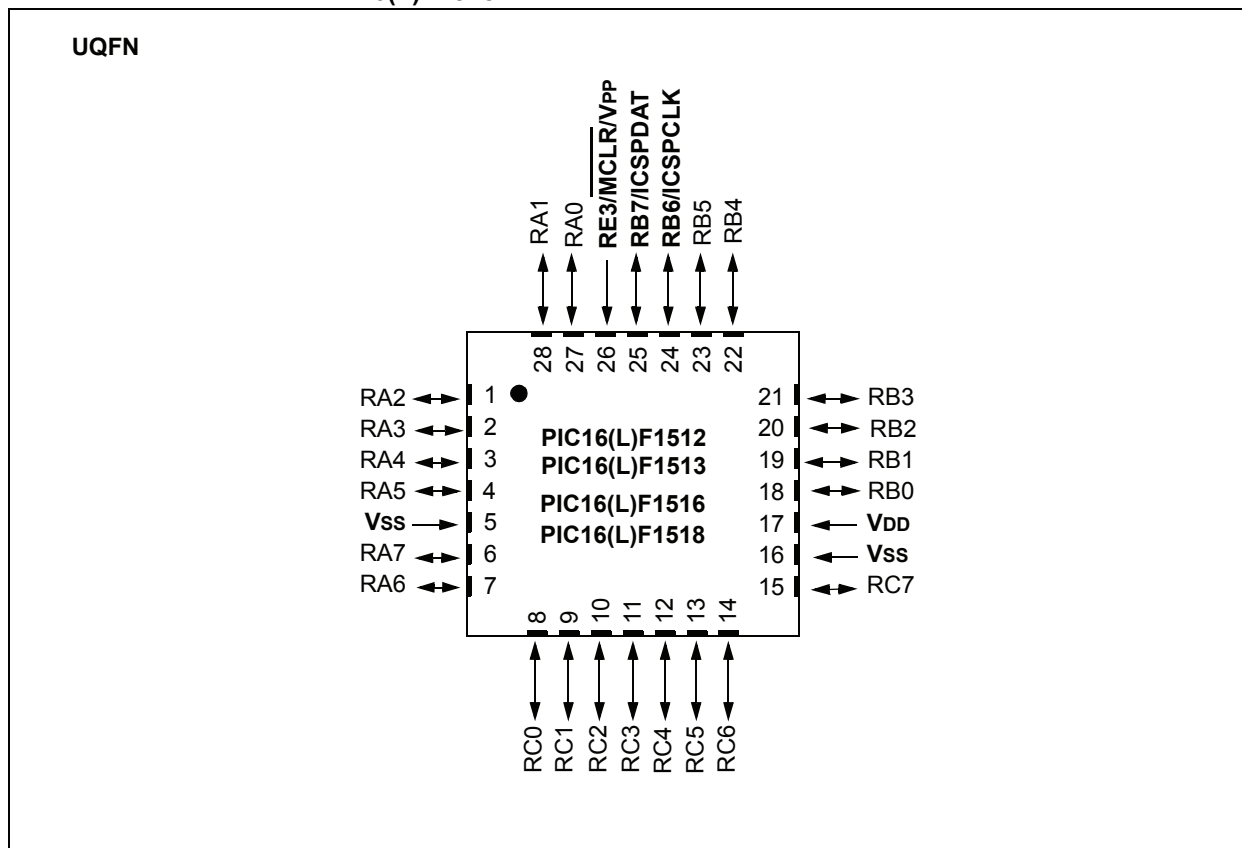
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1516t-i-mv

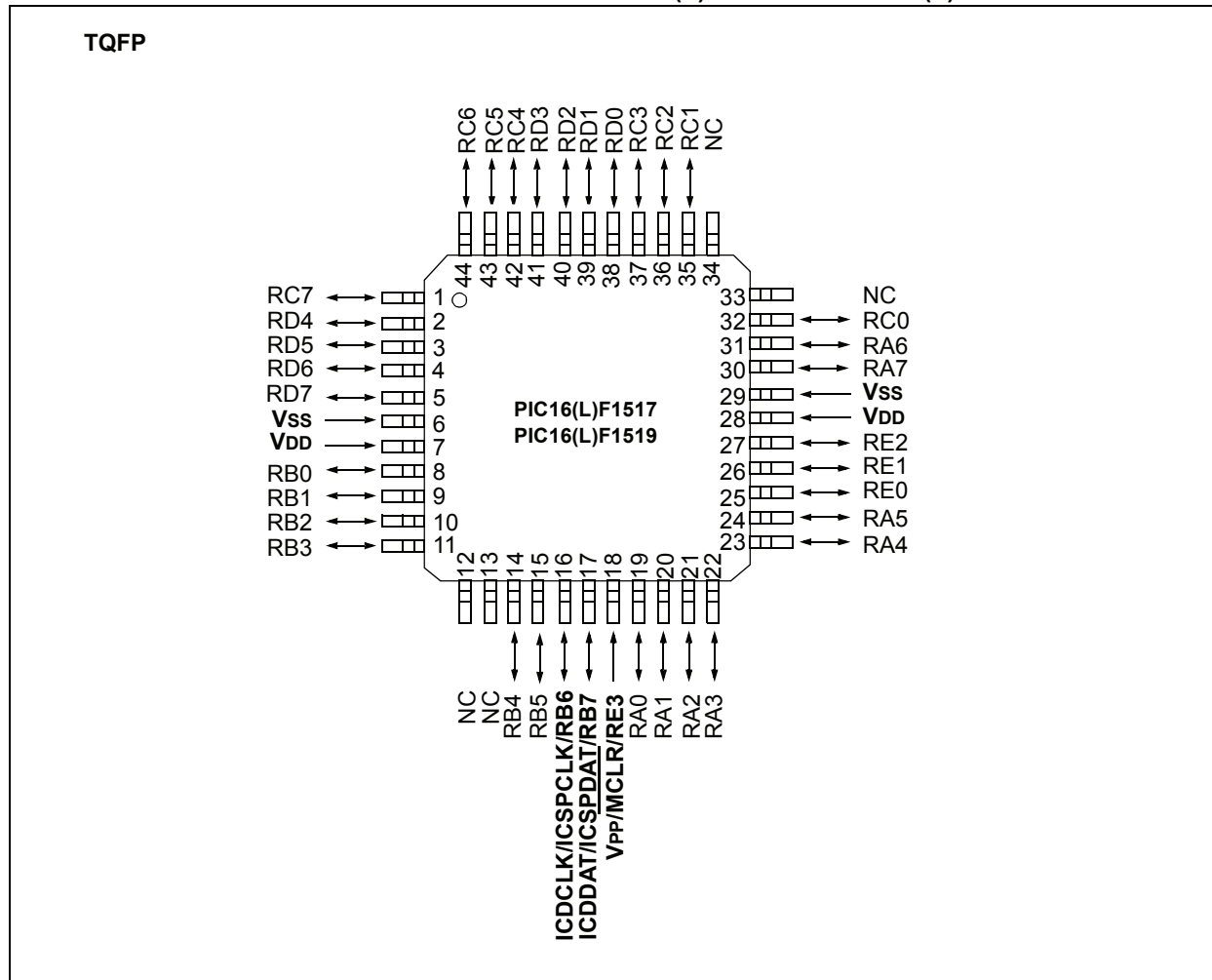
PIC16(L)F151X/152X

FIGURE 2-2: 28-PIN UQFN DIAGRAM FOR PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516 AND PIC16(L)F1518



PIC16(L)F151X/152X

FIGURE 2-5: 44-PIN TQFP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519



PIC16(L)F151X/152X

FIGURE 2-6: 64-PIN QFN DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527

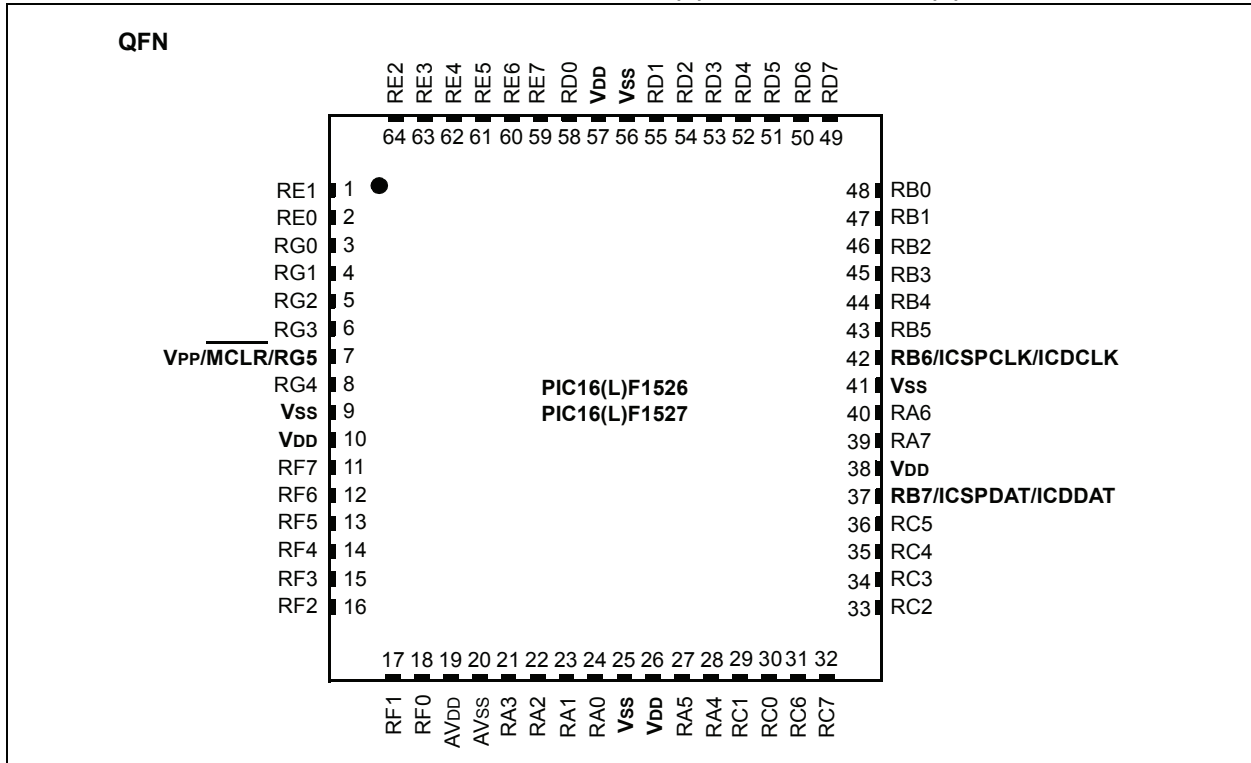
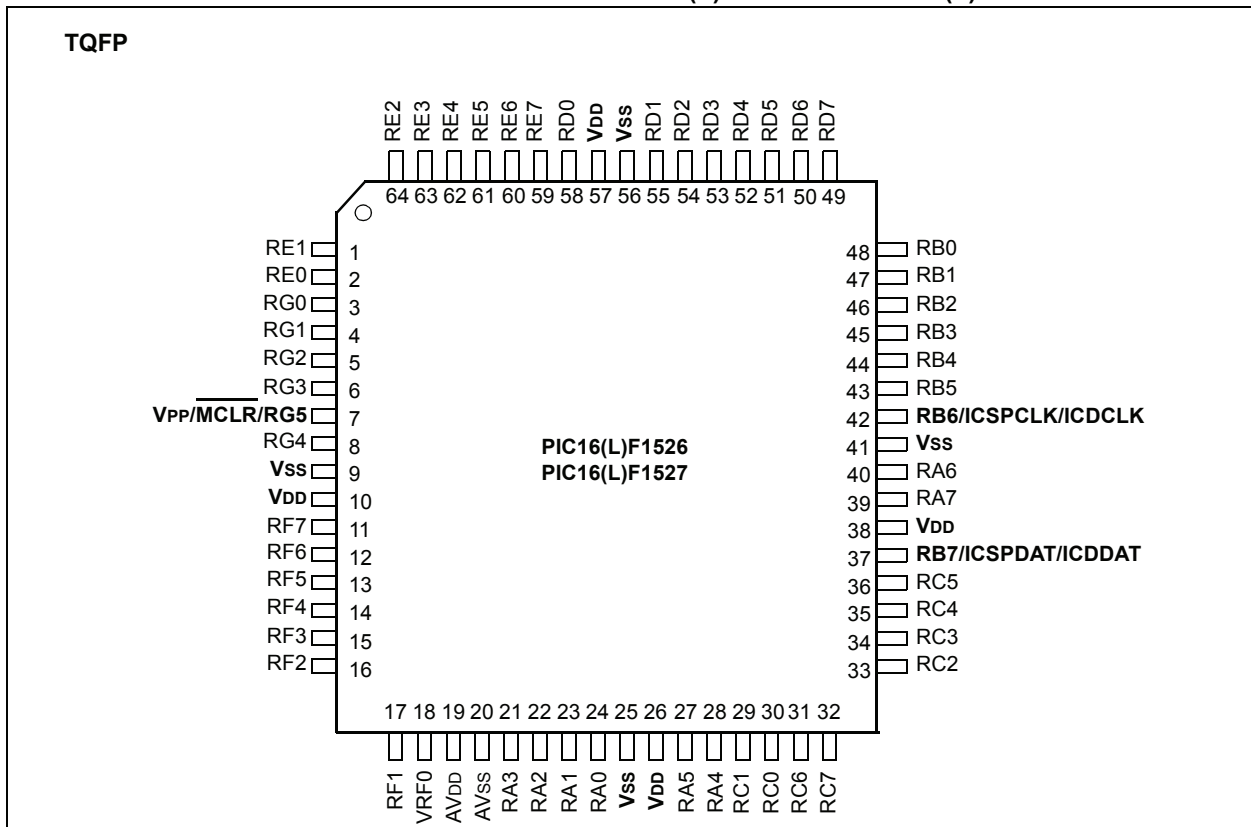


FIGURE 2-7: 64-PIN TQFP DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527



PIC16(L)F151X/152X

3.0 MEMORY MAP

The memory for the PIC16(L)F151X/152X devices is broken into two sections: program memory and configuration memory. Only the size of the program memory changes between devices, the configuration memory remains the same.

FIGURE 3-1: PIC16(L)F1512 PROGRAM MEMORY MAPPING

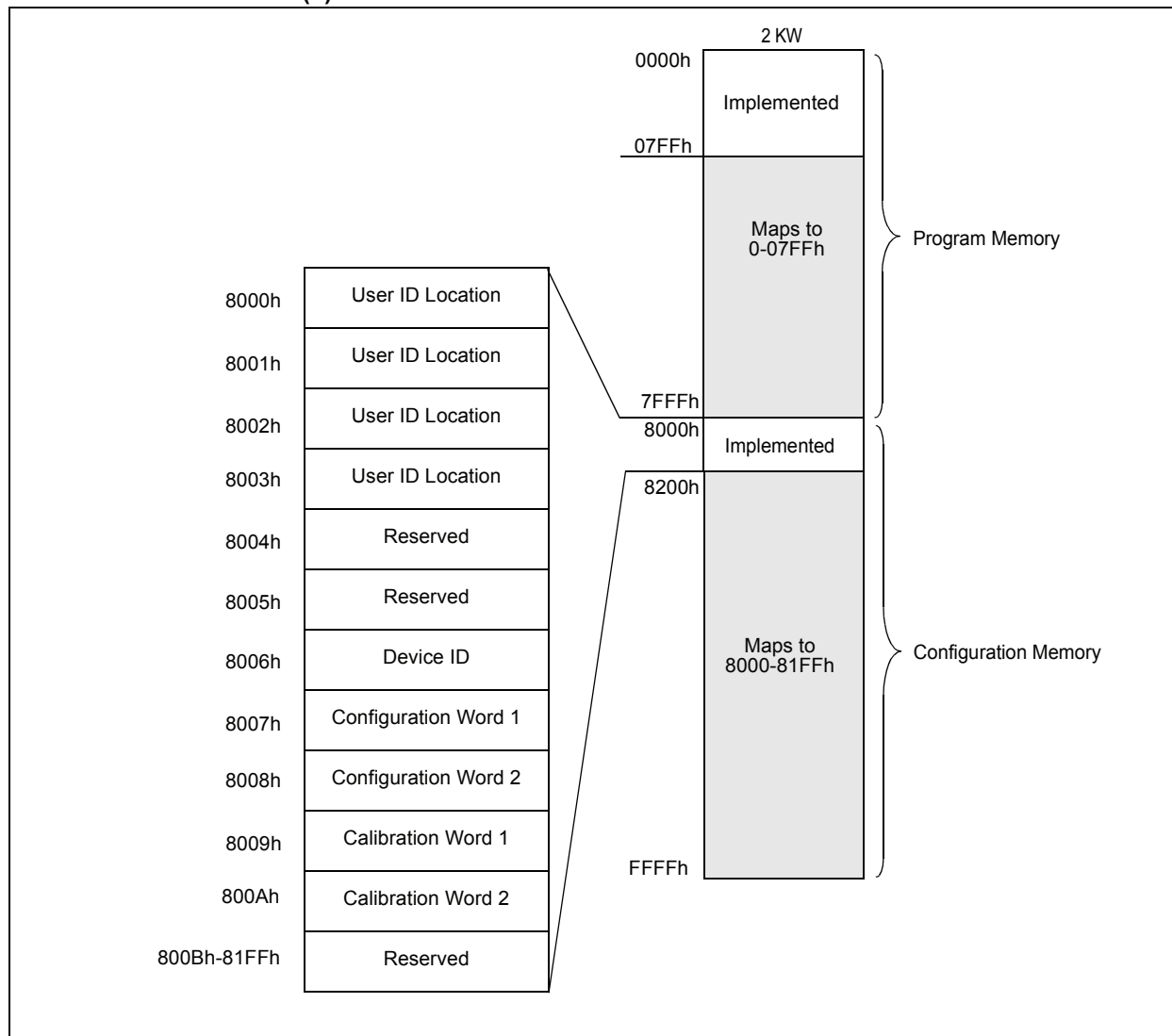
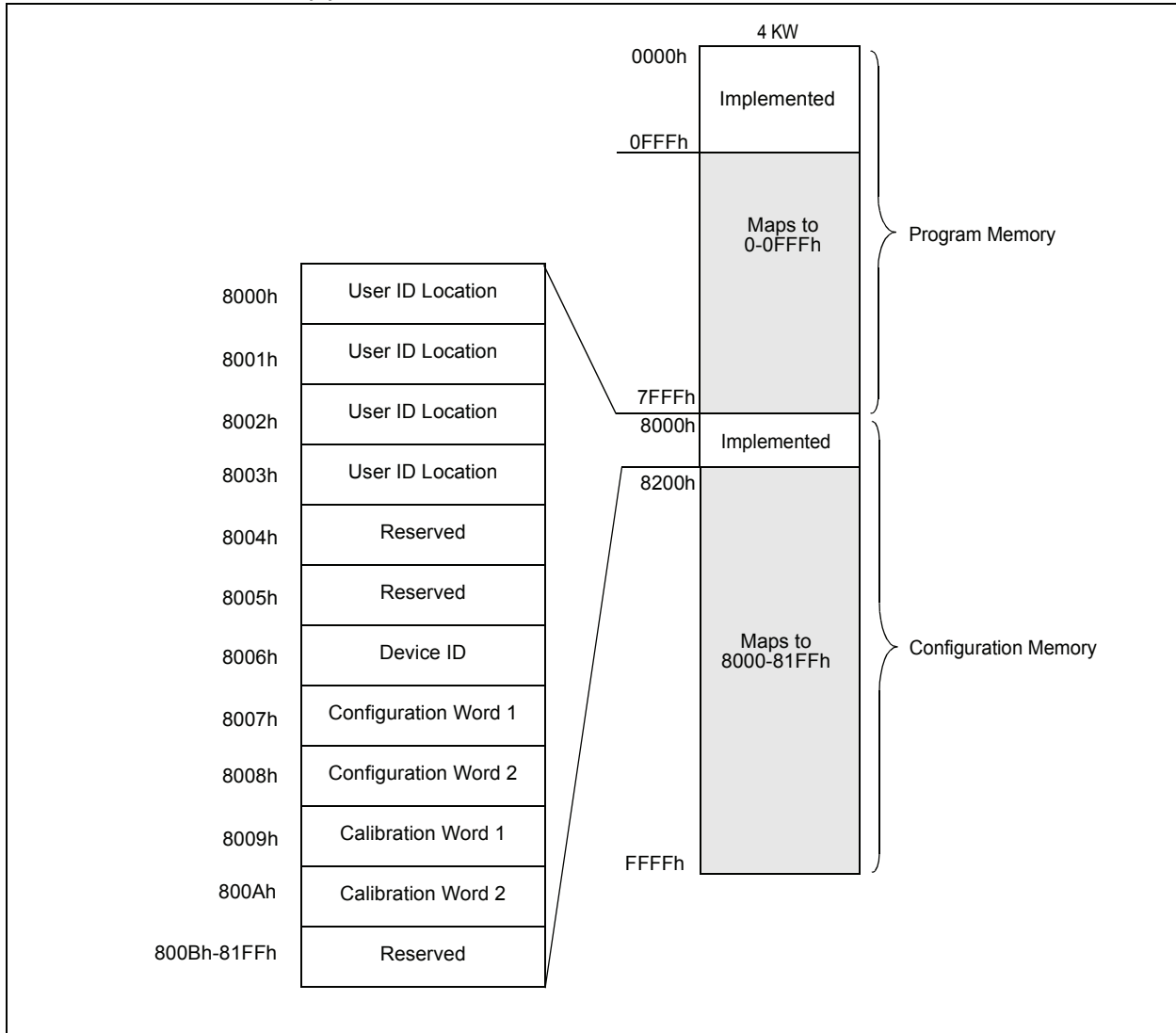


FIGURE 3-2: PIC16(L)F1513 PROGRAM MEMORY MAPPING



PIC16(L)F151X/152X

REGISTER 3-2: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
FCMEN	IESO	CLKOUTEN	BOREN<1:0>	—	
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP	MCLRE	PWRTÉ	WDTE<1:0>	FOSC<2:0>			
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '1'
 '0' = Bit is cleared '1' = Bit is set -n = Value when blank or after Bulk Erase

- bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
 1 = Fail-Safe Clock Monitor is enabled
 0 = Fail-Safe Clock Monitor is disabled
- bit 12 **IESO:** Internal External Switchover bit
 1 = Internal/External Switchover mode is enabled
 0 = Internal/External Switchover mode is disabled
- bit 11 **CLKOUTEN:** Clock Out Enable bit
 1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
 0 = CLKOUT function is enabled on CLKOUT pin
- bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits⁽¹⁾
 11 = BOR enabled
 10 = BOR enabled during operation and disabled in Sleep
 01 = BOR controlled by SBOREN bit of the PCON register
 00 = BOR disabled
- bit 8 **Unimplemented:** Read as '1'
- bit 7 **CP:** Code Protection bit⁽²⁾
 1 = Program memory code protection is disabled
 0 = Program memory code protection is enabled
- bit 6 **MCLRE:** MCLR/VPP Pin Function Select bit
 If LVP bit = 1:
 This bit is ignored.
 If LVP bit = 0:
 1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
 0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUA register.
- bit 5 **PWRTÉ:** Power-up Timer Enable bit⁽¹⁾
 1 = PWRT disabled
 0 = PWRT enabled
- bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
 11 = WDT enabled
 10 = WDT enabled while running and disabled in Sleep
 01 = WDT controlled by the SWDTEN bit in the WDTCON register
 00 = WDT disabled
- bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
 111 = ECH: External Clock, High-Power mode: on CLKIN pin
 110 = ECM: External Clock, Medium-Power mode: on CLKIN pin
 101 = ECL: External Clock, Low-Power mode: on CLKIN pin
 100 = INTOSC oscillator: I/O function on OSC1 pin
 011 = EXTRC oscillator: RC function on OSC1 pin
 010 = HS oscillator: High-speed crystal/resonator on OSC2 pin and OSC1 pin
 001 = XT oscillator: Crystal/resonator on OSC2 pin and OSC1 pin
 000 = LP oscillator: Low-power crystal on OSC2 pin and OSC1 pin

- Note** 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
 2: The entire program memory will be erased when the code protection is turned off.

PIC16(L)F151X/152X

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted Lsb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to V_{IH} .
3. Raise the voltage on VDD FROM 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when Configuration Word 1 has $\overline{\text{MCLR}}$ disabled ($\text{MCLRE} = 0$), the power-up time is disabled ($\text{PWRT} = 0$), the internal oscillator is selected ($\text{FOSC} = 100$), and ICSPCLK and ICSPDAT pins are driven by the user application, the device will execute code. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in [Figure 8-2](#).

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from VDD or below to V_{IH} .

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in [Figure 8-1](#).

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower (V_{IL}). See [Figures 8-3](#) and [8-4](#).

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the PIC16(L)F151X/152X devices to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to V_{IL} .
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at V_{IL} for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see [Figure 8-8](#) and [Figure 8-9](#).

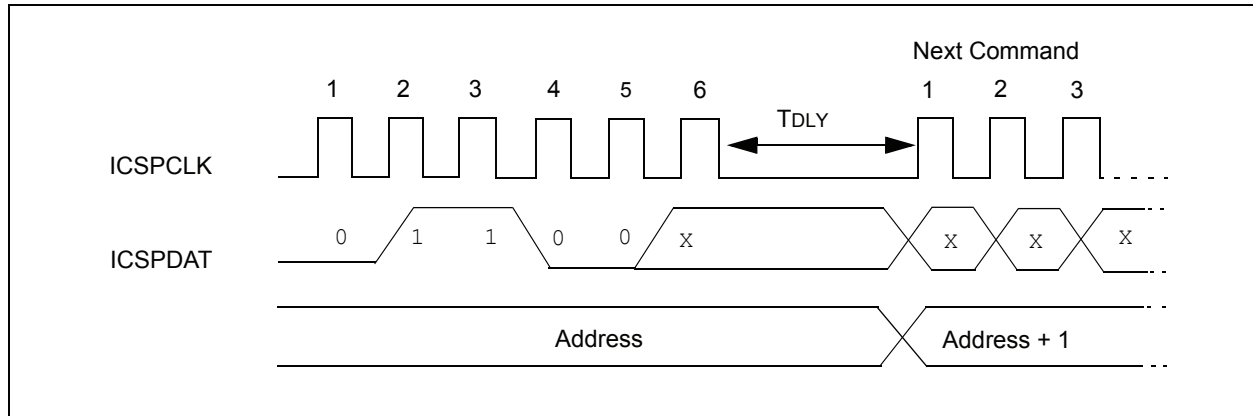
Exiting Program/Verify mode is done by no longer driving $\overline{\text{MCLR}}$ to V_{IL} . See [Figure 8-8](#) and [Figure 8-9](#).

Note: To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

4.3.4 INCREMENT ADDRESS

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it. If the address is incremented from address 7FFFh, it will wrap-around to location 0000h. If the address is incremented from FFFFh, it will wrap-around to location 8000h.

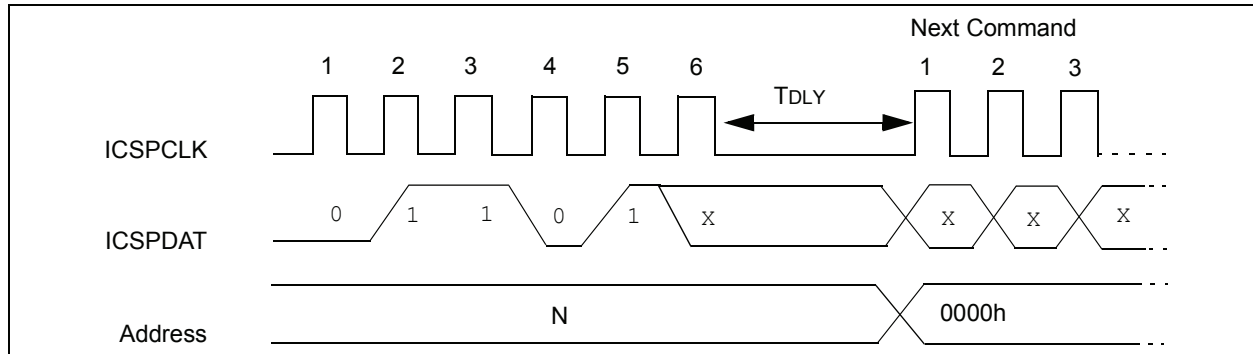
FIGURE 4-4: INCREMENT ADDRESS



4.3.5 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory.

FIGURE 4-5: RESET ADDRESS



PIC16(L)F151X/152X

4.3.10 ROW ERASE PROGRAM MEMORY

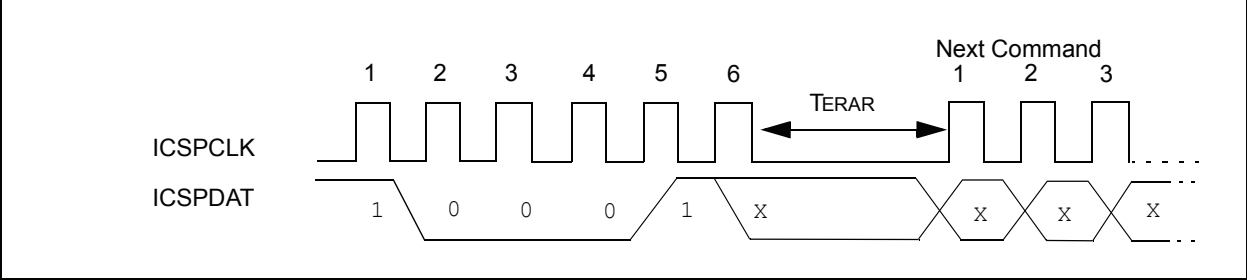
The Row Erase Program Memory command will erase an individual row. Refer to [Table 4-2](#) for row sizes of specific devices and the PC bits used to address them. If the program memory is code-protected the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h the Row Erase Program Memory command will only erase the user ID locations regardless of the setting of the \overline{CP} Configuration bit.

After receiving the Row Erase Program Memory command the erase will not complete until the time interval, T_{ERAR} , has expired.

TABLE 4-2: PROGRAMMING ROW SIZE AND LATCHES

Devices	PC	Row Size	Number of Latches
PIC16(L)F151X/152X	<15:5>	32	32

FIGURE 4-10: ROW ERASE PROGRAM MEMORY



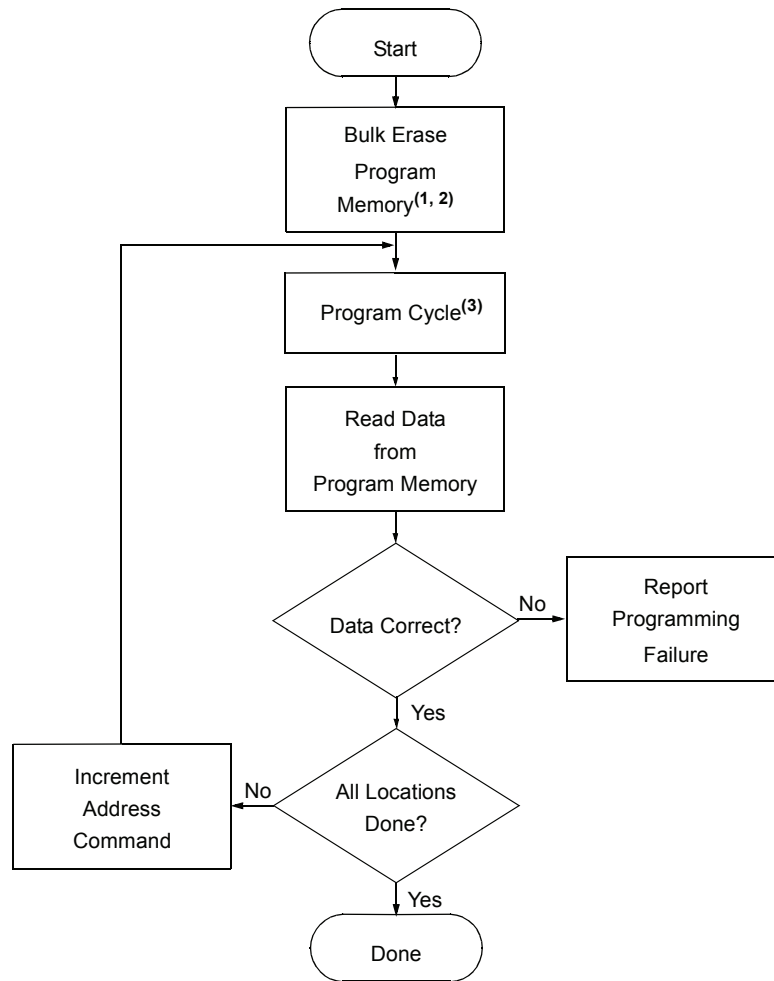
5.0 PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to [Table 4-2](#) for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC's address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes cannot cross the physical boundary. For example, with the PIC16F1527, attempting to write from address 0002h-0009h will result in data being written to 0008h-000Fh.

If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

FIGURE 5-2: PROGRAM MEMORY FLOWCHART



- Note 1:** This step is optional if device has already been erased or has not been previously programmed.
Note 2: If the device is code-protected or must be completely erased, then Bulk Erase device per [Figure 5-6](#).
Note 3: See [Figure 5-3](#) or [Figure 5-4](#).

PIC16(L)F151X/152X

FIGURE 5-3: ONE-WORD PROGRAM CYCLE

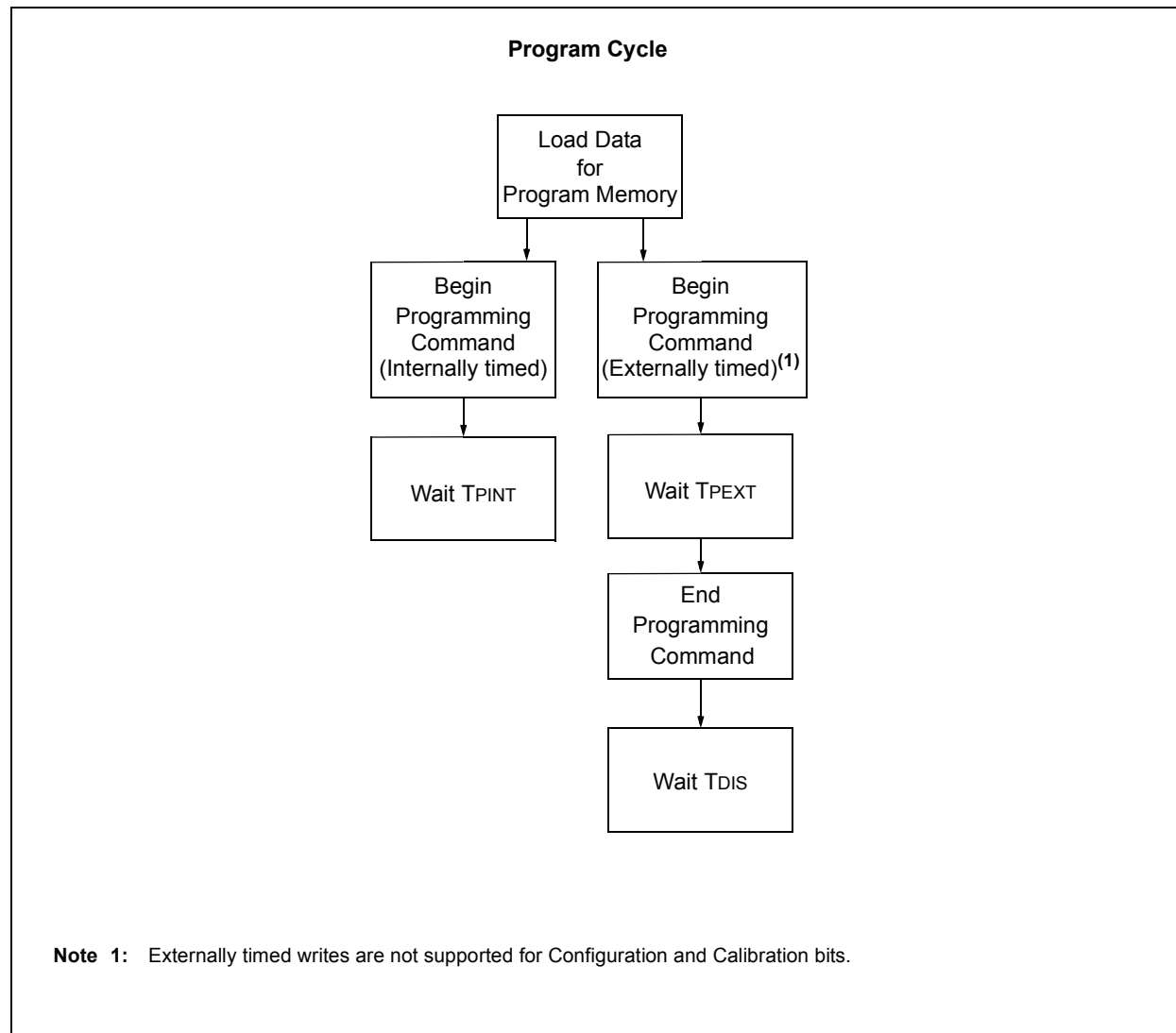
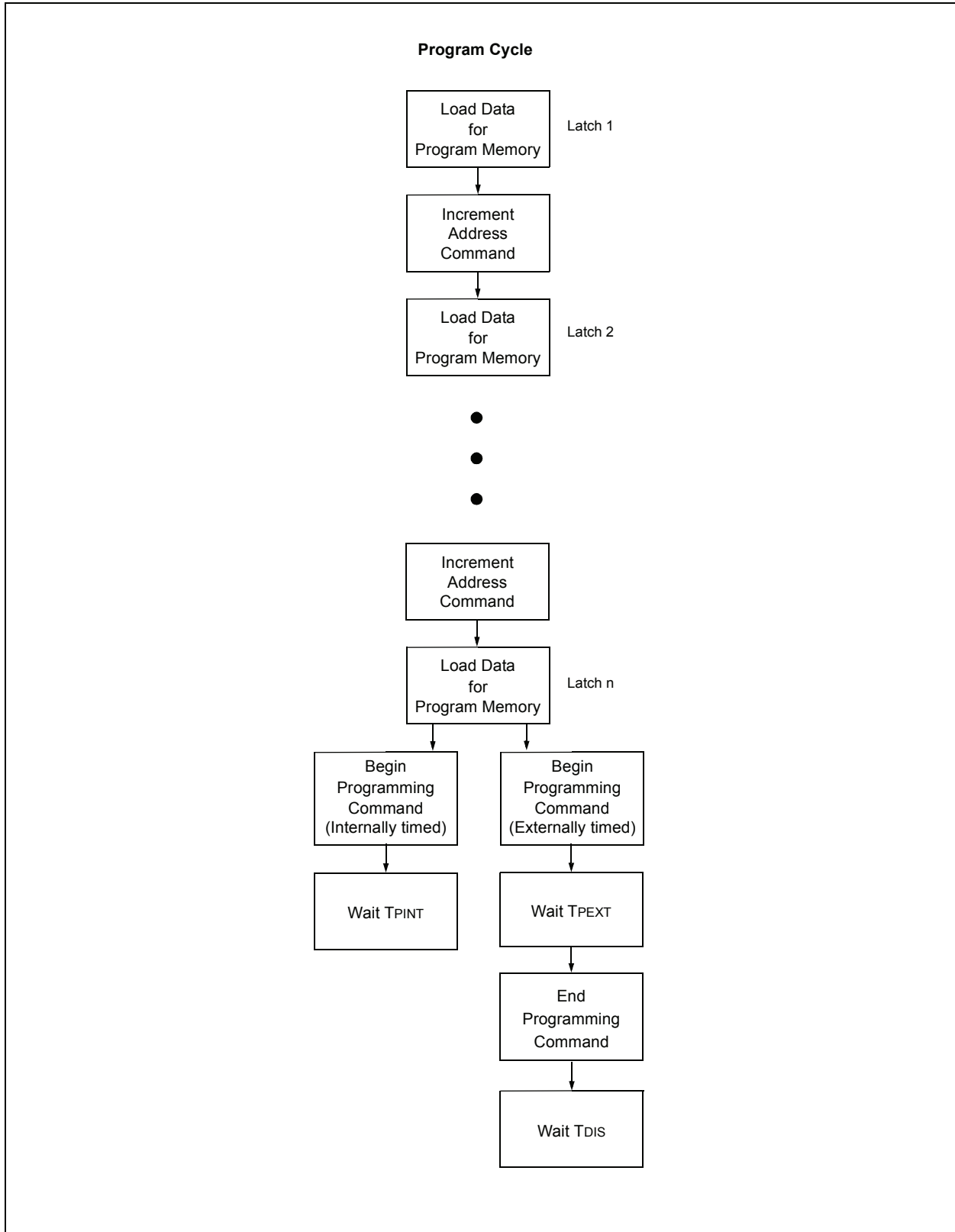


FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE



7.3 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the \overline{CP} Configuration bit.

TABLE 7-1: CONFIGURATION WORD MASK VALUES

Device	Config. Word 1 Mask	Config. Word 2 Mask
PIC16F1512	3EFFh	3E13h
PIC16F1513	3EFFh	3E13h
PIC16F1516	3EFFh	3E13h
PIC16F1517	3EFFh	3E13h
PIC16F1518	3EFFh	3E13h
PIC16F1519	3EFFh	3E13h
PIC16LF1512	3EFFh	3E03h
PIC16LF1513	3EFFh	3E03h
PIC16LF1516	3EFFh	3E03h
PIC16LF1517	3EFFh	3E03h
PIC16LF1518	3EFFh	3E03h
PIC16LF1519	3EFFh	3E03h
PIC16F1526	3EFFh	3E13h
PIC16F1527	3EFFh	3E13h
PIC16LF1526	3EFFh	3E03h
PIC16LF1527	3EFFh	3E03h

7.3.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the PIC16(L)F151X/152X program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location. Any Carry bit exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

PIC16(L)F151X/152X

EXAMPLE 7-4: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC16LF1527, 00AAh AT FIRST AND LAST ADDRESS

PIC16LF1527	Configuration Word 1 ⁽²⁾	3F7Fh
	Configuration Word 1 mask ⁽³⁾	3EFFh
	Configuration Word 2 ⁽²⁾	3FFFh
	Configuration Word 2 mask ^{(3), (5)}	3E03h
	User ID (8000h) ⁽¹⁾	000Eh
	User ID (8001h) ⁽¹⁾	0008h
	User ID (8002h) ⁽¹⁾	0005h
	User ID (8003h) ⁽¹⁾	0008h
	Sum of User IDs ⁽⁴⁾	$= (000Eh \text{ and } 000Fh) \ll 12 + (0008h \text{ and } 000Fh) \ll 8 +$ $(0005h \text{ and } 000Fh) \ll 4 + (0008h \text{ and } 000Fh)$ $= E000h + 0800h + 0050h + 0008h$ $= E858h$
	Checksum	$= (3F7Fh \text{ and } 3EFFh) + (3FFFh \text{ and } 3E03h) + \text{Sum of User IDs}$ $= 3E7Fh + 3E03h + E858h$ $= 64DAh$

- Note 1:** User ID values in this example are random values.
- 2:** Configuration Word 1 and 2 = all bits are '1' except the code-protect enable bit.
- 3:** Configuration Word 1 and 2 Mask = all Configuration Word bits are set to '1', except for unimplemented bits which read '0'.
- 4:** \ll = shift left, thus the LSb of the first user ID value is the MSb of the sum of user IDs and so on, until the LSb of the last user ID value becomes the LSb of the sum of user IDs.
- 5:** On the PIC16LF1527 device, the $\overline{\text{VCPEN}}$ bit is not implemented in Configuration Word 2; thus, all unimplemented bits are '0'.

PIC16(L)F151X/152X

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
TPINT	Internally timed programming operation time	—	—	2.5 5	ms ms	Program memory Configuration Words
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms	Note 1
TDIS	Time delay from program to compare (HV discharge time)	300	—	—	μs	
TEXT	Time delay when exiting Program/Verify mode	1	—	—	μs	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – VDD FIRST

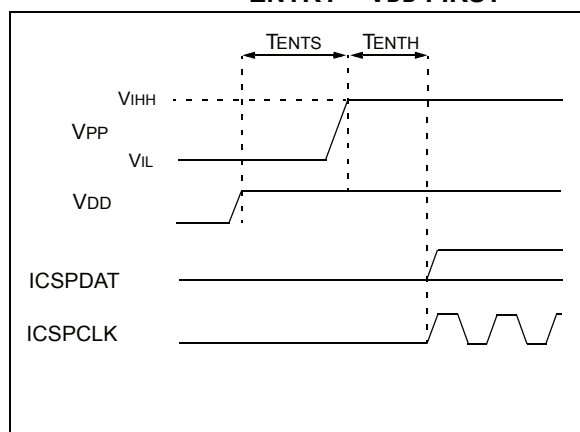


FIGURE 8-2: PROGRAMMING MODE ENTRY – VPP FIRST

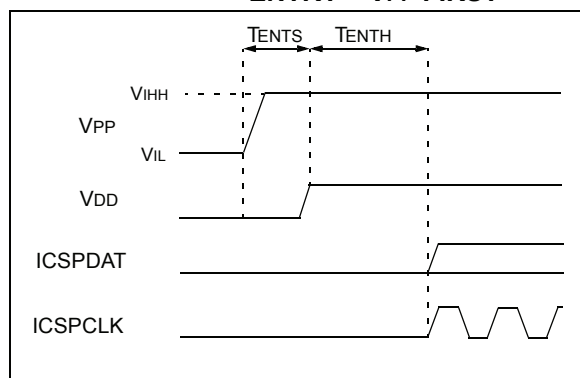


FIGURE 8-3: PROGRAMMING MODE EXIT – VPP LAST

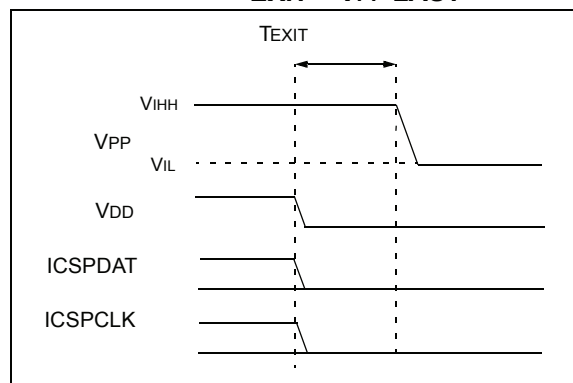


FIGURE 8-4: PROGRAMMING MODE EXIT – VDD LAST

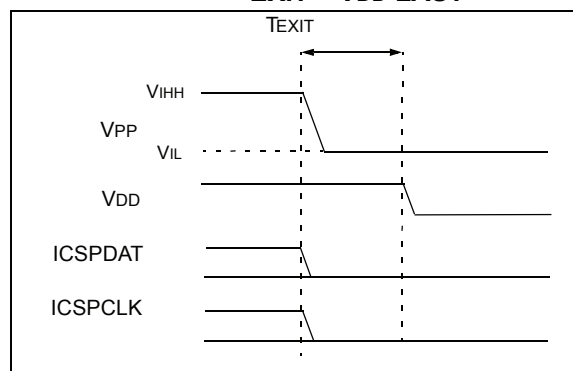


FIGURE 8-5: CLOCK AND DATA TIMING

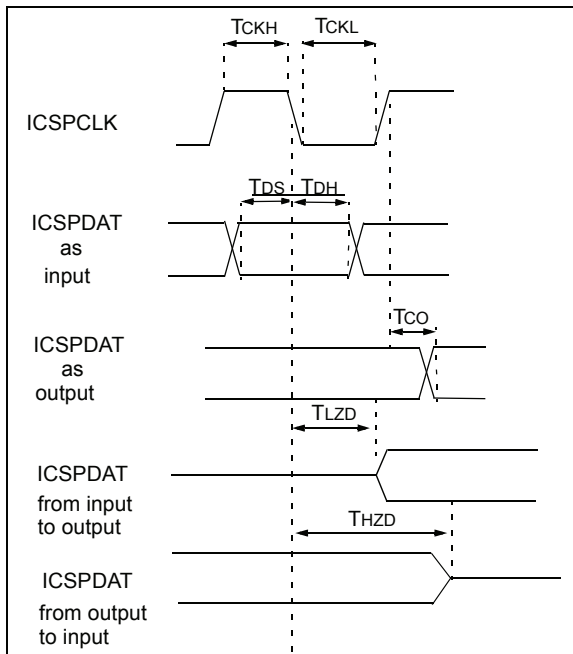


FIGURE 8-6: WRITE COMMAND-PAYLOAD TIMING

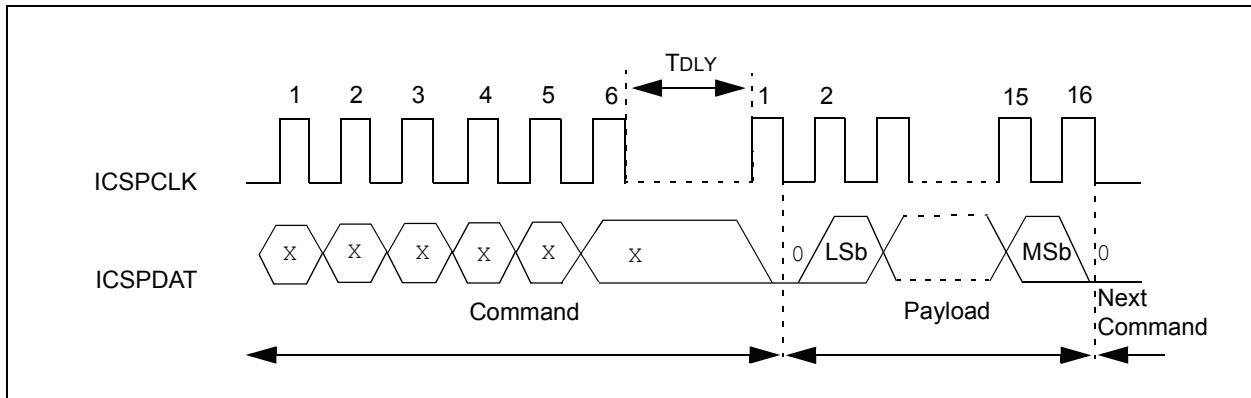
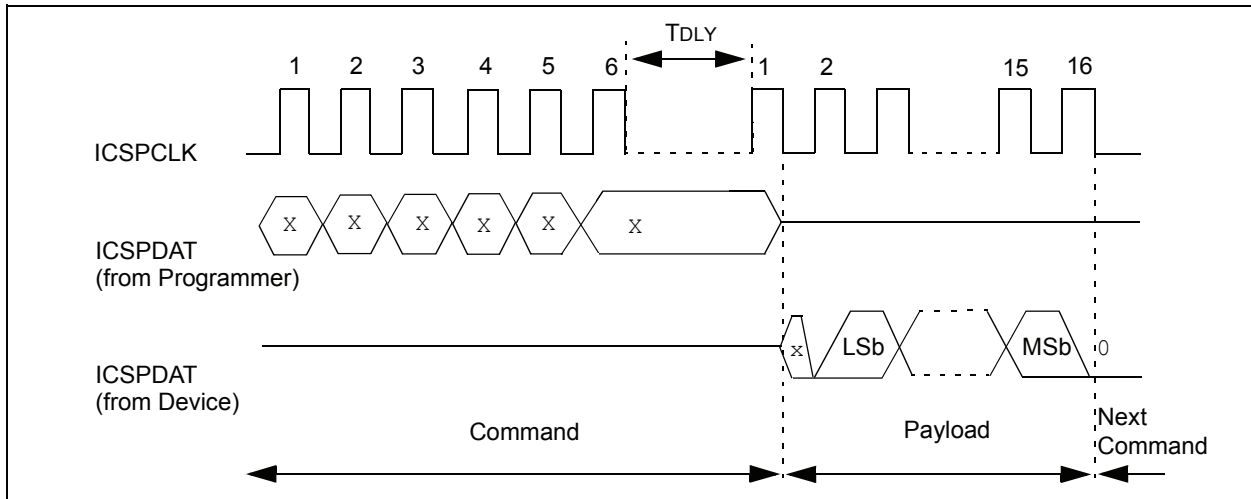


FIGURE 8-7: READ COMMAND-PAYLOAD TIMING



APPENDIX A: REVISION HISTORY

Revision A (08/2010)

Original release of this document.

Revision B (09/2011)

Added PIC16(L)F1512/1513 devices; Added new Figures 3-1 and 3-2; Updated Registers 3-1, 3-2 and 3-3 to new format; Updated Register 3-3 to add 2 kW and 4 kW Flash memory; Added Notes to Examples 7-1 to 7-4; Updated Table 8-1; Other minor corrections.

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ISBN: 978-1-61341-635-8

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08/02/11