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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

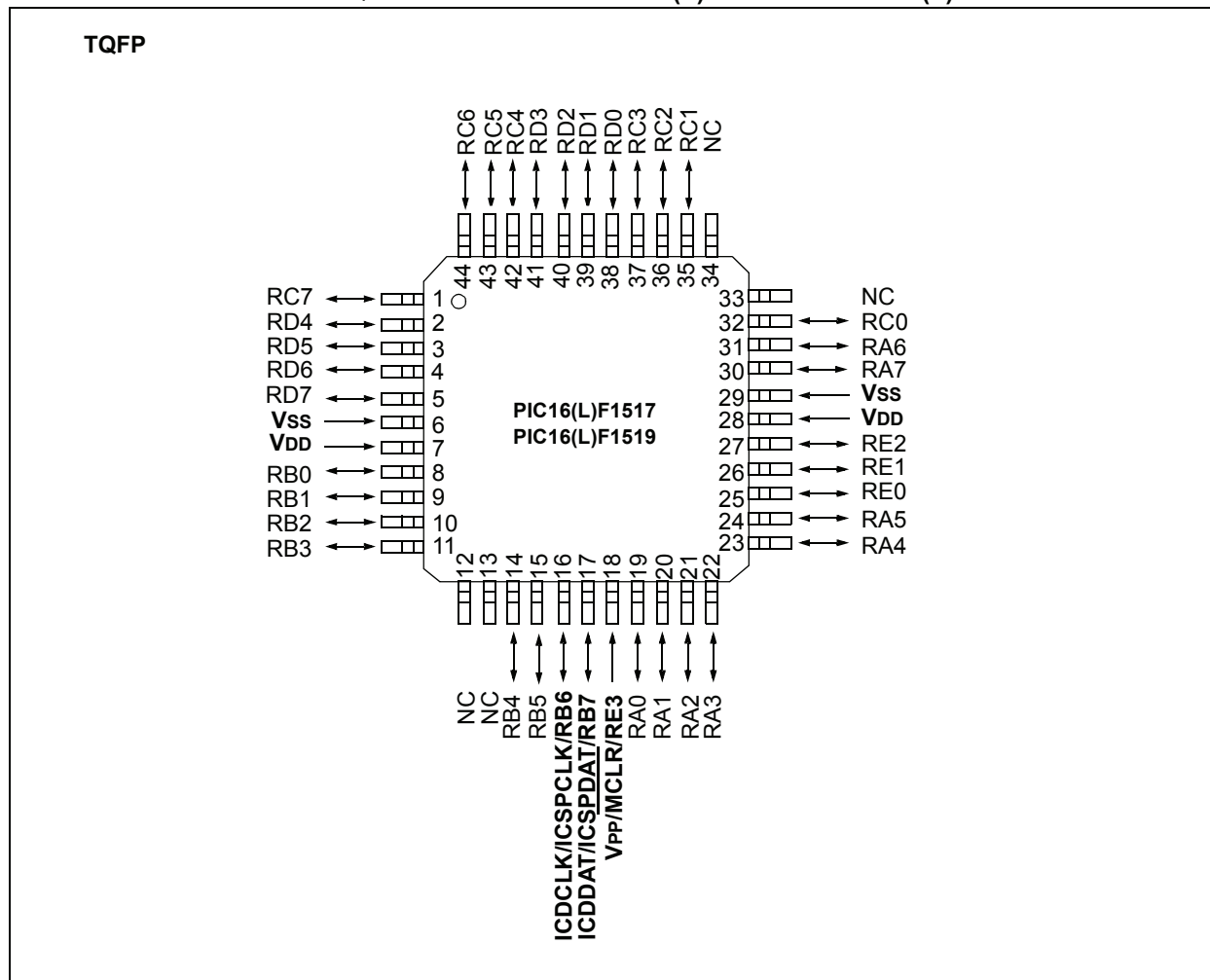
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16f1517-e-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic16f1517-e-pt</a>

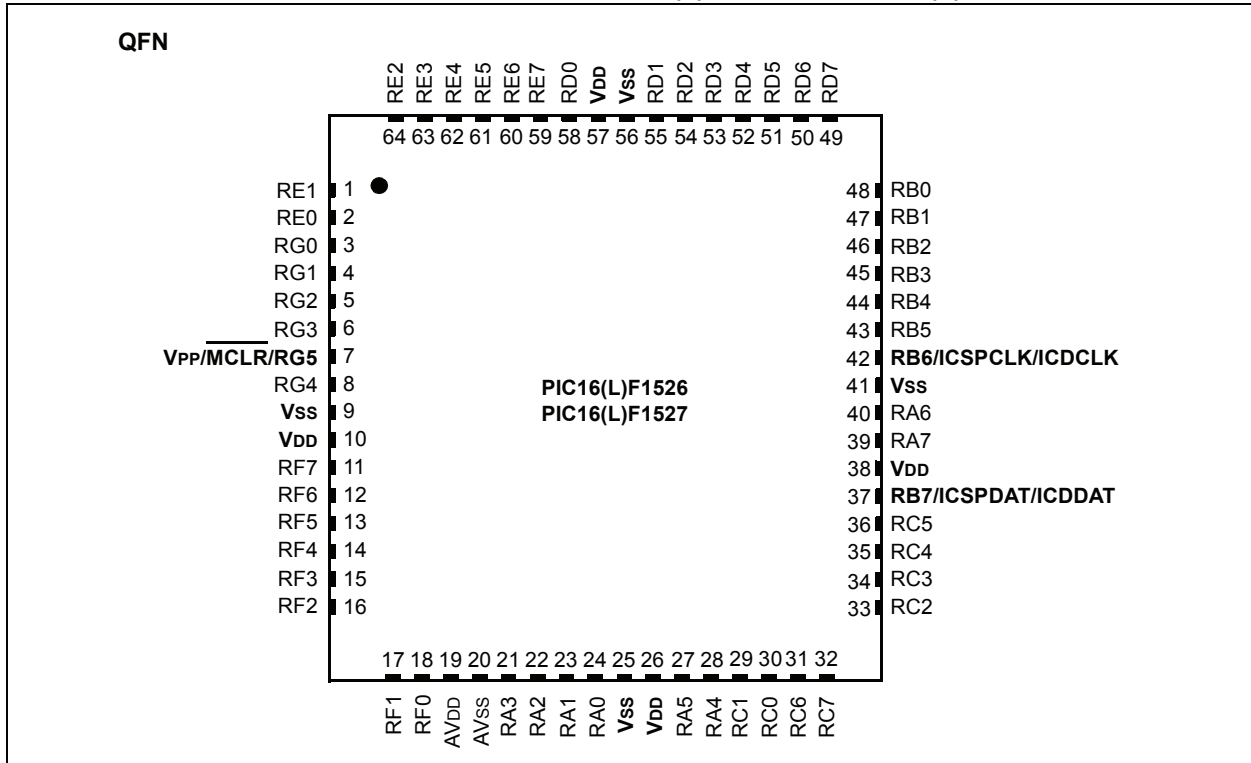
# PIC16(L)F151X/152X

FIGURE 2-5: 44-PIN TQFP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519

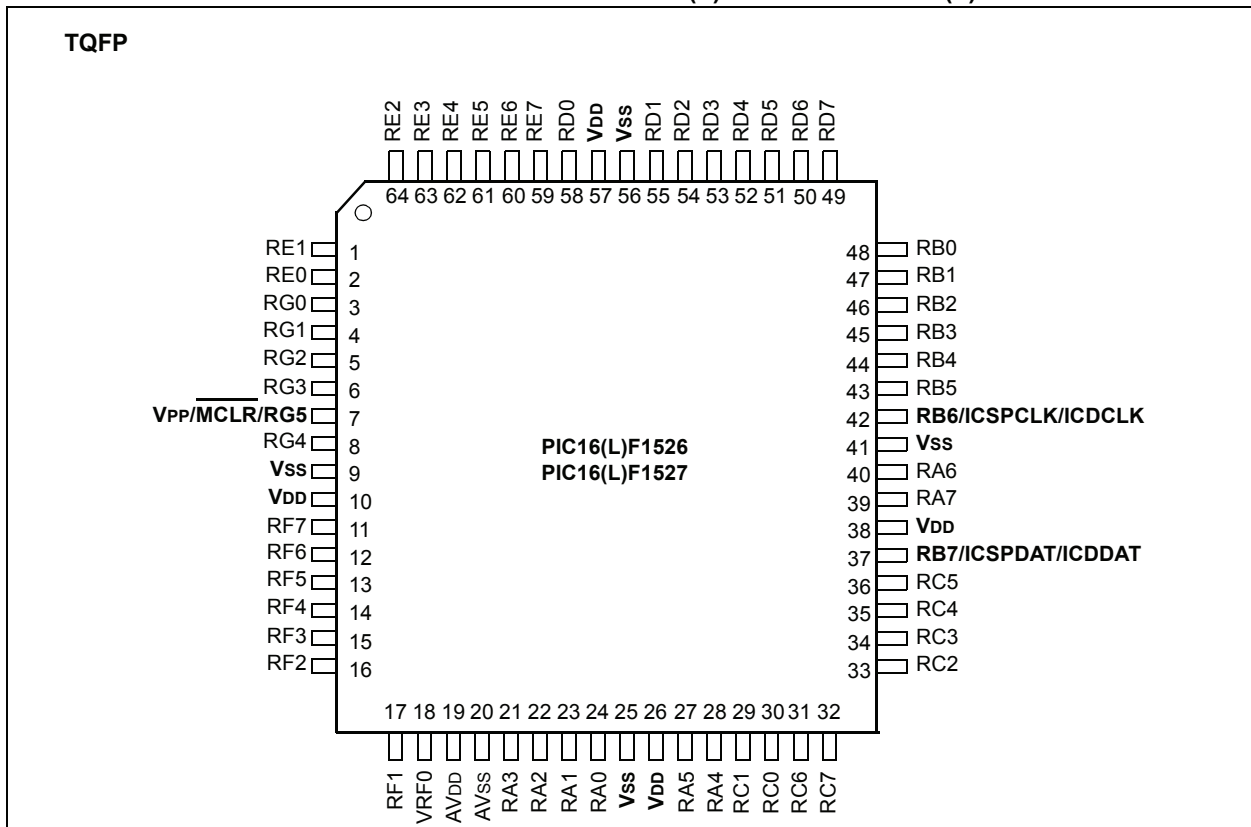


# PIC16(L)F151X/152X

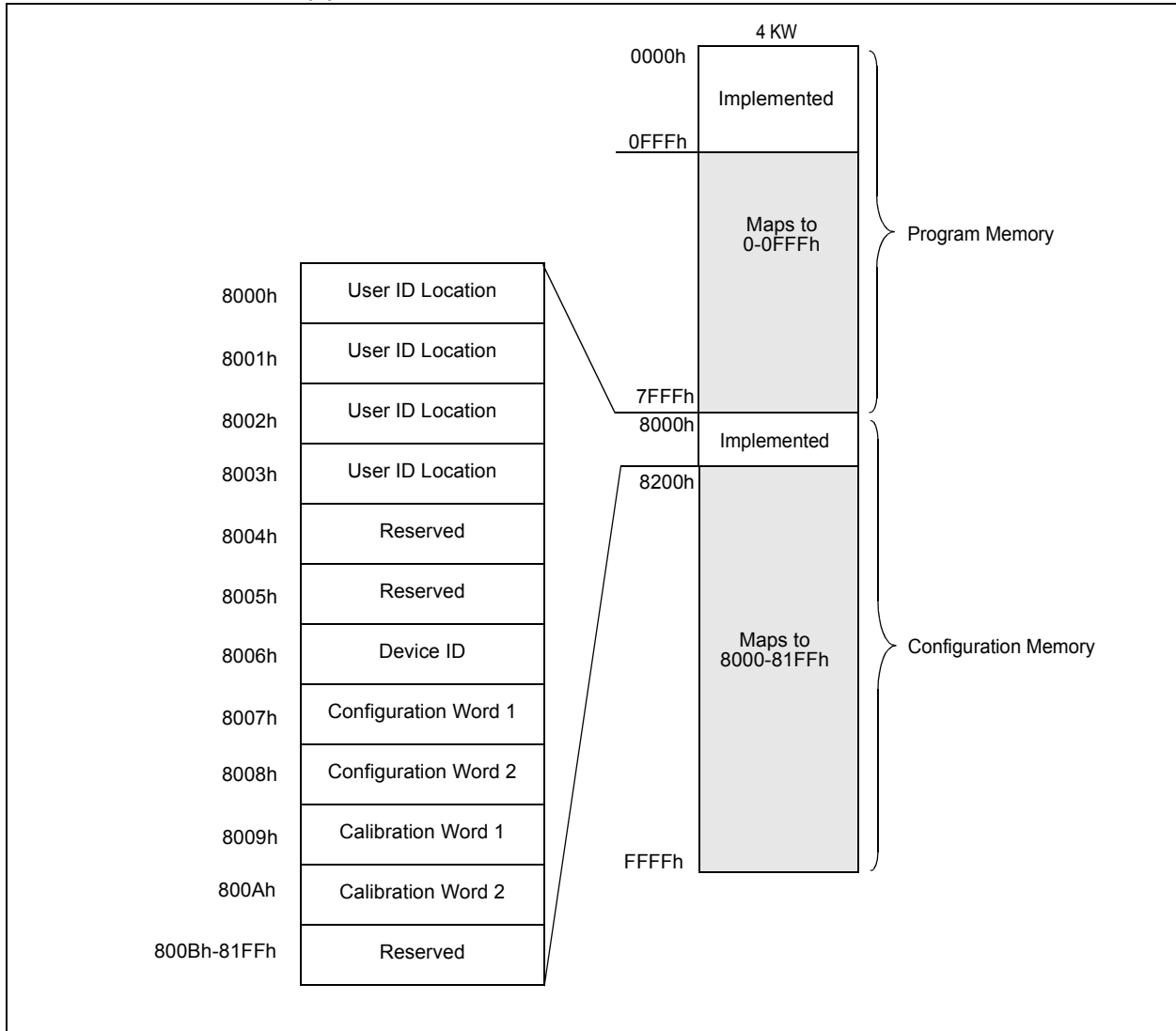
**FIGURE 2-6: 64-PIN QFN DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527**



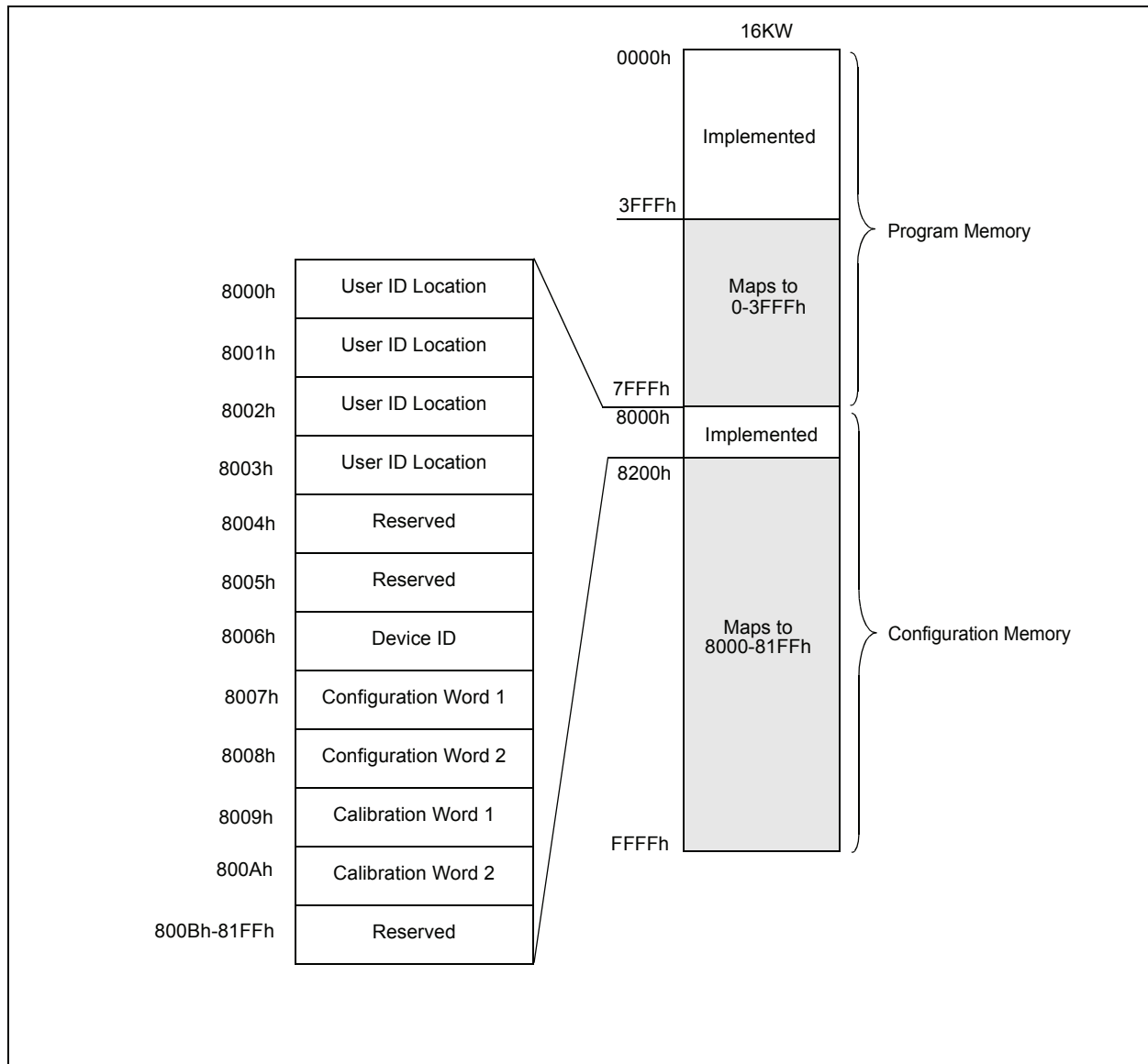
**FIGURE 2-7: 64-PIN TQFP DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527**



**FIGURE 3-2: PIC16(L)F1513 PROGRAM MEMORY MAPPING**



**FIGURE 3-4: PIC16(L)F1527, PIC16(L)F1518 AND PIC16(L)F1519 PROGRAM MEMORY MAPPING**



# PIC16(L)F151X/152X

## 3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

**Note:** MPLAB® IDE only displays the 7 Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the 7 LSbs be used if MPLAB IDE is the primary tool used to read these addresses.

## 3.2 Device ID

The device ID word is located at 8006h. This location is read-only and cannot be erased or modified.

**REGISTER 3-1: DEVICE ID: DEVICE ID REGISTER<sup>(1)</sup>**

R	R	R	R	R	R
DEV<8:3>					
bit 13			bit 8		

R	R	R	R	R	R	R	R
DEV<2:0>				REV<4:0>			
bit 7				bit 0			

<b>Legend:</b>	P = Programmable bit	U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit	'0' = Bit is cleared
-n = Value at POR	'1' = Bit is set	x = Bit is unknown

bit 13-5      **DEV<8:0>**: Device ID bits  
These bits are used to identify the part number.

bit 4-0      **REV<4:0>**: Revision ID bits  
These bits are used to identify the revision.

**Note 1:** This location cannot be written.

# PIC16(L)F151X/152X

## REGISTER 3-2: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
FCMEN	IESO	CLKOUTEN	BOREN<1:0>	—	
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP	MCLRE	PWRTÉ	WDTE<1:0>	FOSC<2:0>			
bit 7							bit 0

### Legend:

R = Readable bit                      P = Programmable bit                      U = Unimplemented bit, read as '1'  
 '0' = Bit is cleared                      '1' = Bit is set                      -n = Value when blank or after Bulk Erase

- bit 13      **FCMEN:** Fail-Safe Clock Monitor Enable bit  
             1 = Fail-Safe Clock Monitor is enabled  
             0 = Fail-Safe Clock Monitor is disabled
- bit 12      **IESO:** Internal External Switchover bit  
             1 = Internal/External Switchover mode is enabled  
             0 = Internal/External Switchover mode is disabled
- bit 11      **CLKOUTEN:** Clock Out Enable bit  
             1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.  
             0 = CLKOUT function is enabled on CLKOUT pin
- bit 10-9    **BOREN<1:0>:** Brown-out Reset Enable bits<sup>(1)</sup>  
             11 = BOR enabled  
             10 = BOR enabled during operation and disabled in Sleep  
             01 = BOR controlled by SBOREN bit of the PCON register  
             00 = BOR disabled
- bit 8      **Unimplemented:** Read as '1'
- bit 7      **CP:** Code Protection bit<sup>(2)</sup>  
             1 = Program memory code protection is disabled  
             0 = Program memory code protection is enabled
- bit 6      **MCLRE:** MCLR/VPP Pin Function Select bit  
             If LVP bit = 1:  
                 This bit is ignored.  
             If LVP bit = 0:  
                 1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.  
                 0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUA register.
- bit 5      **PWRTÉ:** Power-up Timer Enable bit<sup>(1)</sup>  
             1 = PWRT disabled  
             0 = PWRT enabled
- bit 4-3    **WDTE<1:0>:** Watchdog Timer Enable bit  
             11 = WDT enabled  
             10 = WDT enabled while running and disabled in Sleep  
             01 = WDT controlled by the SWDTEN bit in the WDTCON register  
             00 = WDT disabled
- bit 2-0    **FOSC<2:0>:** Oscillator Selection bits  
             111 = ECH: External Clock, High-Power mode: on CLKIN pin  
             110 = ECM: External Clock, Medium-Power mode: on CLKIN pin  
             101 = ECL: External Clock, Low-Power mode: on CLKIN pin  
             100 = INTOSC oscillator: I/O function on OSC1 pin  
             011 = EXTRC oscillator: RC function on OSC1 pin  
             010 = HS oscillator: High-speed crystal/resonator on OSC2 pin and OSC1 pin  
             001 = XT oscillator: Crystal/resonator on OSC2 pin and OSC1 pin  
             000 = LP oscillator: Low-power crystal on OSC2 pin and OSC1 pin

- Note** 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.  
 2: The entire program memory will be erased when the code protection is turned off.

## REGISTER 3-3: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
LVP	DEBUG	LPBOR	BORV	STVREN	—
bit 13					bit 8

U-1	U-1	U-1	R/P-1	U-1	U-1	R/P-1	R/P-1
—	—	—	VCAPEN <sup>(2)</sup>	—	—	WRT<1:0>	
bit 7							bit 0

### Legend:

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '1'

'0' = Bit is cleared

'1' = Bit is set

-n = Value when blank or after Bulk Erase

- bit 13 **LVP:** Low-Voltage Programming Enable bit<sup>(1)</sup>  
 1 = Low-voltage programming enabled  
 0 = HV on MCLR/VPP must be used for programming
- bit 12 **DEBUG:** In-Circuit Debugger Mode bit  
 1 = In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins  
 0 = In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger
- bit 11 **LPBOR:** Low-Power BOR  
 1 = Low-Power BOR is disabled  
 0 = Low-Power BOR is enabled
- bit 10 **BORV:** Brown-out Reset Voltage Selection bit  
 1 = Brown-out Reset voltage (VBOR), low trip point selected  
 0 = Brown-out Reset voltage (VBOR), high trip point selected
- bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit  
 1 = Stack Overflow or Underflow will cause a Reset  
 0 = Stack Overflow or Underflow will not cause a Reset
- bit 8-5 **Unimplemented:** Read as '1'
- bit 4 **VCAPEN:** Voltage Regulator Capacitor Enable bits<sup>(1)</sup>  
 0 = VCAP functionality is enabled on VCAP pin  
 1 = All VCAP pin functions are disabled
- bit 3-2 **Unimplemented:** Read as '1'
- bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits  
**2 kW Flash memory (PIC16(L)F1512):**  
 11 = Write protection off  
 10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control  
 01 = 000h to FFFh write-protected, 400h to 7FFh may be modified by PMCON control  
 00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control  
**4 kW Flash memory (PIC16(L)F1513):**  
 11 = Write protection off  
 10 = 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control  
 01 = 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control  
 00 = 000h to FFFh write-protected, no addresses may be modified by PMCON control  
**8 kW Flash memory (PIC16F/LF1516/1517/1526):**  
 11 = Write protection off  
 10 = 000h to 1FFh write-protected, 200h to 1FFFh may be modified by PMCON control  
 01 = 000h to FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control  
 00 = 000h to 1FFFh write-protected, no addresses may be modified by PMCON control  
**16 kW Flash memory (PIC16F/LF1518/1519/1527):**  
 11 = Write protection off  
 10 = 000h to 1FFh write-protected, 200h to 3FFFh may be modified by PMCON control  
 01 = 000h to 1FFFh write-protected, 2000h to 3FFFh may be modified by PMCON control  
 00 = 000h to 3FFFh write-protected, no addresses may be modified by PMCON control

**Note 1:** The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.

**Note 2:** Applies to PIC16F151X/152X devices only. On PIC16LF151X/152X, the VCAPEN bit is unimplemented.

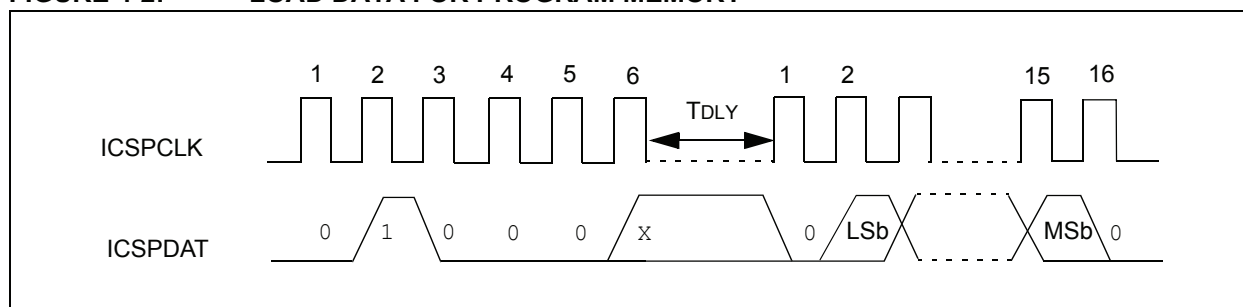


# PIC16(L)F151X/152X

## 4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

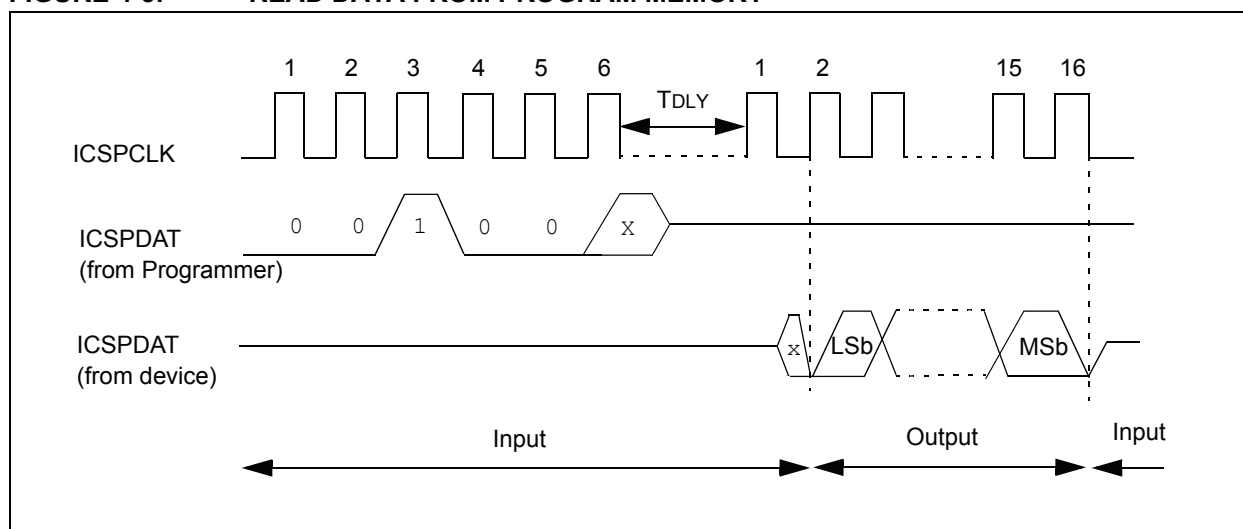
**FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY**



## 4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ( $\overline{CP}$ ), the data will be read as zeros (see Figure 4-3).

**FIGURE 4-3: READ DATA FROM PROGRAM MEMORY**



# PIC16(L)F151X/152X

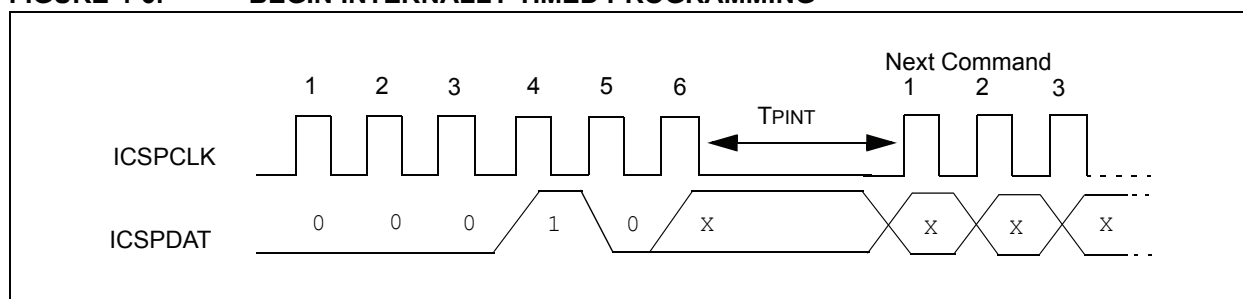
## 4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time,  $T_{PINT}$ , for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed.

**FIGURE 4-6: BEGIN INTERNALLY TIMED PROGRAMMING**

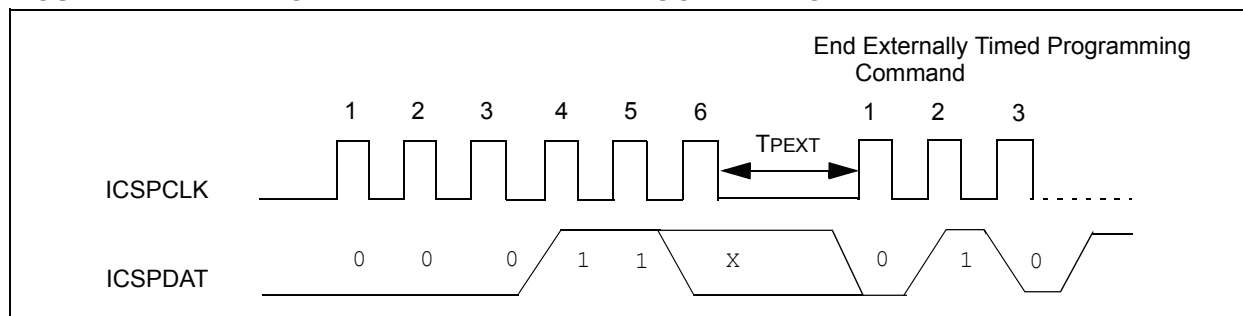


## 4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming the End Externally Timed Programming command must be sent in the specified time window defined by  $T_{PEXT}$  (see [Figure 4-7](#)).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

**FIGURE 4-7: BEGIN EXTERNALLY TIMED PROGRAMMING**

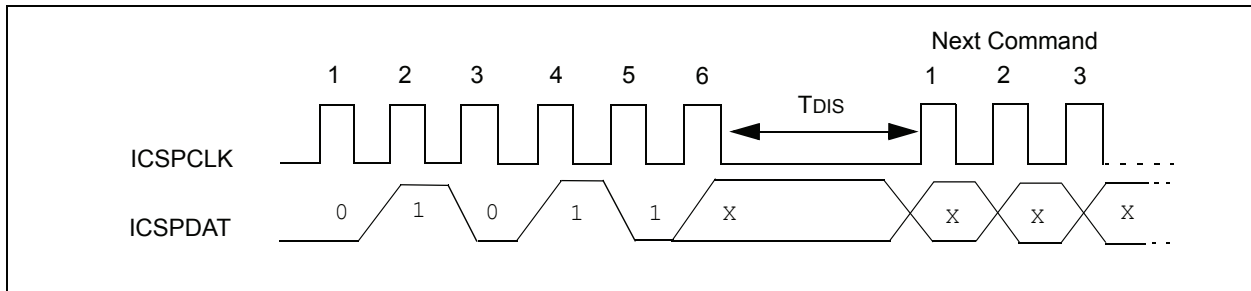


## 4.3.8 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPEXT after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 4-8).

**FIGURE 4-8: END EXTERNALLY TIMED PROGRAMMING**



## 4.3.9 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-7FFFh:

- Program Memory is erased
- Configuration Words are erased

Address 8000h-8008h:

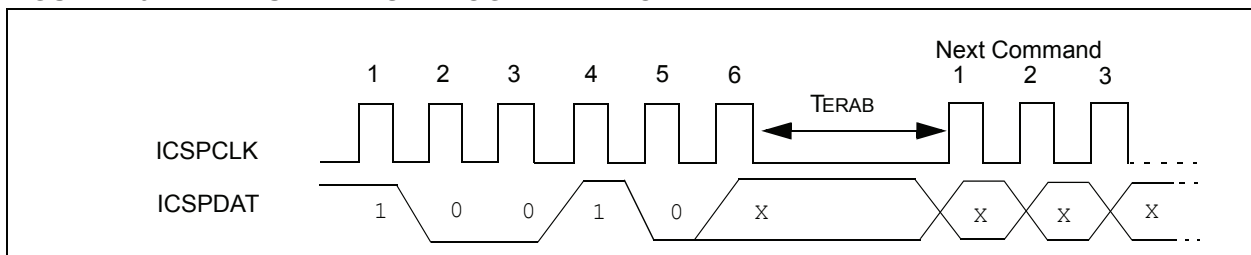
- Program Memory is erased
- Configuration Words are erased
- User ID Locations are erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

After receiving the Bulk Erase Program Memory command the erase will not complete until the time interval, TERAB, has expired.

**Note:** The code protection Configuration bit (CP) has no effect on the Bulk Erase Program Memory command.

**FIGURE 4-9: BULK ERASE PROGRAM MEMORY**



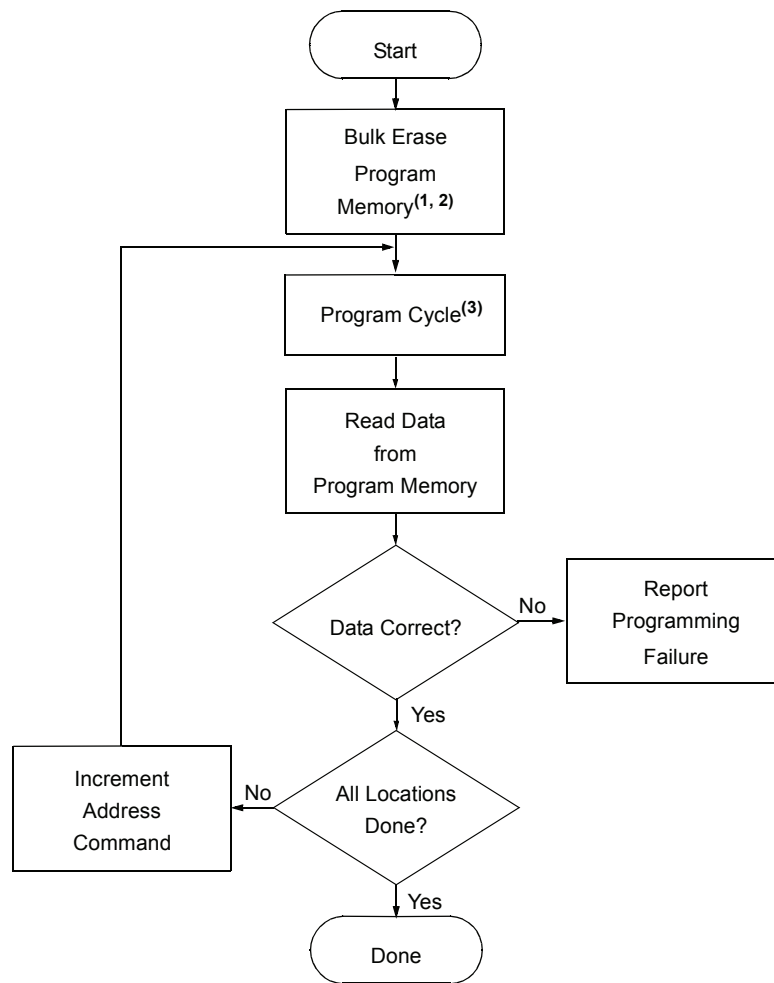
## 5.0 PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to [Table 4-2](#) for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC's address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes cannot cross the physical boundary. For example, with the PIC16F1527, attempting to write from address 0002h-0009h will result in data being written to 0008h-000Fh.

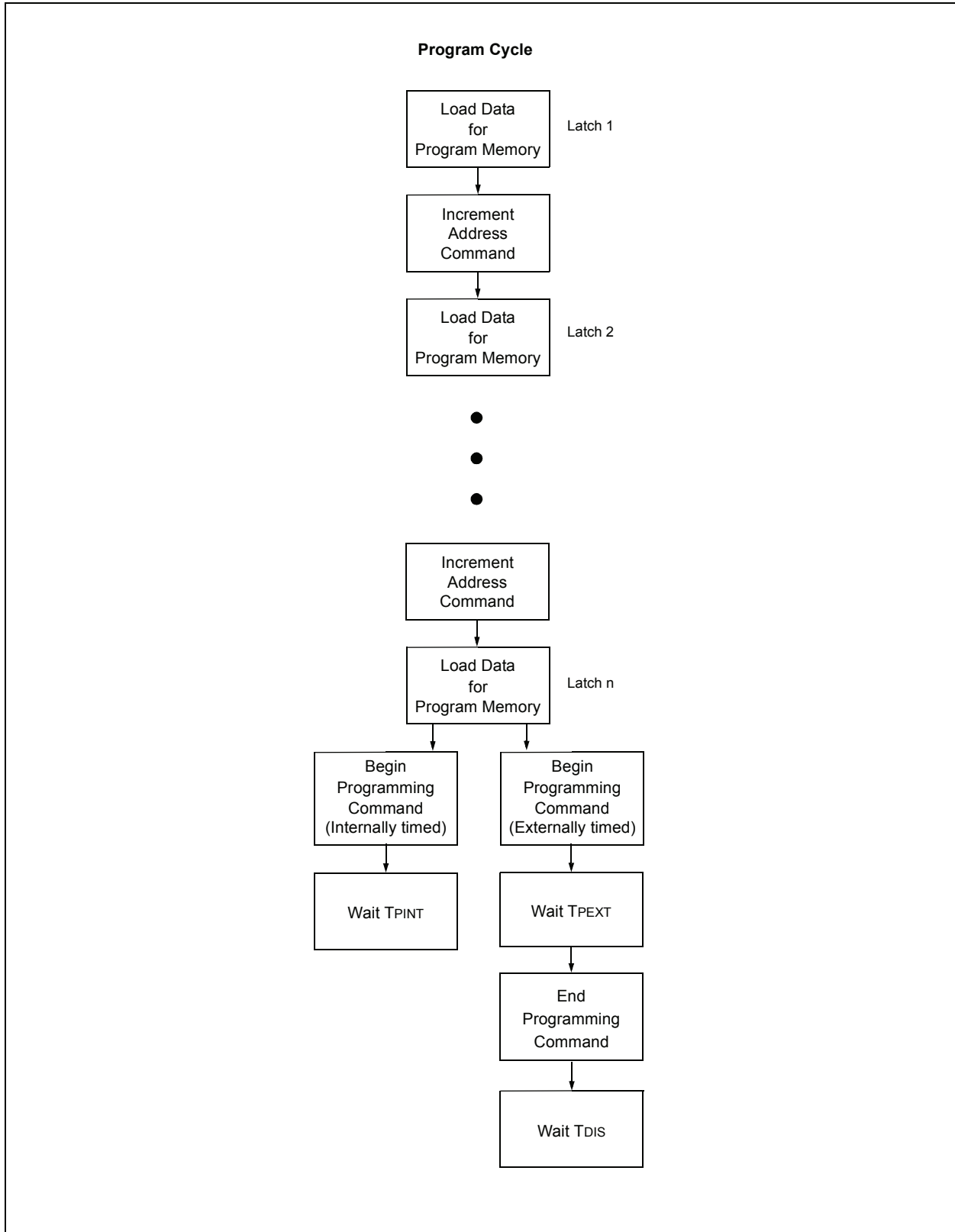
If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

**FIGURE 5-2: PROGRAM MEMORY FLOWCHART**



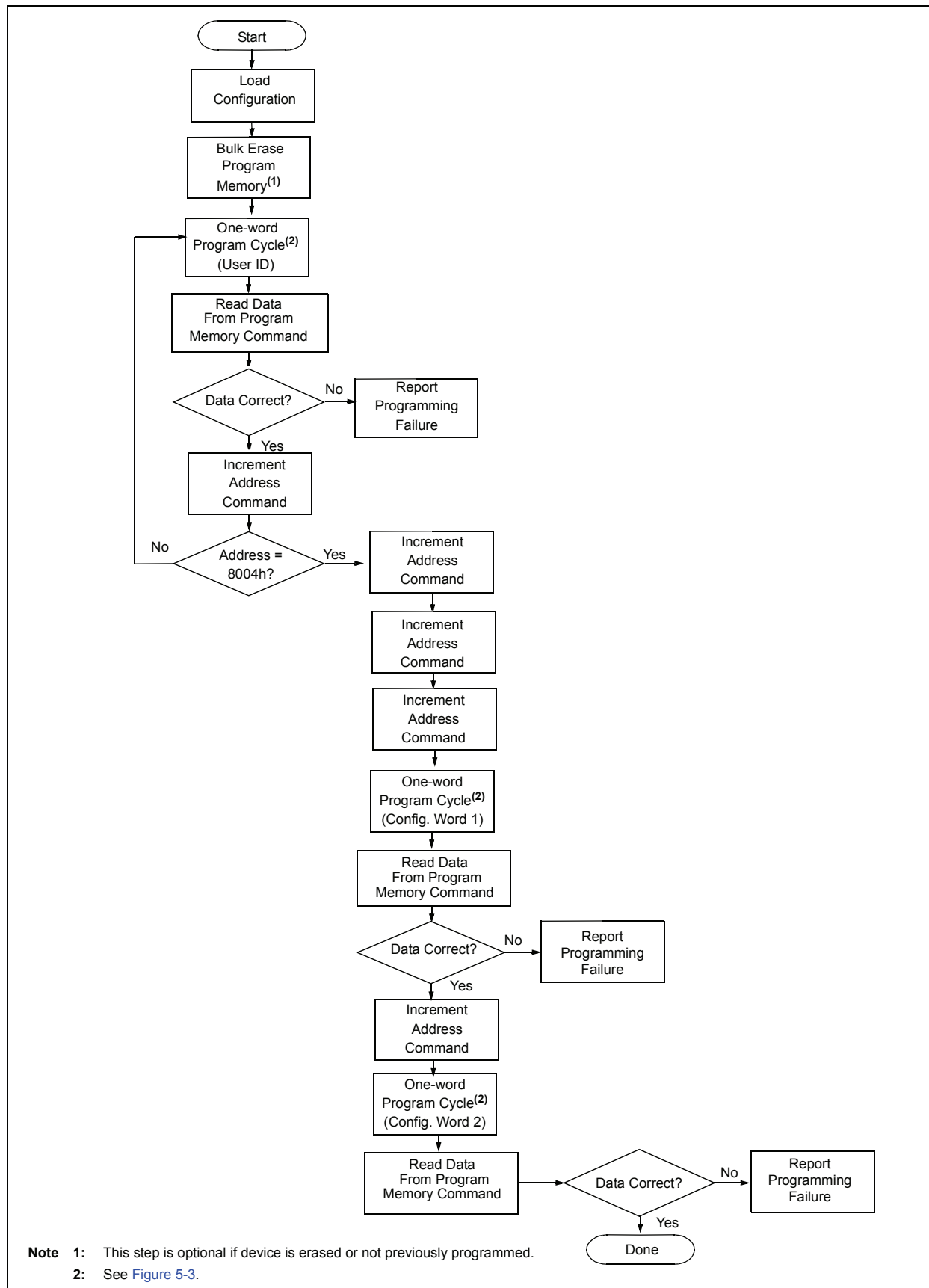
- Note 1:** This step is optional if device has already been erased or has not been previously programmed.  
**Note 2:** If the device is code-protected or must be completely erased, then Bulk Erase device per [Figure 5-6](#).  
**Note 3:** See [Figure 5-3](#) or [Figure 5-4](#).

**FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE**



# PIC16(L)F151X/152X

**FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART**



# PIC16(L)F151X/152X

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## 6.0 CODE PROTECTION

Code protection is controlled using the  $\overline{\text{CP}}$  bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFFh) read as all '0'. Further programming is disabled for the program memory (0000h-7FFFh).

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

### 6.1 Program Memory

Code protection is enabled by programming the  $\overline{\text{CP}}$  bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

## 7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: Configuration Word 1 is stored at 8007h on the PIC16(L)F151X/152X. In the hex file this will be referenced as 1000Eh-1000Fh).

### 7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

### 7.2 Device ID and Revision

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID (excluding the revision) against the value read from the part. On a mismatch condition the programmer should generate a warning message.



# PIC16(L)F151X/152X

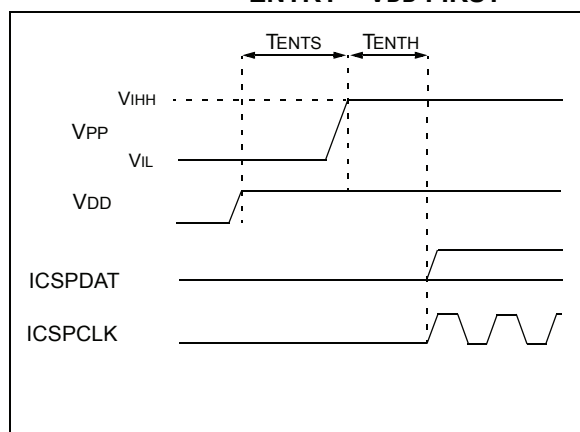
**TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY**

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
TPINT	Internally timed programming operation time	—	—	2.5 5	ms ms	Program memory Configuration Words
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms	<b>Note 1</b>
TDIS	Time delay from program to compare (HV discharge time)	300	—	—	μs	
TEXT	Time delay when exiting Program/Verify mode	1	—	—	μs	

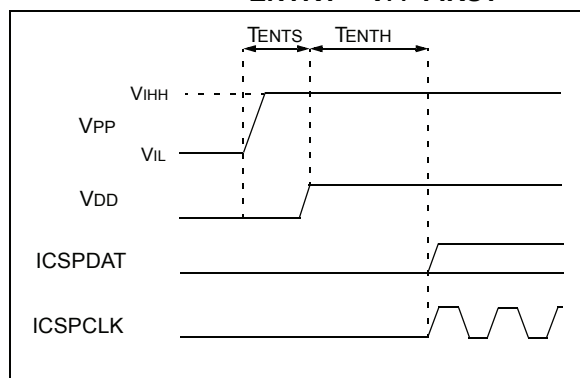
**Note 1:** Externally timed writes are not supported for Configuration and Calibration bits.

## 8.1 AC Timing Diagrams

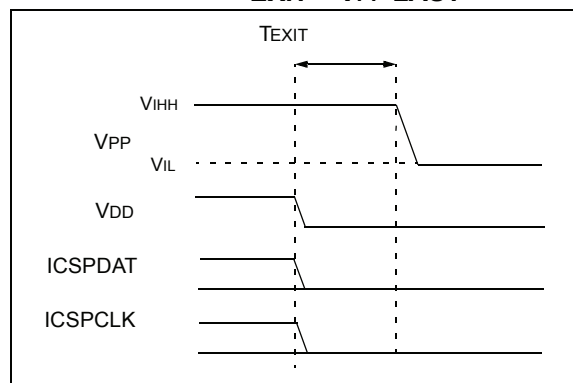
**FIGURE 8-1: PROGRAMMING MODE ENTRY – VDD FIRST**



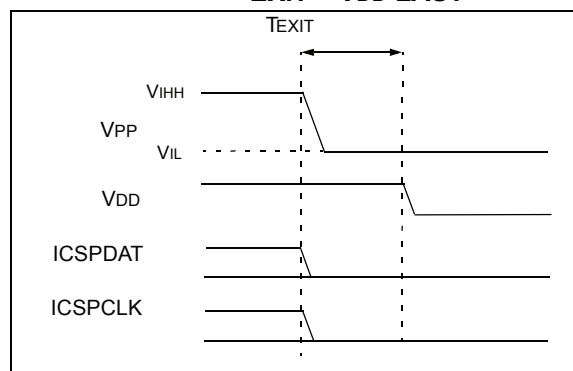
**FIGURE 8-2: PROGRAMMING MODE ENTRY – VPP FIRST**



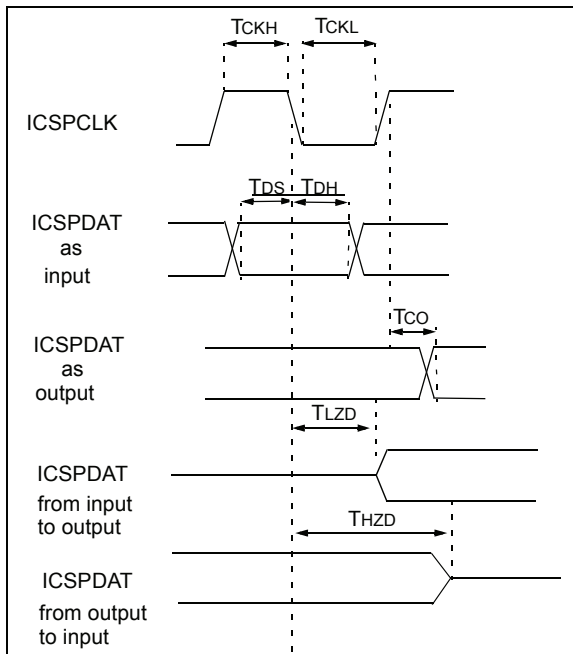
**FIGURE 8-3: PROGRAMMING MODE EXIT – VPP LAST**



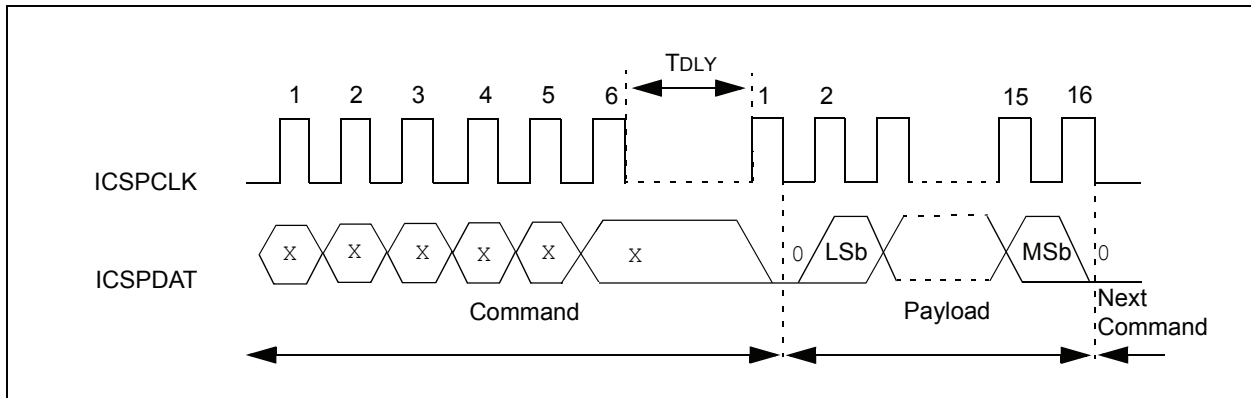
**FIGURE 8-4: PROGRAMMING MODE EXIT – VDD LAST**



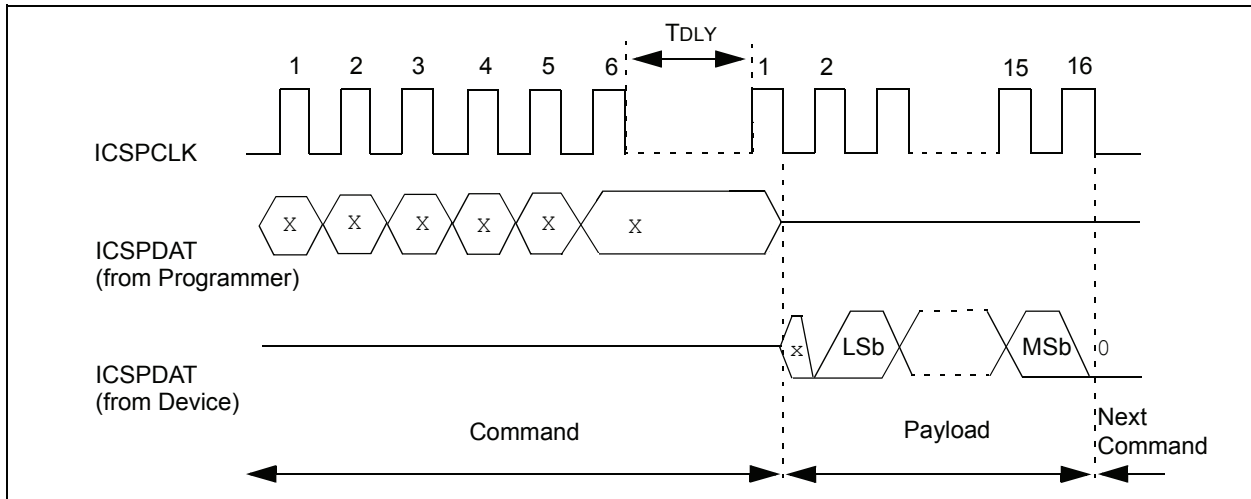
**FIGURE 8-5: CLOCK AND DATA TIMING**



**FIGURE 8-6: WRITE COMMAND-PAYLOAD TIMING**



**FIGURE 8-7: READ COMMAND-PAYLOAD TIMING**



# PIC16(L)F151X/152X

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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ISBN: 978-1-61341-635-8

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08/02/11