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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1517t-i-mv

PIC16(L)F151X/152X

1.2 Pin Utilization

Five pins are needed for ICSP™ programming. The pins are listed in Table 1-1 and Table 1-2.

TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING – PIC16(L)F1526 AND PIC16(L)F1527

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RG5/$\overline{\text{MCLR}}$/VPP	Program/Verify mode	P[1]	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{\text{MCLR}}$ input. Since the $\overline{\text{MCLR}}$ is used for a level source, $\overline{\text{MCLR}}$ does not draw any significant current.

TABLE 1-2: PIN DESCRIPTIONS DURING PROGRAMMING – PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516, PIC16(L)F1517, PIC16(L)F1518 and PIC16(L)F1519

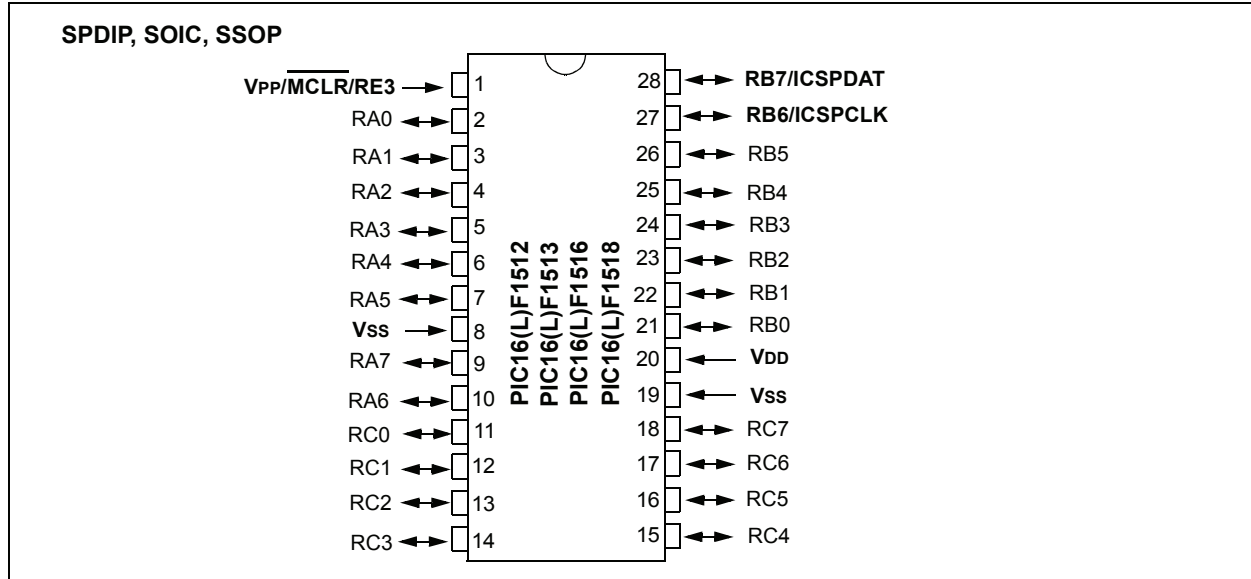| Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RE3/$\overline{\text{MCLR}}$/VPP	Program/Verify mode	P[1]	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{\text{MCLR}}$ input. Since the $\overline{\text{MCLR}}$ is used for a level source, $\overline{\text{MCLR}}$ does not draw any significant current.

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2.0   DEVICE PINOUTS

The pin diagrams for the PIC16(L)F151X/152X family are shown in Figure 2-1 through Figure 2-7. The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagrams.

FIGURE 2-1:   28-PIN SPDIP, SOIC, SSOP DIAGRAM FOR PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516 AND PIC16(L)F1518

SPDIP, SOIC, SSOP

Pin	Left Signal		Pin	Right Signal
1	V$_{PP}$/$\overline{MCLR}$/RE3		28	RB7/ICSPDAT
2	RA0		27	RB6/ICSPCLK
3	RA1		26	RB5
4	RA2		25	RB4
5	RA3		24	RB3
6	RA4		23	RB2
7	RA5		22	RB1
8	Vss		21	RB0
9	RA7		20	V$_{DD}$
10	RA6		19	Vss
11	RC0		18	RC7
12	RC1		17	RC6
13	RC2		16	RC5
14	RC3		15	RC4

(Device markings: PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516, PIC16(L)F1518)

FIGURE 2-2: **28-PIN UQFN DIAGRAM FOR PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516 AND PIC16(L)F1518**

UQFN

PIC16(L)F1512
PIC16(L)F1513
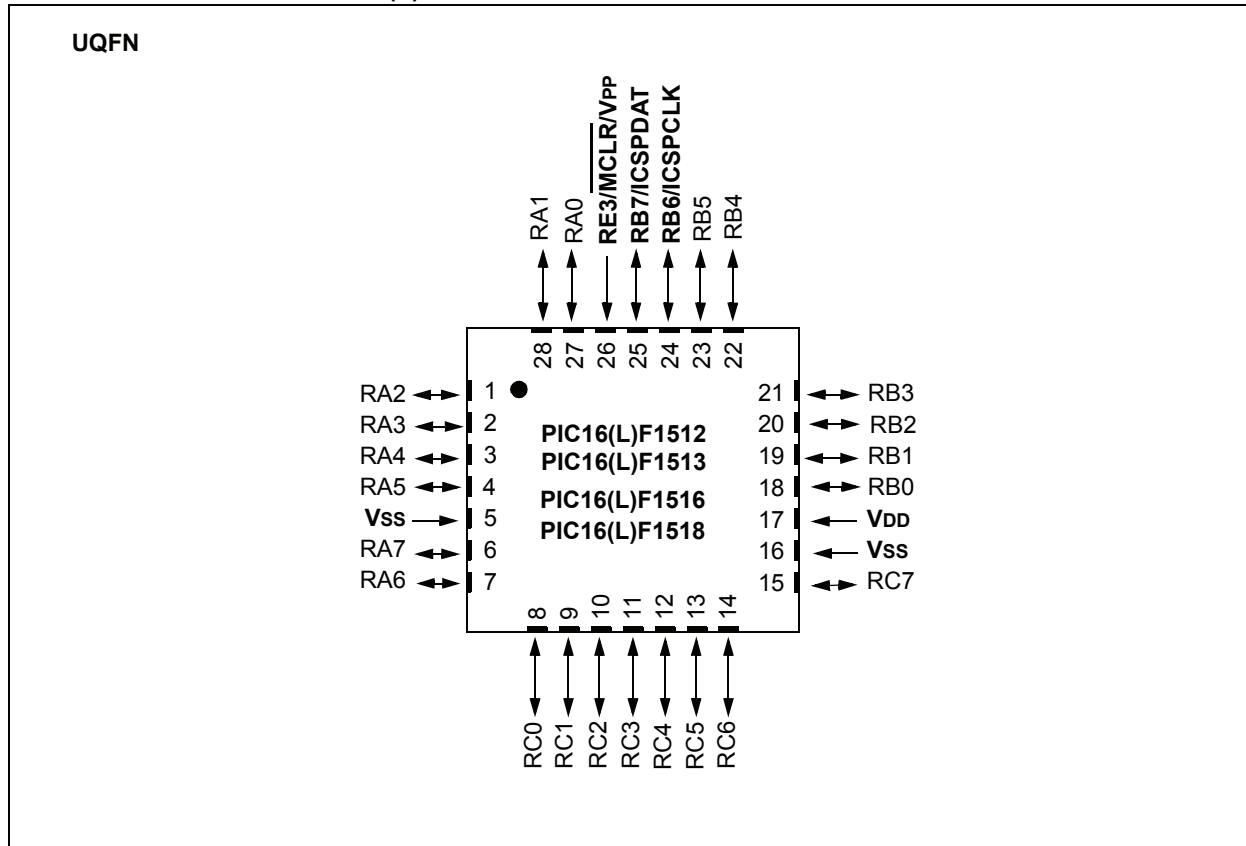
PIC16(L)F1516
PIC16(L)F1518

REGISTER 3-2: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
FCMEN	IESO	CLKOUTEN	BOREN<1:0>		—
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP	MCLRE	PWRTE	WDTE<1:0>		FOSC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13   **FCMEN:** Fail-Safe Clock Monitor Enable bit
            1 = Fail-Safe Clock Monitor is enabled
            0 = Fail-Safe Clock Monitor is disabled

bit 12   **IESO:** Internal External Switchover bit
            1 = Internal/External Switchover mode is enabled
            0 = Internal/External Switchover mode is disabled

bit 11   **CLKOUTEN:** Clock Out Enable bit
            1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
            0 = CLKOUT function is enabled on CLKOUT pin

bit 10-9   **BOREN<1:0>:** Brown-out Reset Enable bits[1]
            11 = BOR enabled
            10 = BOR enabled during operation and disabled in Sleep
            01 = BOR controlled by SBOREN bit of the PCON register
            00 = BOR disabled

bit 8   **Unimplemented:** Read as '1'

bit 7   **CP:** Code Protection bit[2]
            1 = Program memory code protection is disabled
            0 = Program memory code protection is enabled

bit 6   **MCLRE:** MCLR/VPP Pin Function Select bit
            If LVP bit = 1:
                This bit is ignored.
            If LVP bit = 0:
                1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
                0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUA register.

bit 5   **PWRTE:** Power-up Timer Enable bit[1]
            1 = PWRT disabled
            0 = PWRT enabled

bit 4-3   **WDTE<1:0>:** Watchdog Timer Enable bit
            11 = WDT enabled
            10 = WDT enabled while running and disabled in Sleep
            01 = WDT controlled by the SWDTEN bit in the WDTCON register
            00 = WDT disabled

bit 2-0   **FOSC<2:0>:** Oscillator Selection bits
            111 = ECH: External Clock, High-Power mode: on CLKIN pin
            110 = ECM: External Clock, Medium-Power mode: on CLKIN pin
            101 = ECL: External Clock, Low-Power mode: on CLKIN pin
            100 = INTOSC oscillator: I/O function on OSC1 pin
            011 = EXTRC oscillator: RC function on OSC1 pin
            010 = HS oscillator: High-speed crystal/resonator on OSC2 pin and OSC1 pin
            001 = XT oscillator: Crystal/resonator on OSC2 pin and OSC1 pin
            000 = LP oscillator: Low-power crystal on OSC2 pin and OSC1 pin

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
     2: The entire program memory will be erased when the code protection is turned off.

PIC16(L)F151X/152X

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- V$_{PP}$ – First entry mode
- V$_{DD}$ – First entry mode

4.1.1 V$_{PP}$ – FIRST ENTRY MODE

To enter Program/Verify mode via the V$_{PP}$-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{MCLR}$ from 0V to V$_{IHH}$.
3. Raise the voltage on V$_{DD}$ FROM 0V to the desired operating voltage.

The V$_{PP}$-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when Configuration Word 1 has $\overline{MCLR}$ disabled (MCLRE = 0), the power-up time is disabled ($\overline{PWRTE}$ = 0), the internal oscillator is selected (F$_{OSC}$ = 100), and ICSPCLK and ICSPDAT pins are driven by the user application, the device will execute code. Since this may prevent entry, V$_{PP}$-first entry mode is strongly recommended. See the timing diagram in Figure 8-2.

4.1.2 V$_{DD}$ – FIRST ENTRY MODE

To enter Program/Verify mode via the V$_{DD}$-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on V$_{DD}$ from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{MCLR}$ from V$_{DD}$ or below to V$_{IHH}$.

The V$_{DD}$-first method is useful when programming the device when V$_{DD}$ is already applied, for it is not necessary to disconnect V$_{DD}$ to enter Program/Verify mode. See the timing diagram in Figure 8-1.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{MCLR}$ to V$_{DD}$ or lower (V$_{IL}$). See Figures 8-3 and 8-4.

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the PIC16(L)F151X/152X devices to be programmed using V$_{DD}$ only, without high voltage. When the LVP bit of Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{MCLR}$ is brought to V$_{IL}$.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{MCLR}$ must be held at V$_{IL}$ for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 8-8 and Figure 8-9.

Exiting Program/Verify mode is done by no longer driving $\overline{MCLR}$ to V$_{IL}$. See Figure 8-8 and Figure 8-9.

> **Note:** To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

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4.3 Program/Verify Commands

The PIC16(L)F151X/152X implements 10 programming commands; each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of T$_{DLY}$ between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING

Command	Mapping							Data/Note
	Binary (MSb … LSb)						Hex	
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data For Program Memory	x	0	0	0	1	0	02h	0, data (14), 0
Read Data From Program Memory	x	0	0	1	0	0	04h	0, data (14), 0
Increment Address	x	0	0	1	1	0	06h	—
Reset Address	x	1	0	1	1	0	16h	—
Begin Internally Timed Programming	x	0	1	0	0	0	08h	—
Begin Externally Timed Programming	x	1	1	0	0	0	18h	—
End Externally Timed Programming	x	0	1	0	1	0	0Ah	—
Bulk Erase Program Memory	x	0	1	0	0	1	09h	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	11h	Internally Timed

4.3.1 LOAD CONFIGURATION

The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

Note: Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.
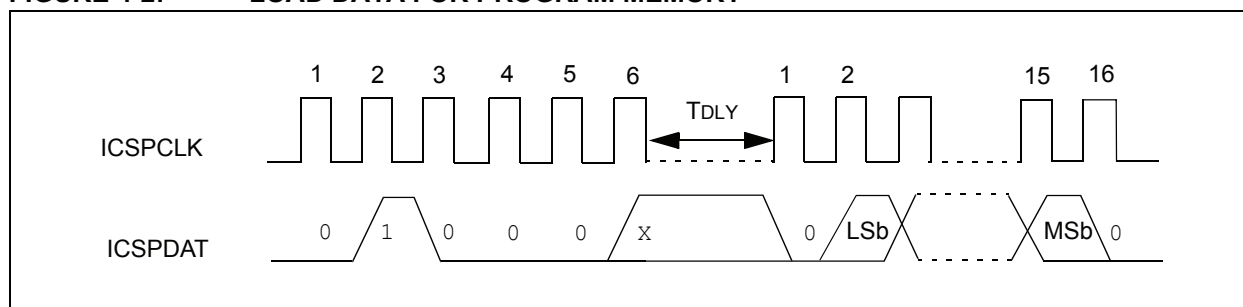
FIGURE 4-1: LOAD CONFIGURATION
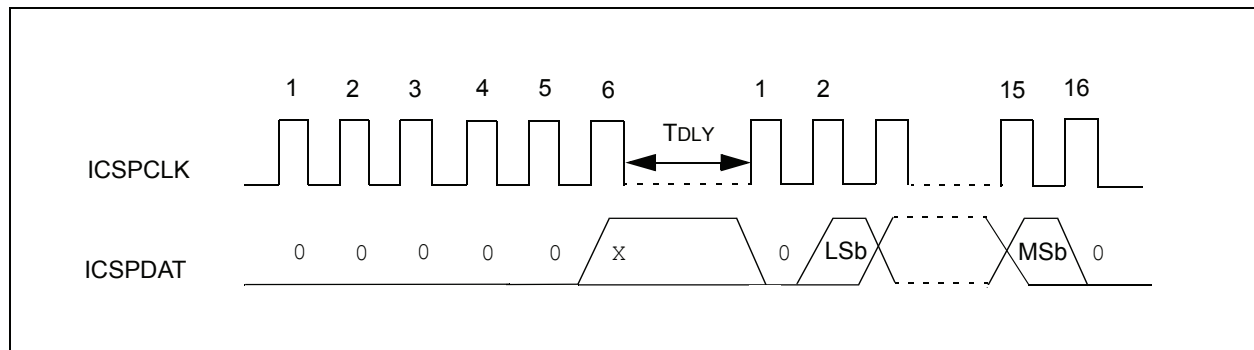
4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY

4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros (see Figure 4-3).

FIGURE 4-3: READ DATA FROM PROGRAM MEMORY

Advance Information
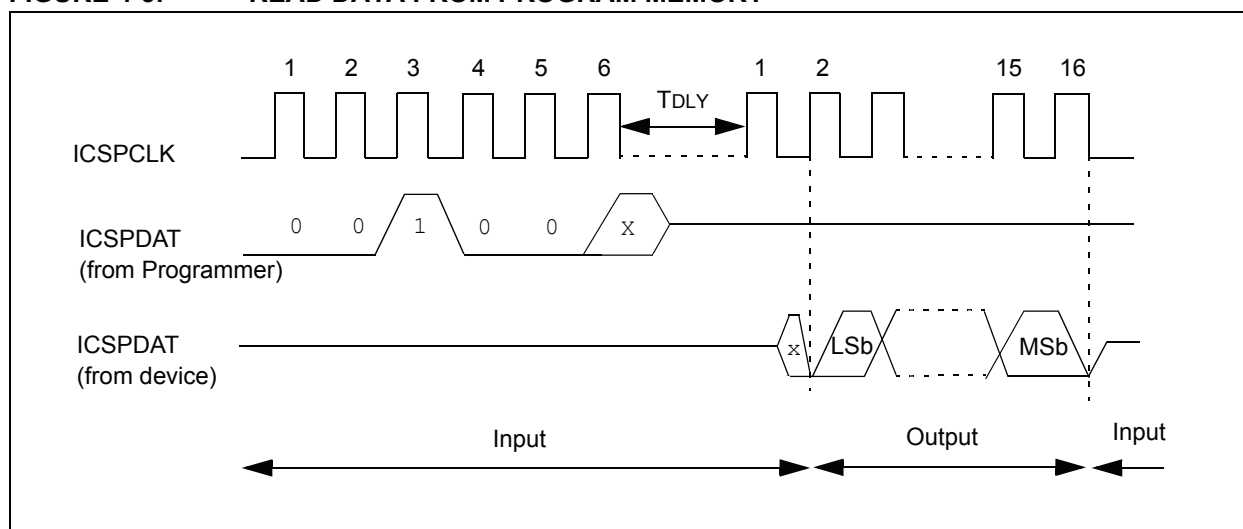
4.3.4 INCREMENT ADDRESS

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it. If the address is incremented from address 7FFFh, it will wrap-around to location 0000h. If the address is incremented from FFFFh, it will wrap-around to location 8000h.
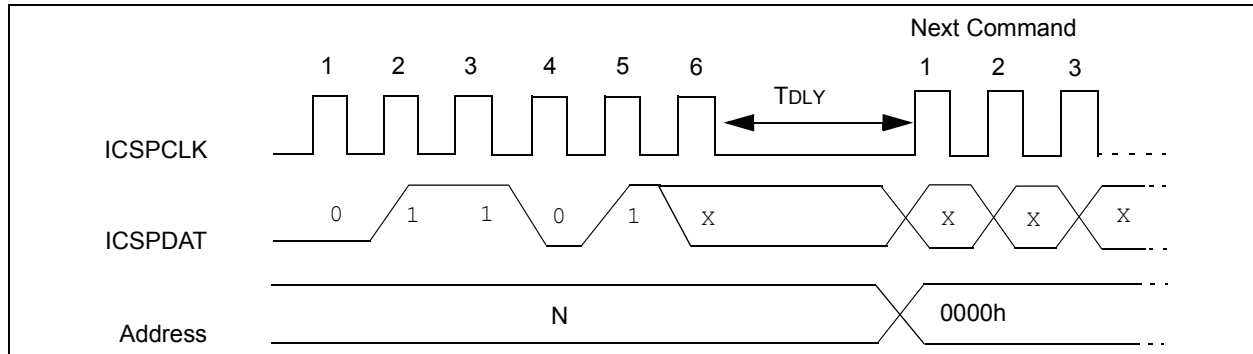
FIGURE 4-4: **INCREMENT ADDRESS**
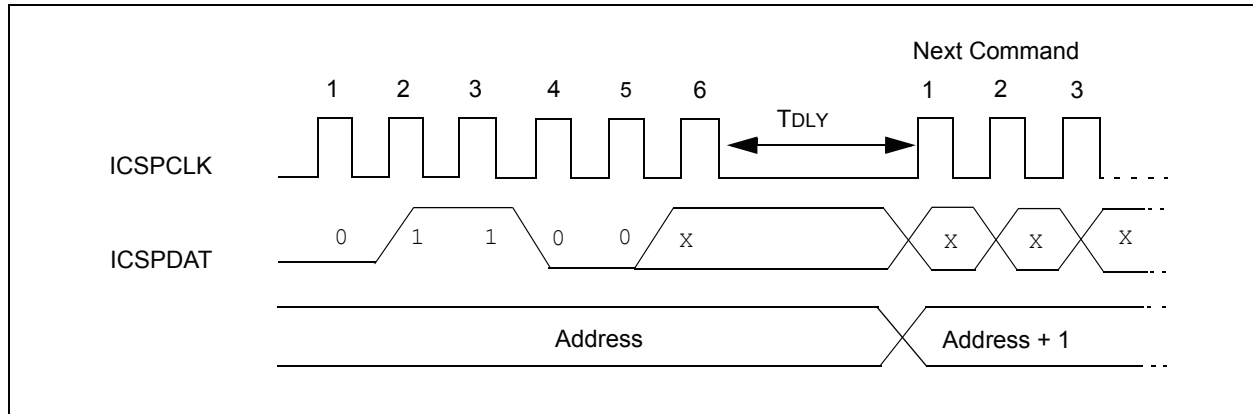
4.3.5 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory.

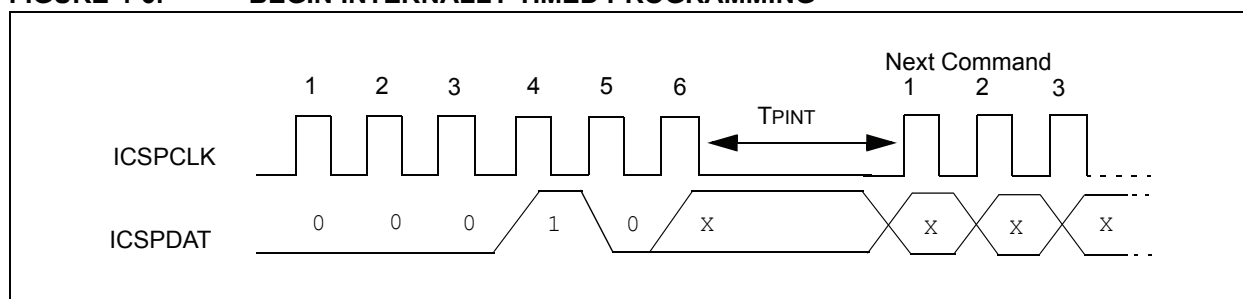**FIGURE 4-5:** **RESET ADDRESS**

PIC16(L)F151X/152X

4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, TPINT, for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed.

FIGURE 4-6: BEGIN INTERNALLY TIMED PROGRAMMING

4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming the End Externally Timed Programming command must be sent in the specified time window defined by TPEXT (see Figure 4-7).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 4-7: BEGIN EXTERNALLY TIMED PROGRAMMING

Advance Information
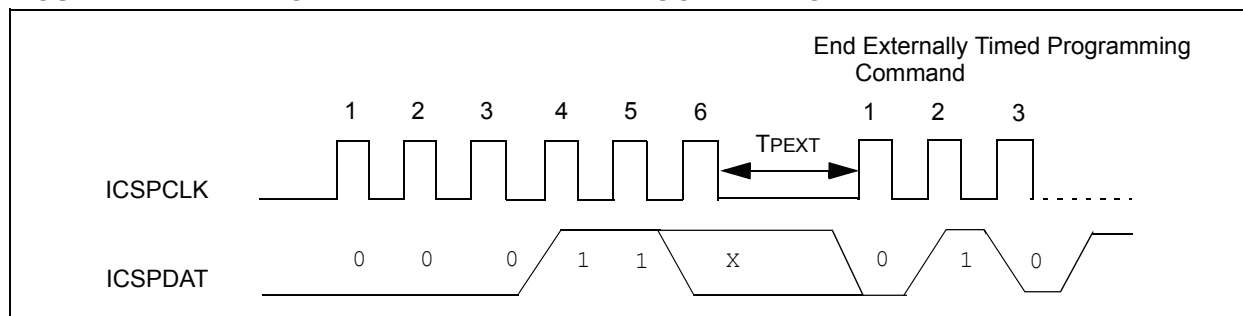
PIC16(L)F151X/152X

4.3.10   ROW ERASE PROGRAM MEMORY

The Row Erase Program Memory command will erase an individual row. Refer to Table 4-2 for row sizes of specific devices and the PC bits used to address them. If the program memory is code-protected the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h the Row Erase Program Memory command will only erase the user ID locations regardless of the setting of the $\overline{CP}$ Configuration bit.

After receiving the Row Erase Program Memory command the erase will not complete until the time interval, T_{ERAR}, has expired.

TABLE 4-2:   PROGRAMMING ROW SIZE AND LATCHES

Devices	PC	Row Size	Number of Latches
PIC16(L)F151X/152X	<15:5>	32	32

FIGURE 4-10:   ROW ERASE PROGRAM MEMORY

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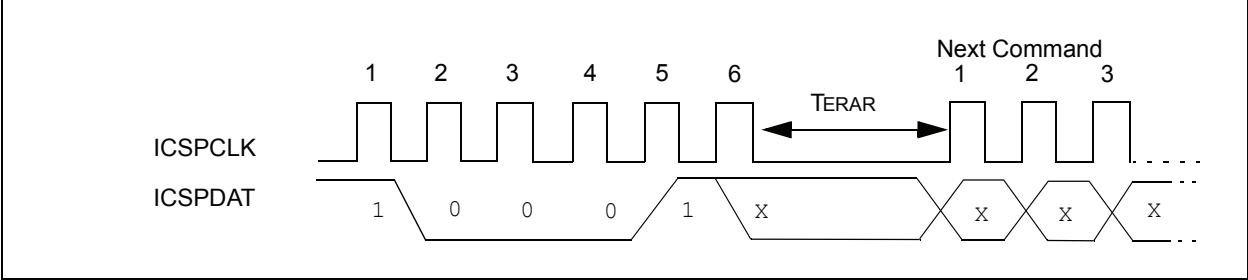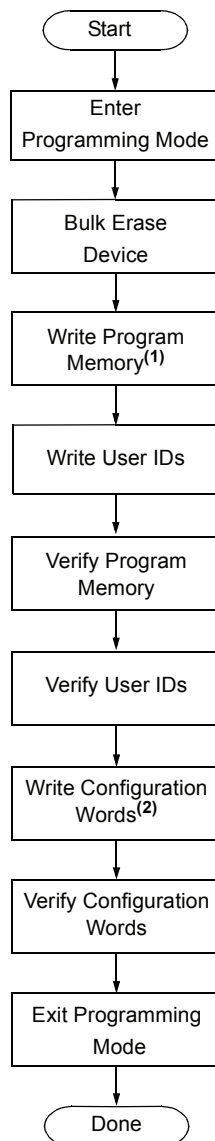
5.0 PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to Table 4-2 for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC's address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes cannot cross the physical boundary. For example, with the PIC16F1527, attempting to write from address 0002h-0009h will result in data being written to 0008h-000Fh.

If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.
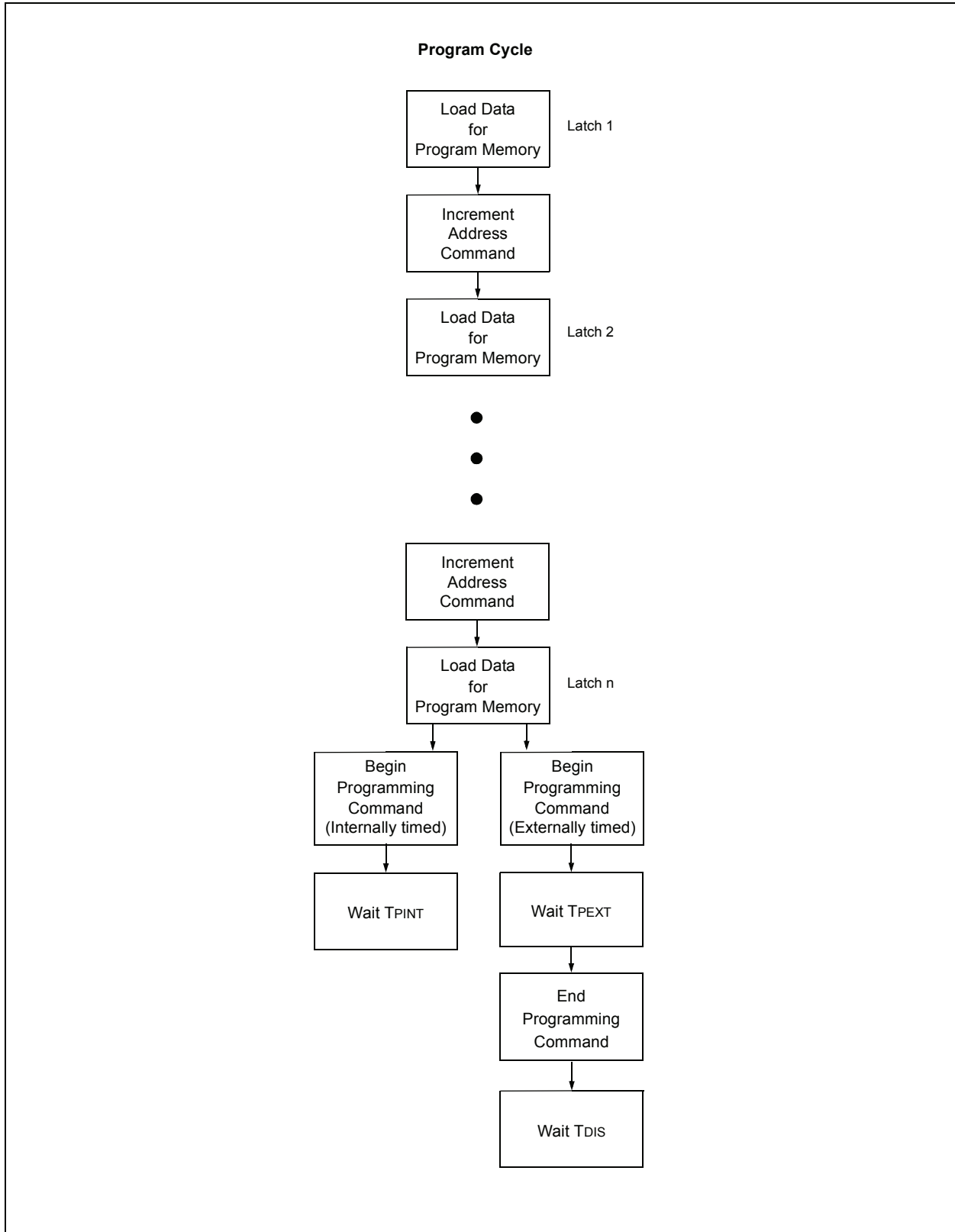
FIGURE 5-1: **DEVICE PROGRAM/VERIFY FLOWCHART**

```
                    ┌─────────┐
                    │  Start  │
                    └────┬────┘
                         │
                         ▼
                 ┌───────────────┐
                 │     Enter     │
                 │ Programming Mode │
                 └───────┬───────┘
                         │
                         ▼
                 ┌───────────────┐
                 │  Bulk Erase   │
                 │    Device     │
                 └───────┬───────┘
                         │
                         ▼
                 ┌───────────────┐
                 │ Write Program │
                 │  Memory(1)    │
                 └───────┬───────┘
                         │
                         ▼
                 ┌───────────────┐
                 │ Write User IDs│
                 └───────┬───────┘
                         │
                         ▼
                 ┌───────────────┐
                 │ Verify Program│
                 │    Memory     │
                 └───────┬───────┘
                         │
                         ▼
                 ┌───────────────┐
                 │Verify User IDs│
                 └───────┬───────┘
                         │
                         ▼
                 ┌───────────────┐
                 │ Write Configuration │
                 │    Words(2)   │
                 └───────┬───────┘
                         │
                         ▼
                 ┌───────────────┐
                 │Verify Configuration │
                 │    Words      │
                 └───────┬───────┘
                         │
                         ▼
                 ┌───────────────┐
                 │Exit Programming│
                 │     Mode      │
                 └───────┬───────┘
                         │
                         ▼
                    ┌─────────┐
                    │  Done   │
                    └─────────┘
```

Note 1: See Figure 5-2.
2: See Figure 5-5.

FIGURE 5-4: **MULTIPLE-WORD PROGRAM CYCLE**

Program Cycle

Load Data
for
Program Memory — Latch 1

↓

Increment
Address
Command

↓

Load Data
for
Program Memory — Latch 2

●
●
●

Increment
Address
Command

↓

Load Data
for
Program Memory — Latch n

Begin
Programming
Command
(Internally timed)

Begin
Programming
Command
(Externally timed)

Wait T_{PINT}

Wait T_{PEXT}

↓

End
Programming
Command

↓

Wait T_{DIS}

FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART

Note 1: This step is optional if device is erased or not previously programmed.
2: See Figure 5-3.
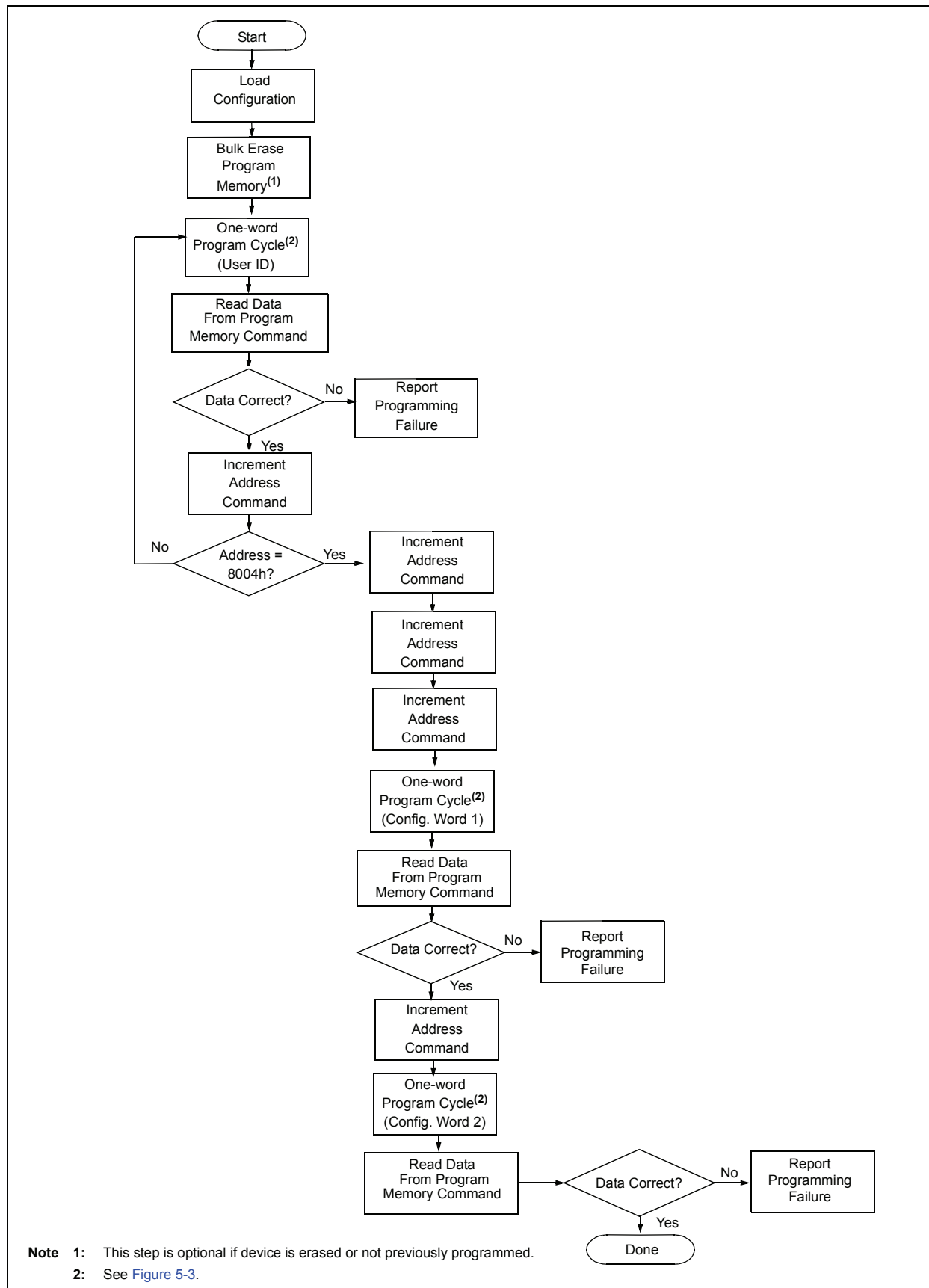
FIGURE 5-6: **ERASE FLOWCHART**

Note: This sequence does not erase the Calibration Words.
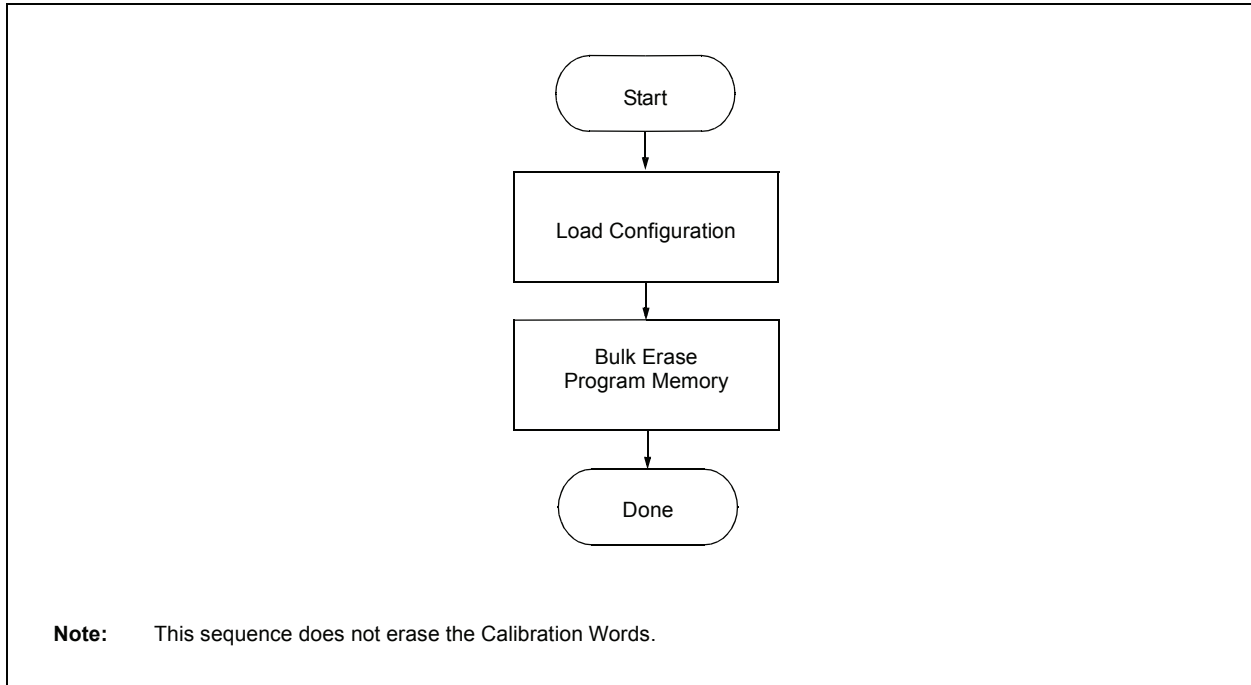
7.3.2 PROGRAM CODE PROTECTION ENABLED

With the program code protection enabled, the checksum is computed in the following manner: The Least Significant nibble of each user ID is used to create a 16-bit value. The masked value of user ID location 8000h is the Most Significant nibble. This sum of user IDs is summed with the Configuration Words (all unimplemented Configuration bits are masked to '0').

EXAMPLE 7-3: **CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC16F1527, BLANK DEVICE**

PIC16F1527		
	Configuration Word 1[2]	3F7Fh
	Configuration Word 1 mask[3]	3EFFh
	Configuration Word 2[2]	3FFFh
	Configuration Word 2 mask[3]	3E13h
	User ID (8000h)[1]	0006h
	User ID (8001h)[1]	0007h
	User ID (8002h)[1]	0001h
	User ID (8003h)[1]	0002h

Sum of User IDs[4] = (0006h and 000Fh) << 12 + (0007h and 000Fh) << 8 +
                       (0001h and 000Fh) << 4 + (0002h and 000Fh)
                     = 6000h + 0700h + 0010h + 0002h
                     = 6712h

Checksum = (3F7Fh and 3EFFh) + (3FFFh and 3E13h) + Sum of User IDs
          = 3E7Fh + 3713h + 6712h
          = DCA4h

Note 1: User ID values in this example are random values.

2: Configuration Word 1 and 2 = all bits are '1' except the code-protect enable bit.

3: Configuration Word 1 and 2 Mask = all Configuration Word bits are set to '1', except for unimplemented bits which read '0'.

4: << = shift left, thus the LSb of the first user ID value is the MSb of the sum of user IDs and so on, until the LSb of the last user ID value becomes the LSb of the sum of user IDs.

EXAMPLE 7-4: **CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC16LF1527, 00AAh AT FIRST AND LAST ADDRESS**

PIC16LF1527	Configuration Word 1[2]	3F7Fh
	Configuration Word 1 mask[3]	3EFFh
	Configuration Word 2[2]	3FFFh
	Configuration Word 2 mask[3], [5]	3E03h
	User ID (8000h)[1]	000Eh
	User ID (8001h)[1]	0008h
	User ID (8002h)[1]	0005h
	User ID (8003h)[1]	0008h
	Sum of User IDs[4]	= (000Eh and 000Fh) << 12 + (0008h and 000Fh) << 8 +
		(0005h and 000Fh) << 4 + (0008h and 000Fh)
		= E000h + 0800h + 0050h + 0008h
		= E858h
	Checksum	= (3F7Fh and 3EFFh) + (3FFFh and 3E03h) + Sum of User IDs
		= 3E7Fh +3E03h + E858h
		= 64DAh

Note 1: User ID values in this example are random values.

2: Configuration Word 1 and 2 = all bits are '1' except the code-protect enable bit.

3: Configuration Word 1 and 2 Mask = all Configuration Word bits are set to '1', except for unimplemented bits which read '0'.

4: << = shift left, thus the LSb of the first user ID value is the MSb of the sum of user IDs and so on, until the LSb of the last user ID value becomes the LSb of the sum of user IDs.

5: On the PIC16LF1527 device, the $\overline{\text{VCAPEN}}$ bit is not implemented in Configuration Word 2; thus, all unimplemented bits are '0'.

PIC16(L)F151X/152X

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
T$_{PINT}$	Internally timed programming operation time	—	—	2.5	ms	Program memory
		—	—	5	ms	Configuration Words
T$_{PEXT}$	Externally timed programming pulse	1.0	—	2.1	ms	**Note 1**
T$_{DIS}$	Time delay from program to compare (HV discharge time)	300	—	—	µs	
T$_{EXIT}$	Time delay when exiting Program/Verify mode	1	—	—	µs	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – V$_{DD}$ FIRST
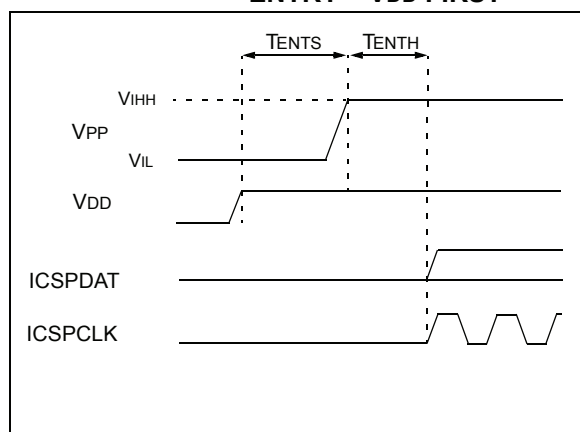
FIGURE 8-2: PROGRAMMING MODE ENTRY – V$_{PP}$ FIRST
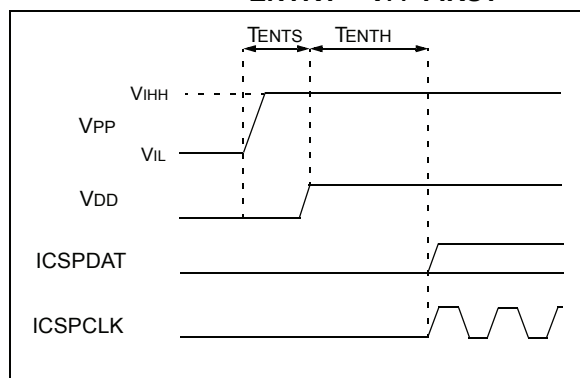
FIGURE 8-3: PROGRAMMING MODE EXIT – V$_{PP}$ LAST
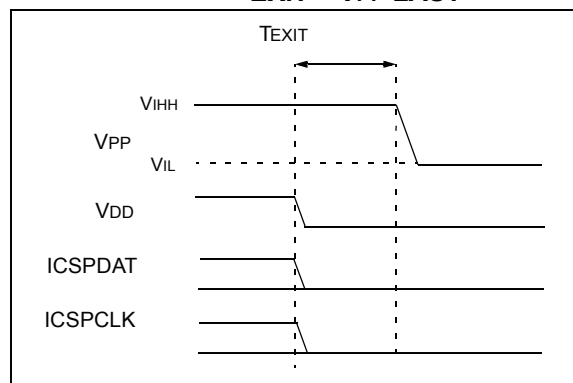
FIGURE 8-4: PROGRAMMING MODE EXIT – V$_{DD}$ LAST
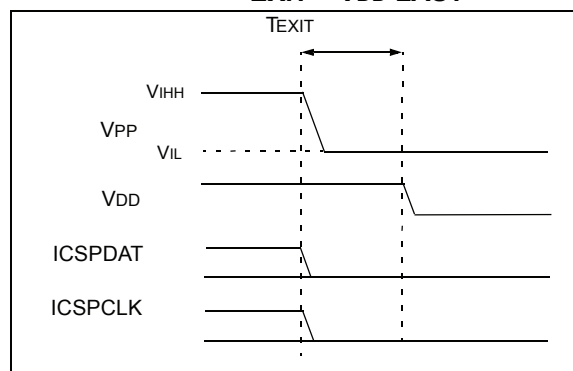
APPENDIX A: REVISION HISTORY

Revision A (08/2010)

Original release of this document.

Revision B (09/2011)

Added PIC16(L)F1512/1513 devices; Added new Figures 3-1 and 3-2; Updated Registers 3-1, 3-2 and 3-3 to new format; Updated Register 3-3 to add 2 kW and 4 kW Flash memory; Added Notes to Examples 7-1 to 7-4; Updated Table 8-1; Other minor corrections.

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• Microchip products meet the specification contained in their particular Microchip Data Sheet.

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