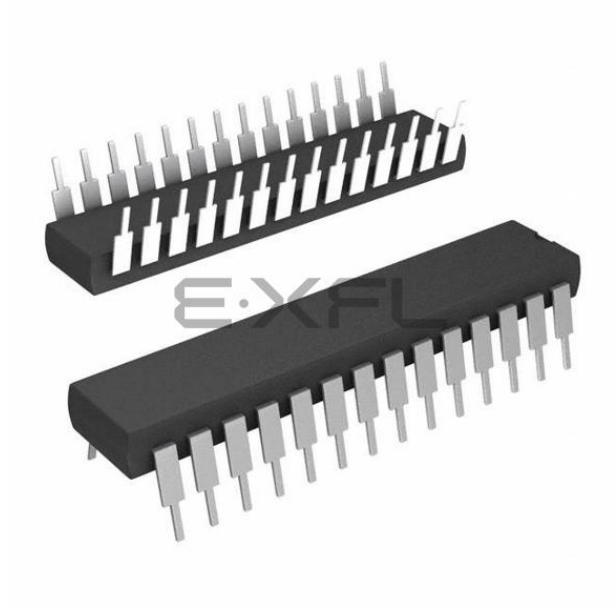

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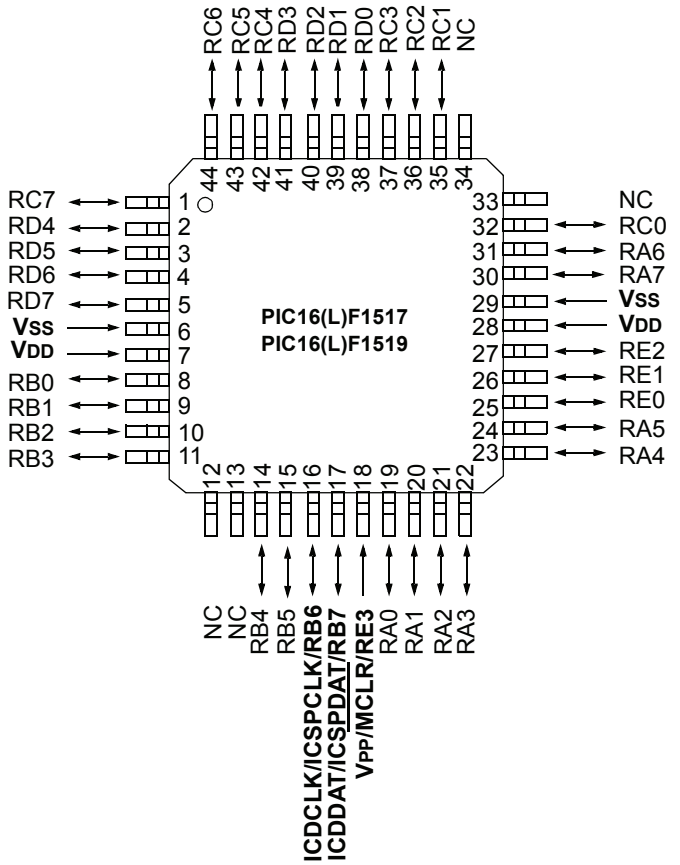
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1518-e-sp

FIGURE 2-5: 44-PIN TQFP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519

TQFP



3.0 MEMORY MAP

The memory for the PIC16(L)F151X/152X devices is broken into two sections: program memory and configuration memory. Only the size of the program memory changes between devices, the configuration memory remains the same.

FIGURE 3-1: PIC16(L)F1512 PROGRAM MEMORY MAPPING

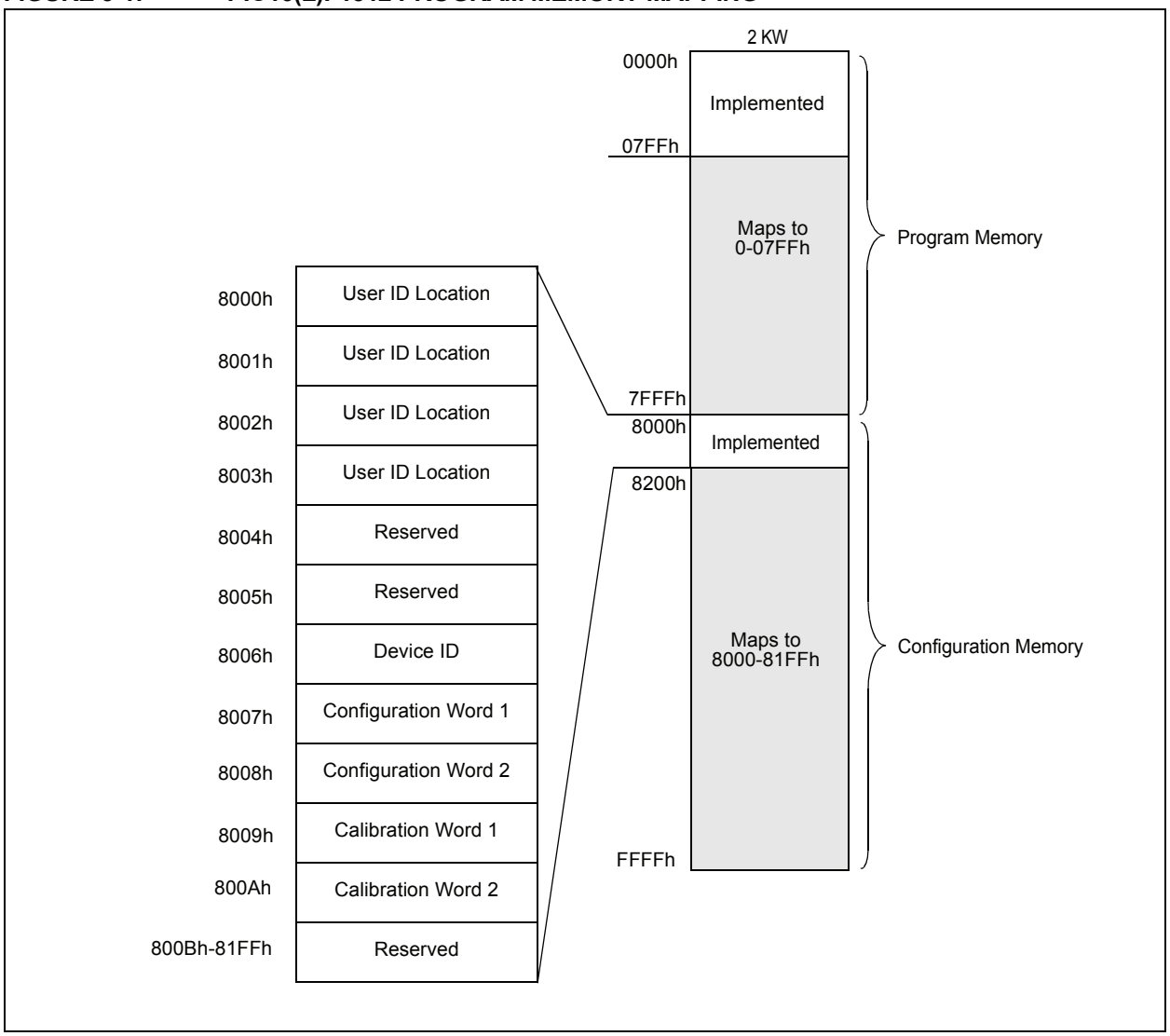


FIGURE 3-2: PIC16(L)F1513 PROGRAM MEMORY MAPPING

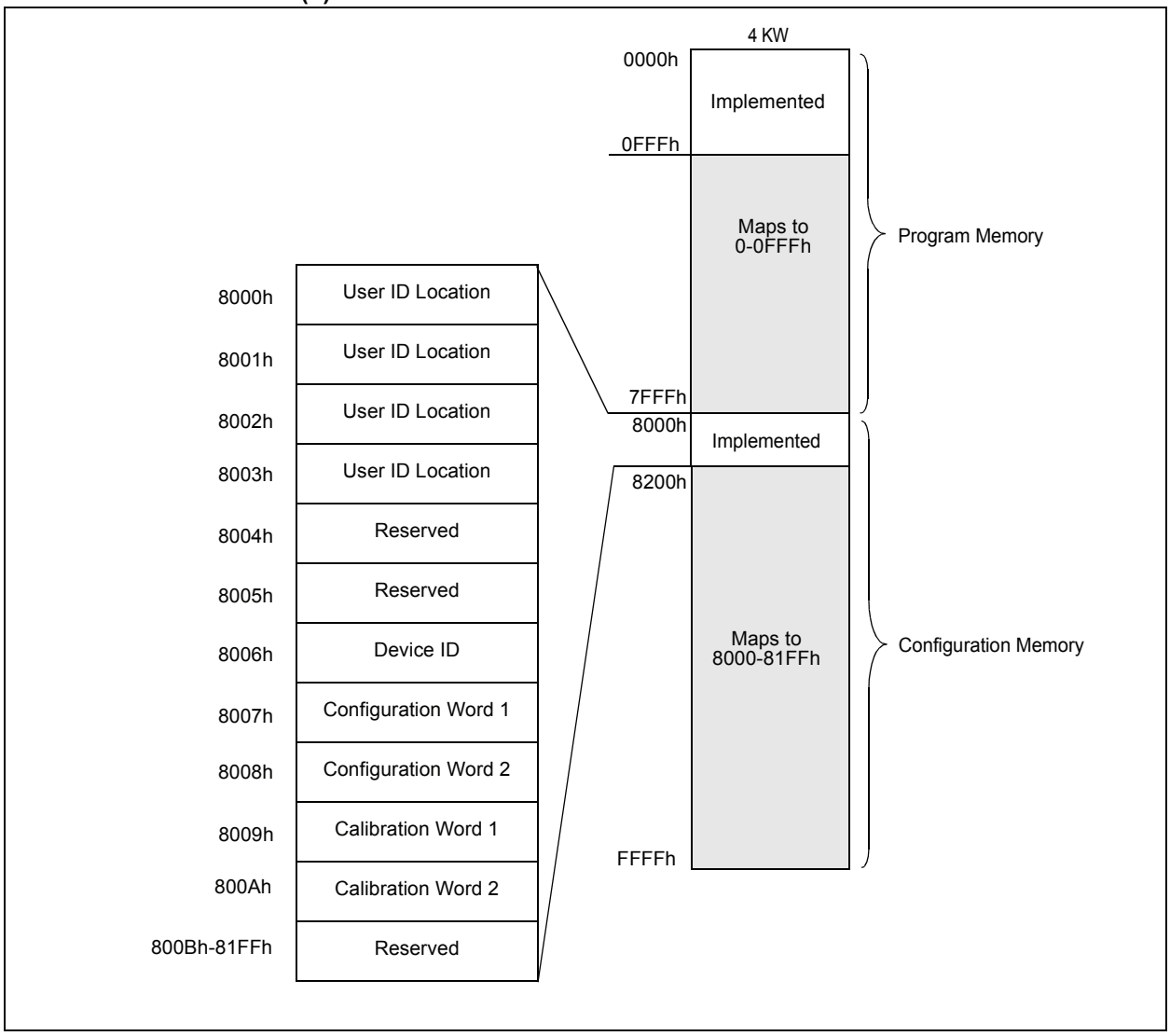
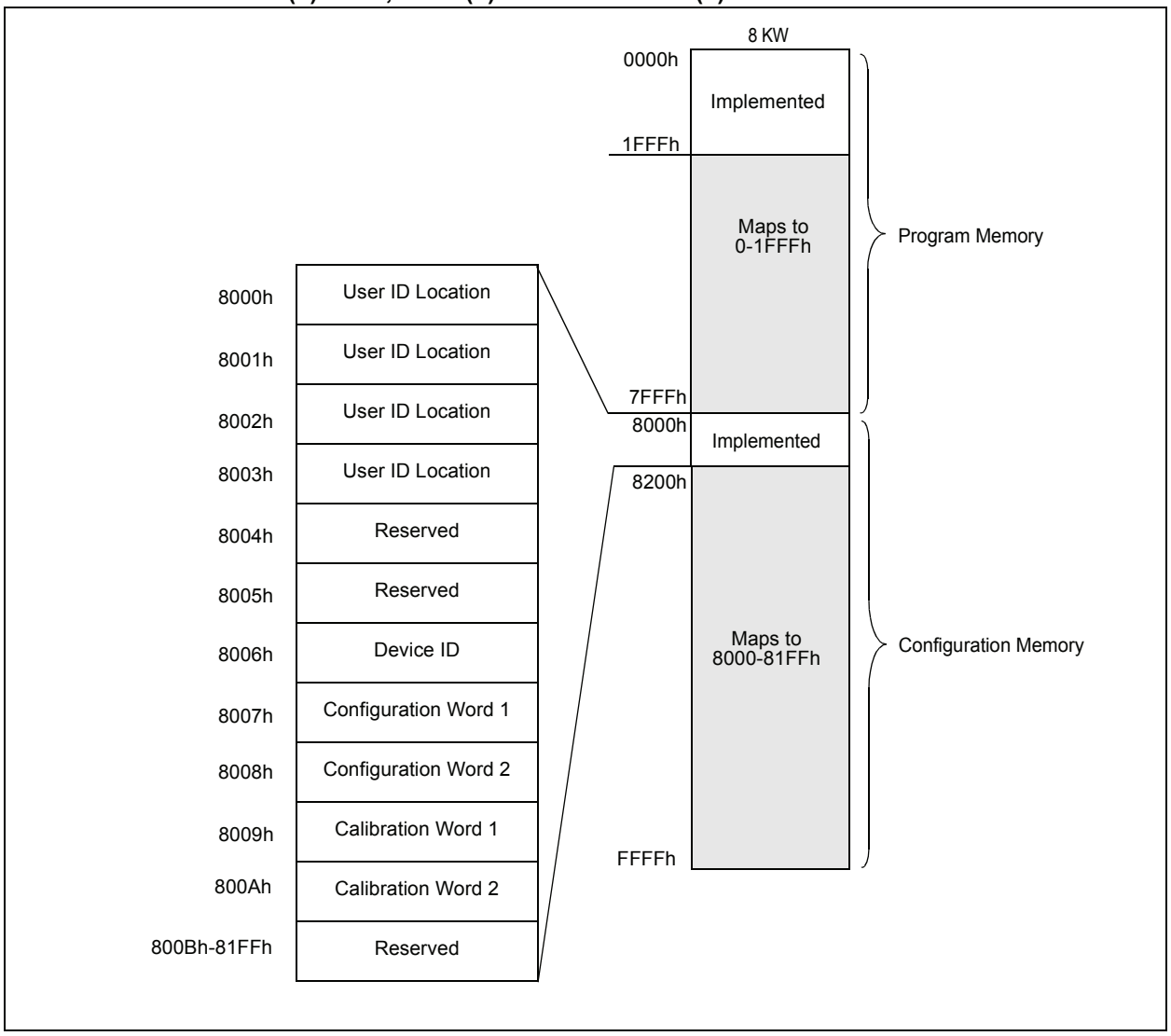


FIGURE 3-3: PIC16(L)F1526, PIC16(L)F1516 AND PIC16(L)F1517 PROGRAM MEMORY MAPPING



3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

Note:	MPLAB® IDE only displays the 7 Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the 7 LSbs be used if MPLAB IDE is the primary tool used to read these addresses.

3.2 Device ID

The device ID word is located at 8006h. This location is read-only and cannot be erased or modified.

REGISTER 3-1: DEVICE ID: DEVICE ID REGISTER(1)

R	R	R	R	R	R
DEV<8:3>					
bit 13					bit 8

R	R	R	R	R	R	R	R
DEV<2:0>			REV<4:0>				
bit 7							bit 0

Legend:	P = Programmable bit	U = Unimplemented bit, read as ‘0’
R = Readable bit	W = Writable bit	‘0’ = Bit is cleared
-n = Value at POR	‘1’ = Bit is set	x = Bit is unknown

bit 13-5 **DEV<8:0>:** Device ID bits
These bits are used to identify the part number.

bit 4-0 **REV<4:0>:** Revision ID bits
These bits are used to identify the revision.

Note 1: This location cannot be written.

TABLE 3-1: DEVICE ID VALUES

DEVICE	DEVICE ID VALUES	
	DEV	REV
PIC16F1527	0001 0101 101	x xxxx
PIC16F1526	0001 0101 100	x xxxx
PIC16LF1527	0001 0101 111	x xxxx
PIC16LF1526	0001 0101 110	x xxxx
PIC16F1519	0001 0110 111	x xxxx
PIC16F1518	0001 0110 110	x xxxx
PIC16F1517	0001 0110 101	x xxxx
PIC16F1516	0001 0110 100	x xxxx
PIC16F1513	0001 0110 010	x xxxx
PIC16F1512	0001 0111 000	x xxxx
PIC16LF1519	0001 0111 111	x xxxx
PIC16LF1518	0001 0111 110	x xxxx
PIC16LF1517	0001 0111 101	x xxxx
PIC16LF1516	0001 0111 100	x xxxx
PIC16LF1513	0001 0111 010	x xxxx
PIC16LF1512	0001 0111 001	x xxxx

3.3 Configuration Words

There are two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

The internal calibration values are factory calibrated and stored in Calibration Words 1 and 2 (8009h, 800Ah).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

REGISTER 3-2: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 12 **IESO:** Internal External Switchover bit
1 = Internal/External Switchover mode is enabled
0 = Internal/External Switchover mode is disabled

bit 11 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
0 = CLKOUT function is enabled on CLKOUT pin

bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits(1)
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the PCON register
00 = BOR disabled

bit 8 **Unimplemented:** Read as '1'

bit 7 **$\overline{\text{CP}}$:** Code Protection bit(2)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6 **MCLRE:** $\overline{\text{MCLR}}$/VPP Pin Function Select bit
If LVP bit = 1:
This bit is ignored.
If LVP bit = 0:
1 = $\overline{\text{MCLR}}$/VPP pin function is $\overline{\text{MCLR}}$; Weak pull-up enabled.
0 = $\overline{\text{MCLR}}$/VPP pin function is digital input; $\overline{\text{MCLR}}$ internally disabled; Weak pull-up under control of WPUA register.

bit 5 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
11 = WDT enabled
10 = WDT enabled while running and disabled in Sleep
01 = WDT controlled by the SWDTEN bit in the WDTCON register
00 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = ECH: External Clock, High-Power mode: on CLKIN pin
110 = ECM: External Clock, Medium-Power mode: on CLKIN pin
101 = ECL: External Clock, Low-Power mode: on CLKIN pin
100 = INTOSC oscillator: I/O function on OSC1 pin
011 = EXTRC oscillator: RC function on OSC1 pin
010 = HS oscillator: High-speed crystal/resonator on OSC2 pin and OSC1 pin
001 = XT oscillator: Crystal/resonator on OSC2 pin and OSC1 pin
000 = LP oscillator: Low-power crystal on OSC2 pin and OSC1 pin

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire program memory will be erased when the code protection is turned off.

REGISTER 3-3: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
LVP	$\overline{\text{DEBUG}}$	$\overline{\text{LPBOR}}$	BORV	STVREN	—
bit 13					bit 8

U-1	U-1	U-1	R/P-1	U-1	U-1	R/P-1	R/P-1
—	—	—	$\overline{\text{VCAPEN}}$(2)	—	—	WRT<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **LVP:** Low-Voltage Programming Enable bit(1)
1 = Low-voltage programming enabled
0 = HV on $\overline{\text{MCLR}}$/VPP must be used for programming

bit 12 **$\overline{\text{DEBUG}}$:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
0 = In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger

bit 11 **$\overline{\text{LPBOR}}$:** Low-Power BOR
1 = Low-Power BOR is disabled
0 = Low-Power BOR is enabled

bit 10 **BORV:** Brown-out Reset Voltage Selection bit
1 = Brown-out Reset voltage (VBOR), low trip point selected
0 = Brown-out Reset voltage (VBOR), high trip point selected

bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
1 = Stack Overflow or Underflow will cause a Reset
0 = Stack Overflow or Underflow will not cause a Reset

bit 8-5 **Unimplemented:** Read as '1'

bit 4 **$\overline{\text{VCAPEN}}$:** Voltage Regulator Capacitor Enable bits(1)
0 = VCAP functionality is enabled on VCAP pin
1 = All VCAP pin functions are disabled

bit 3-2 **Unimplemented:** Read as '1'

bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits
2 kW Flash memory (PIC16(L)F1512):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
01 = 000h to FFFh write-protected, 400h to 7FFh may be modified by PMCON control
00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control
4 kW Flash memory (PIC16(L)F1513):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control
01 = 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control
00 = 000h to FFFh write-protected, no addresses may be modified by PMCON control
8 kW Flash memory (PIC16F/LF1516/1517/1526):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 1FFFh may be modified by PMCON control
01 = 000h to FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control
00 = 000h to 1FFFh write-protected, no addresses may be modified by PMCON control
16 kW Flash memory (PIC16F/LF1518/1519/1527):
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 3FFFh may be modified by PMCON control
01 = 000h to 1FFFh write-protected, 2000h to 3FFFh may be modified by PMCON control
00 = 000h to 3FFFh write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.
2: Applies to PIC16F151X/152X devices only. On PIC16LF151X/152X, the $\overline{\text{VCAPEN}}$ bit is unimplemented.

4.3 Program/Verify Commands

The PIC16(L)F151X/152X implements 10 programming commands; each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING

Command	Mapping							Data/Note
	Binary (MSb … LSb)						Hex	
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data For Program Memory	x	0	0	0	1	0	02h	0, data (14), 0
Read Data From Program Memory	x	0	0	1	0	0	04h	0, data (14), 0
Increment Address	x	0	0	1	1	0	06h	—
Reset Address	x	1	0	1	1	0	16h	—
Begin Internally Timed Programming	x	0	1	0	0	0	08h	—
Begin Externally Timed Programming	x	1	1	0	0	0	18h	—
End Externally Timed Programming	x	0	1	0	1	0	0Ah	—
Bulk Erase Program Memory	x	0	1	0	0	1	09h	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	11h	Internally Timed

4.3.1 LOAD CONFIGURATION

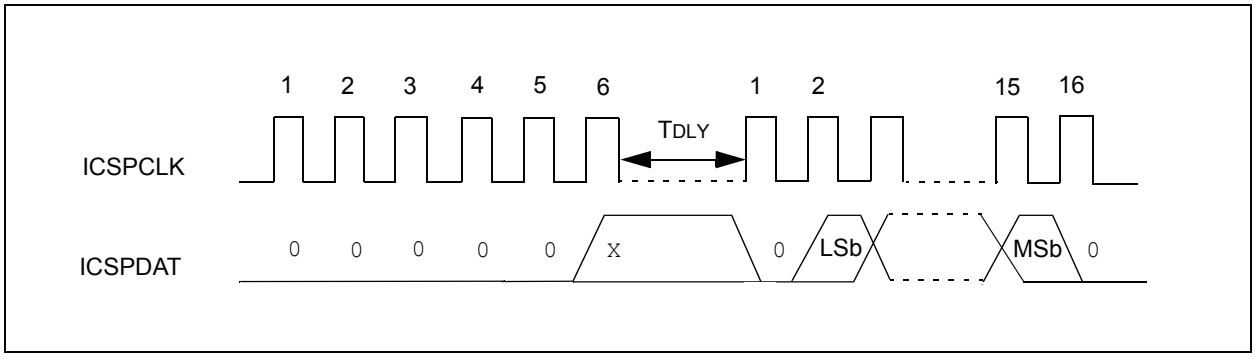
The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

Note: Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

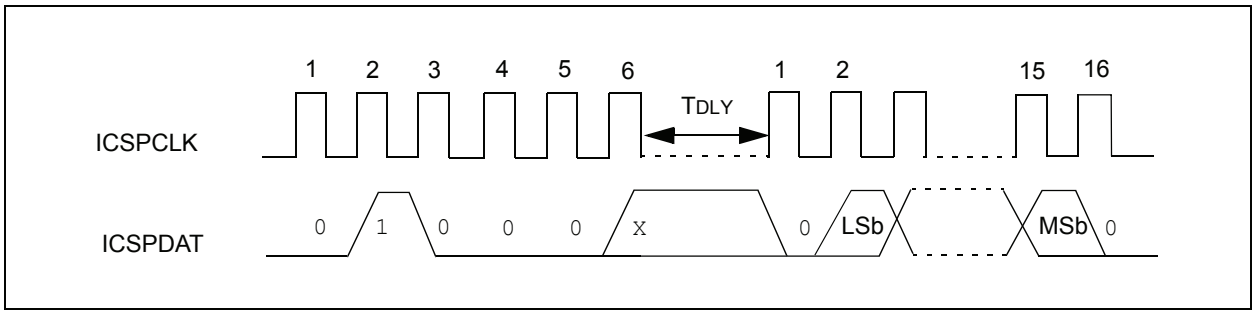
FIGURE 4-1: LOAD CONFIGURATION



4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY



4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros (see Figure 4-3).

FIGURE 4-3: READ DATA FROM PROGRAM MEMORY

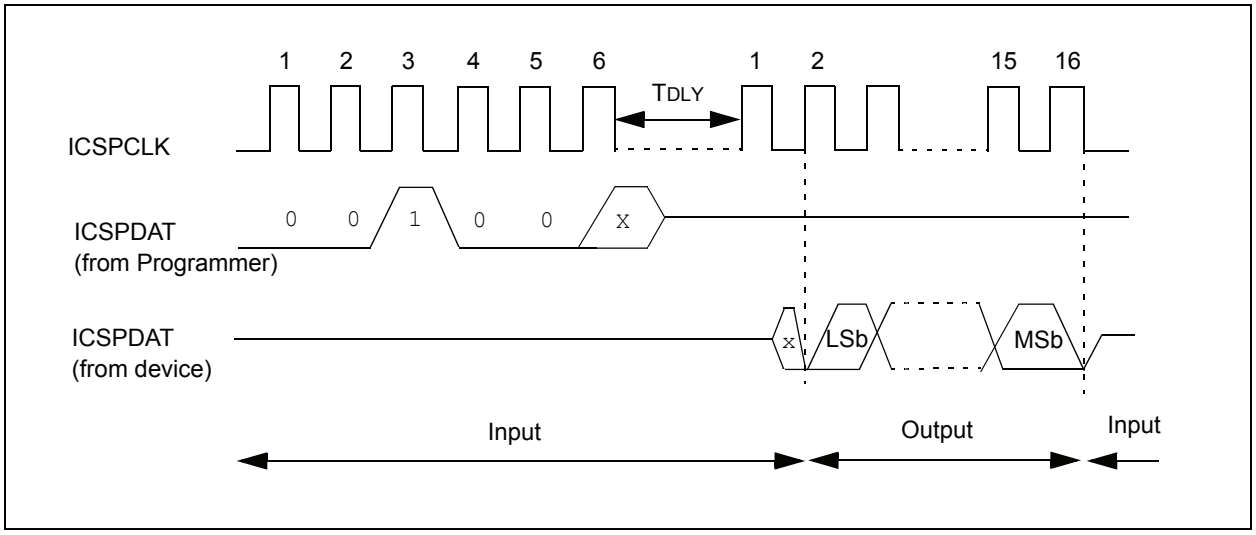
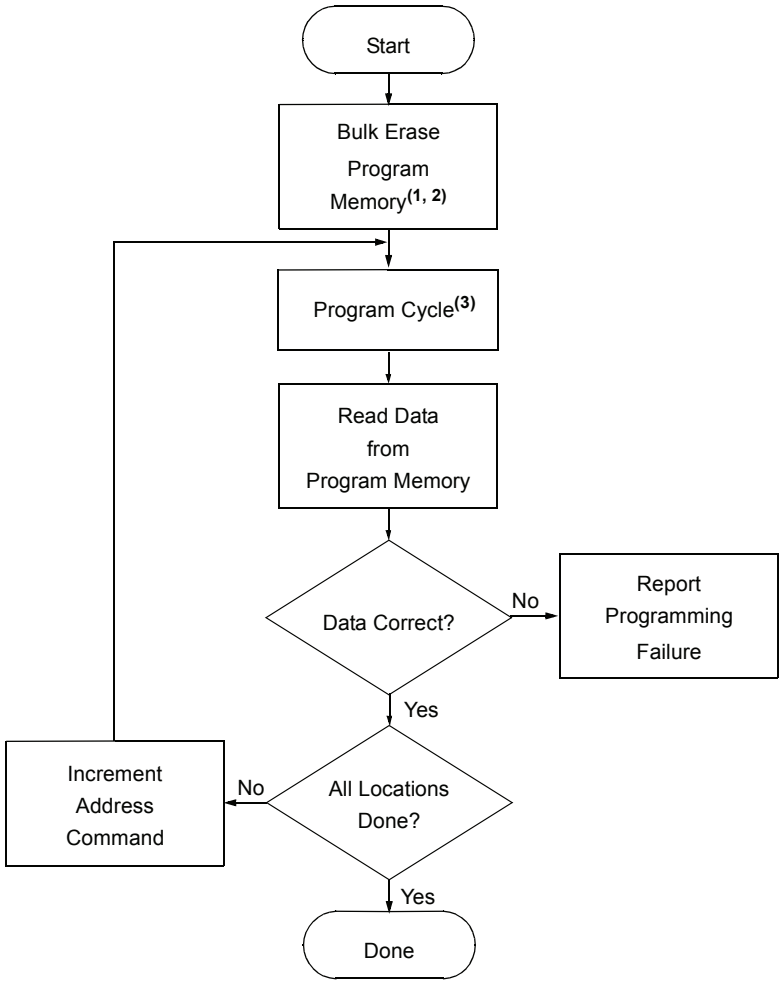


FIGURE 5-2: PROGRAM MEMORY FLOWCHART

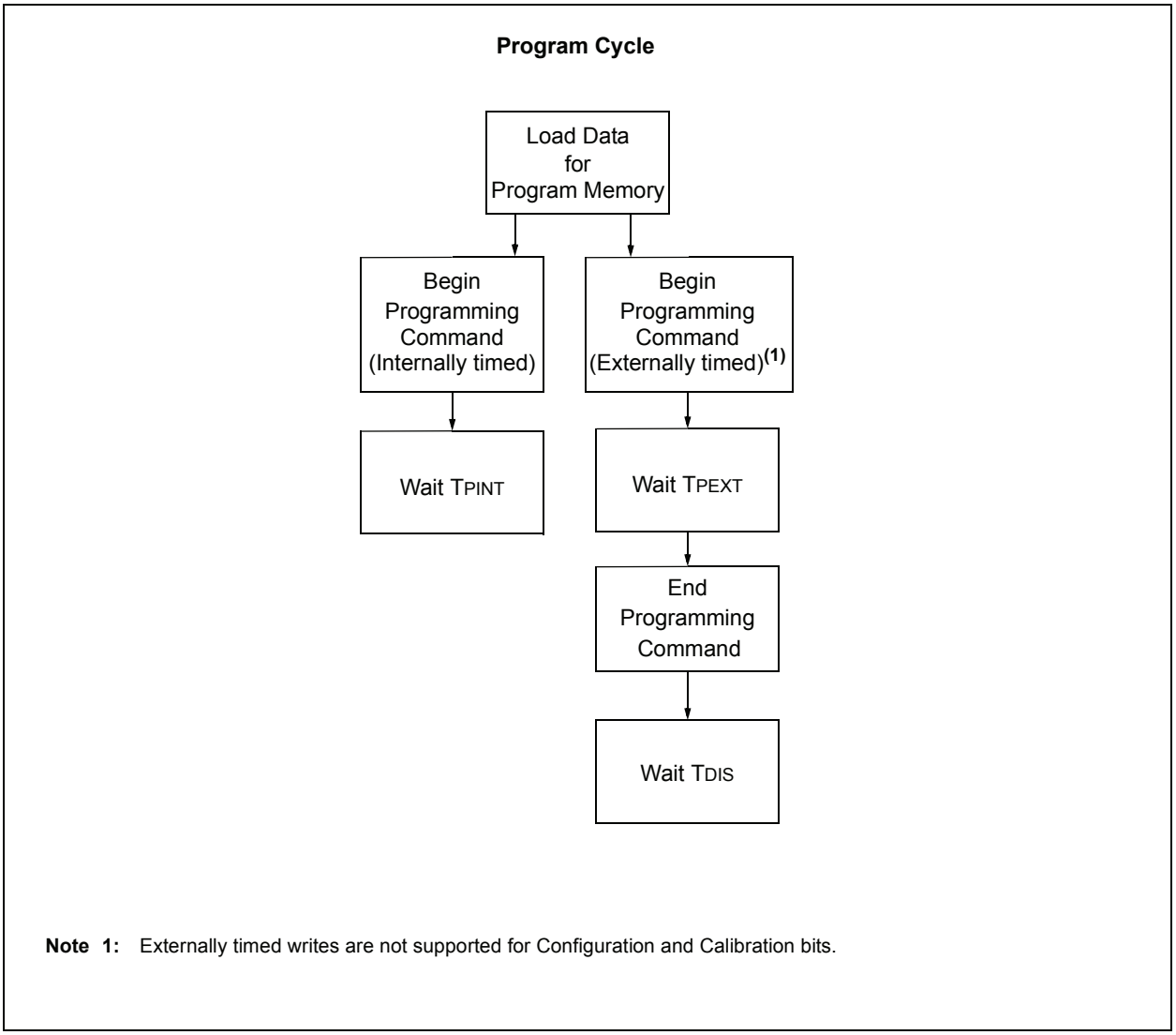


Note 1: This step is optional if device has already been erased or has not been previously programmed.

2: If the device is code-protected or must be completely erased, then Bulk Erase device per Figure 5-6.

3: See Figure 5-3 or Figure 5-4.

FIGURE 5-3: ONE-WORD PROGRAM CYCLE



Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

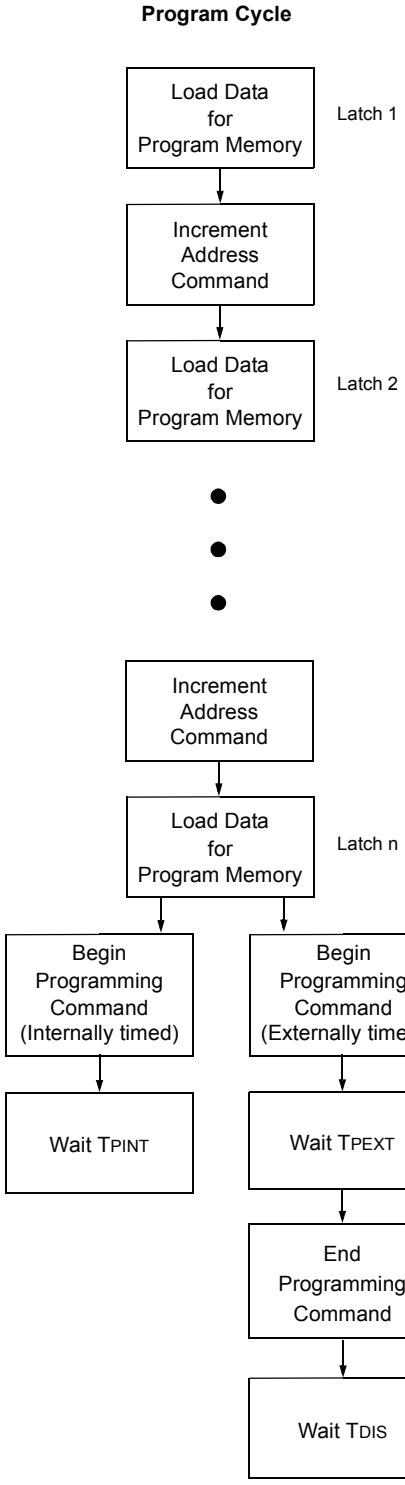
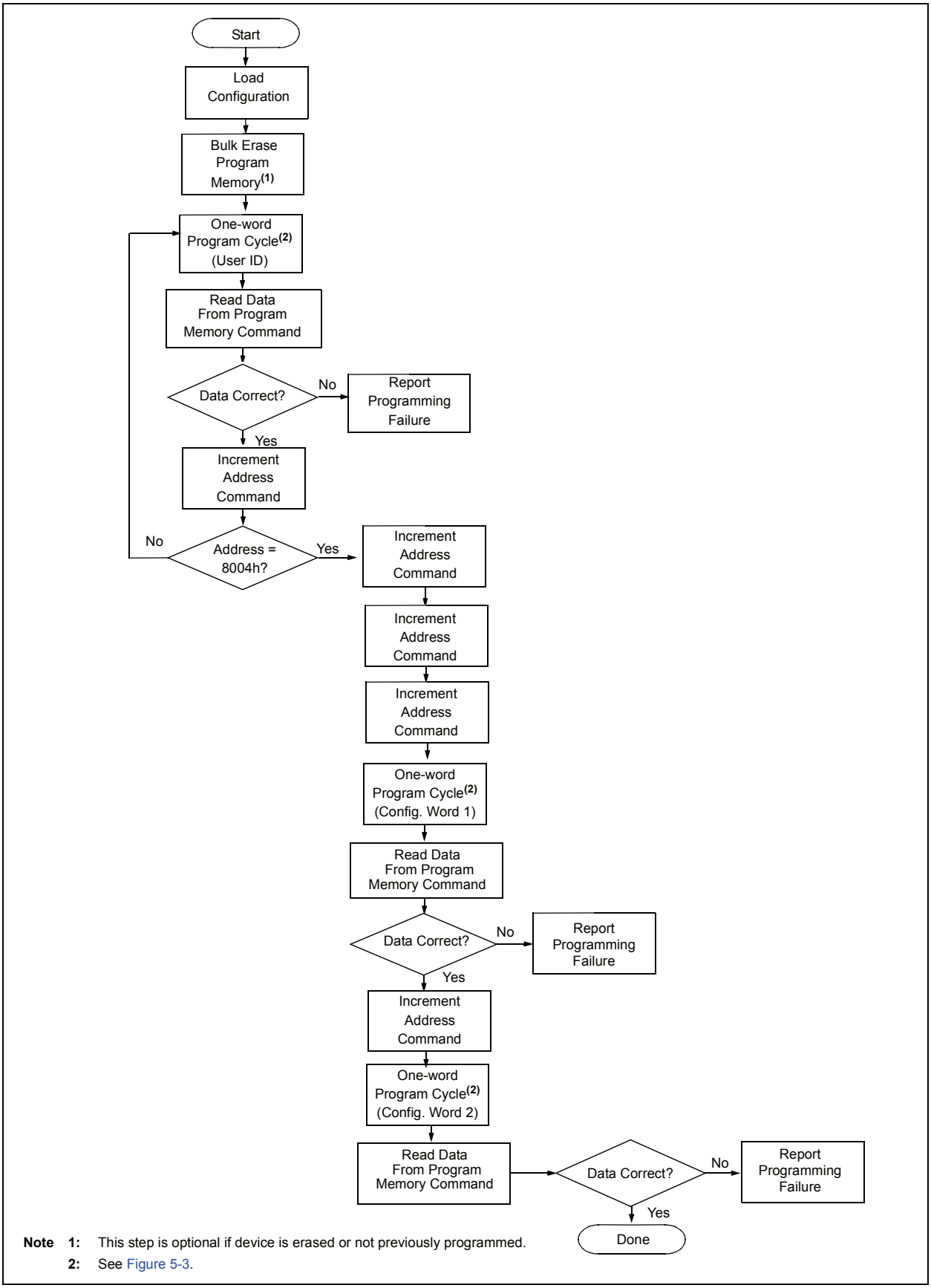


FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART



Note 1: This step is optional if device is erased or not previously programmed.

2: See Figure 5-3.

6.0 CODE PROTECTION

Code protection is controlled using the $\overline{CP}$ bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFFh) read as all '0'. Further programming is disabled for the program memory (0000h-7FFFh).

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Program Memory

Code protection is enabled by programming the $\overline{CP}$ bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: Configuration Word 1 is stored at 8007h on the PIC16(L)F151X/152X. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID and Revision

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID (excluding the revision) against the value read from the part. On a mismatch condition the programmer should generate a warning message.

8.0 ELECTRICAL SPECIFICATIONS

Refer to device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS			Standard Operating Conditions Production tested at 25°C				
Sym.	**Characteristics**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
Supply Voltages and Currents							
V_{DD}	Supply Voltage (V_{DDMIN}, V_{DDMAX})	PIC16F151X PIC16F152X	2.3	—	5.5	V	
		PIC16LF151X PIC16LF152X	1.8	—	3.6	V	
V_{PEW}	Read/Write and Row Erase operations		V_{DDMIN}	—	V_{DDMAX}	V	
V_{PBE}	Bulk Erase operations		2.7	—	V_{DDMAX}	V	
I_{DDI}	Current on V_{DD}, Idle		—	—	1.0	mA	
I_{DDP}	Current on V_{DD}, Programming		—	—	3.0	mA	
	V_{PP}						
I_{PP}	Current on $\overline{MCLR}/V_{PP}$		—	—	600	μA	
V_{IHH}	High voltage on $\overline{MCLR}/V_{PP}$ for Program/Verify mode entry		8.0	—	9.0	V	
T_{VHHR}	$\overline{MCLR}$ rise time (V_{IL} to V_{IHH}) for Program/Verify mode entry		—	—	1.0	μs	
	I/O pins						
V_{IH}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) input high level		0.8 V_{DD}	—	—	V	
V_{IL}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) input low level		—	—	0.2 V_{DD}	V	
V_{OH}	ICSPDAT output high level		V_{DD}-0.7 V_{DD}-0.7 V_{DD}-0.7	—	—	V	I_{OH} = 3.5 mA, V_{DD} = 5V I_{OH} = 3 mA, V_{DD} = 3.3V I_{OH} = 2 mA, V_{DD} = 1.8V
V_{OL}	ICSPDAT output low level		—	—	V_{SS}+0.6 V_{SS}+0.6 V_{SS}+0.6	V	I_{OH} = 8 mA, V_{DD} = 5V I_{OH} = 6 mA, V_{DD} = 3.3V I_{OH} = 3 mA, V_{DD} = 1.8V
Programming Mode Entry and Exit							
T_{ENTS}	Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before V_{DD} or $\overline{MCLR}$↑		100	—	—	ns	
T_{ENTH}	Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after V_{DD} or $\overline{MCLR}$↑		250	—	—	μs	
Serial Program/Verify							
T_{CKL}	Clock Low Pulse Width		100	—	—	ns	
T_{CKH}	Clock High Pulse Width		100	—	—	ns	
T_{DS}	Data in setup time before clock↓		100	—	—	ns	
T_{DH}	Data in hold time after clock↓		100	—	—	ns	
T_{CO}	Clock↑ to data out valid (during a Read Data command)		0	—	80	ns	
T_{LZD}	Clock↓ to data low-impedance (during a Read Data command)		0	—	80	ns	
T_{HZD}	Clock↓ to data high-impedance (during a Read Data command)		0	—	80	ns	
T_{DLY}	Data input not driven to next clock input (delay required between command/data or command/command)		1.0	—	—	μs	
T_{ERAB}	Bulk Erase cycle time		—	—	5	ms	
T_{ERAR}	Row Erase cycle time		—	—	2.5	ms	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

FIGURE 8-5: CLOCK AND DATA TIMING

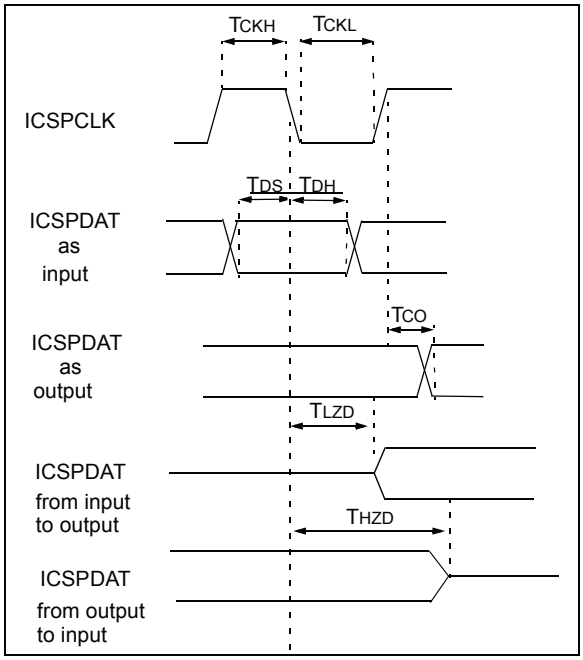


FIGURE 8-6: WRITE COMMAND-PAYLOAD TIMING

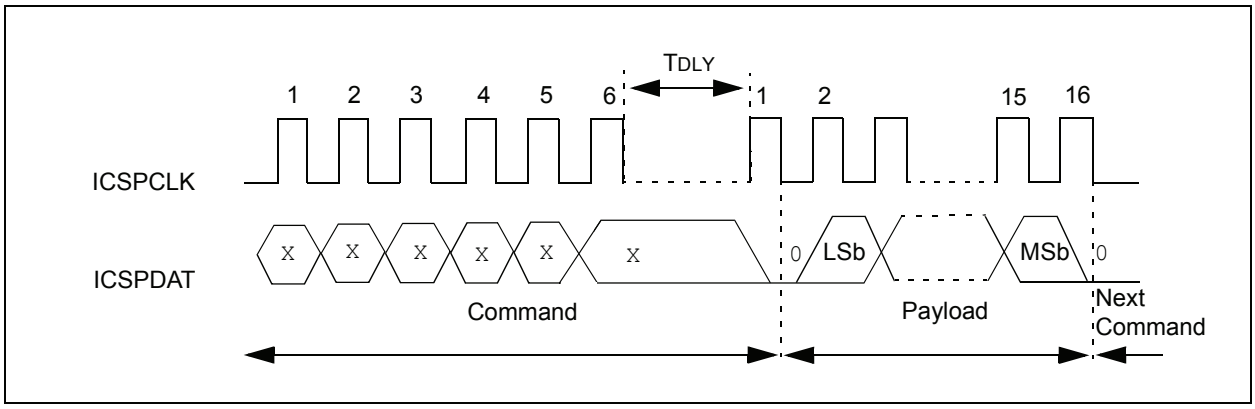


FIGURE 8-7: READ COMMAND-PAYLOAD TIMING

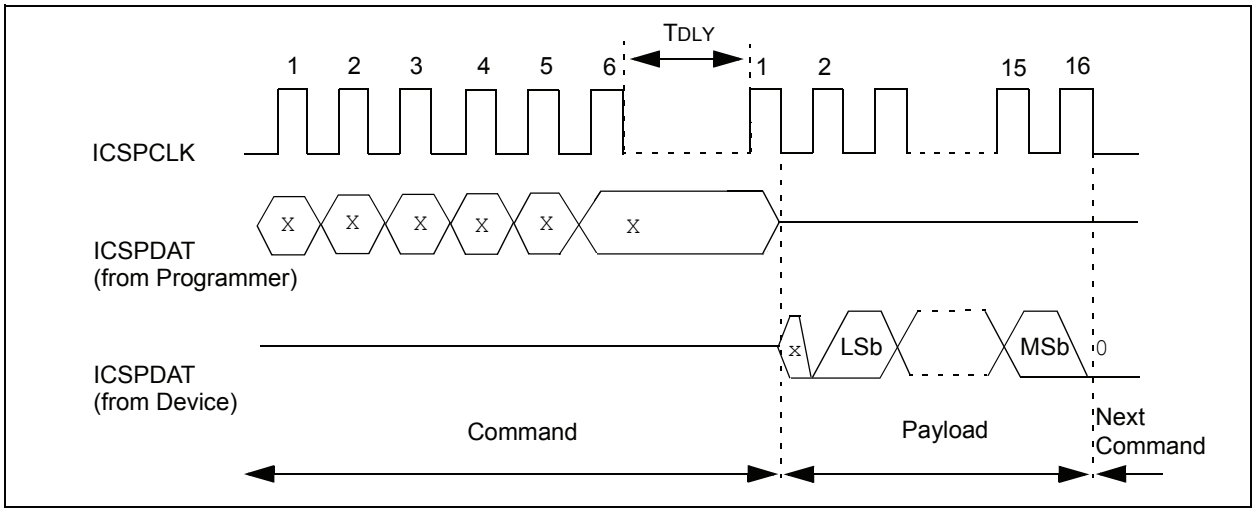


FIGURE 8-8: LVP ENTRY (POWERED)

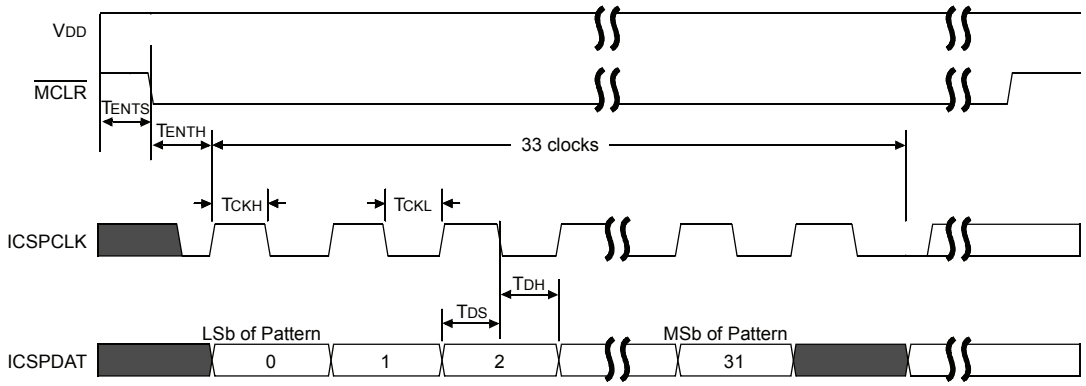
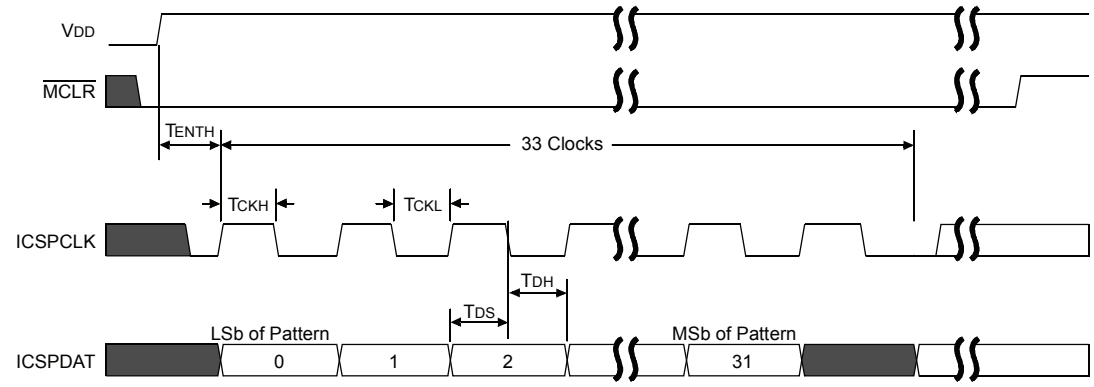


FIGURE 8-9: LVP ENTRY (POWERING UP)



Note 1: Sequence matching can start with no edge on $\overline{MCLR}$ first.

NOTES:

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