What is "<u>Embedded - Microcontrollers</u>"?

"<u>Embedded - Microcontrollers</u>" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1518t-i-ss

FIGURE 2-6: **64-PIN QFN DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527**

QFN

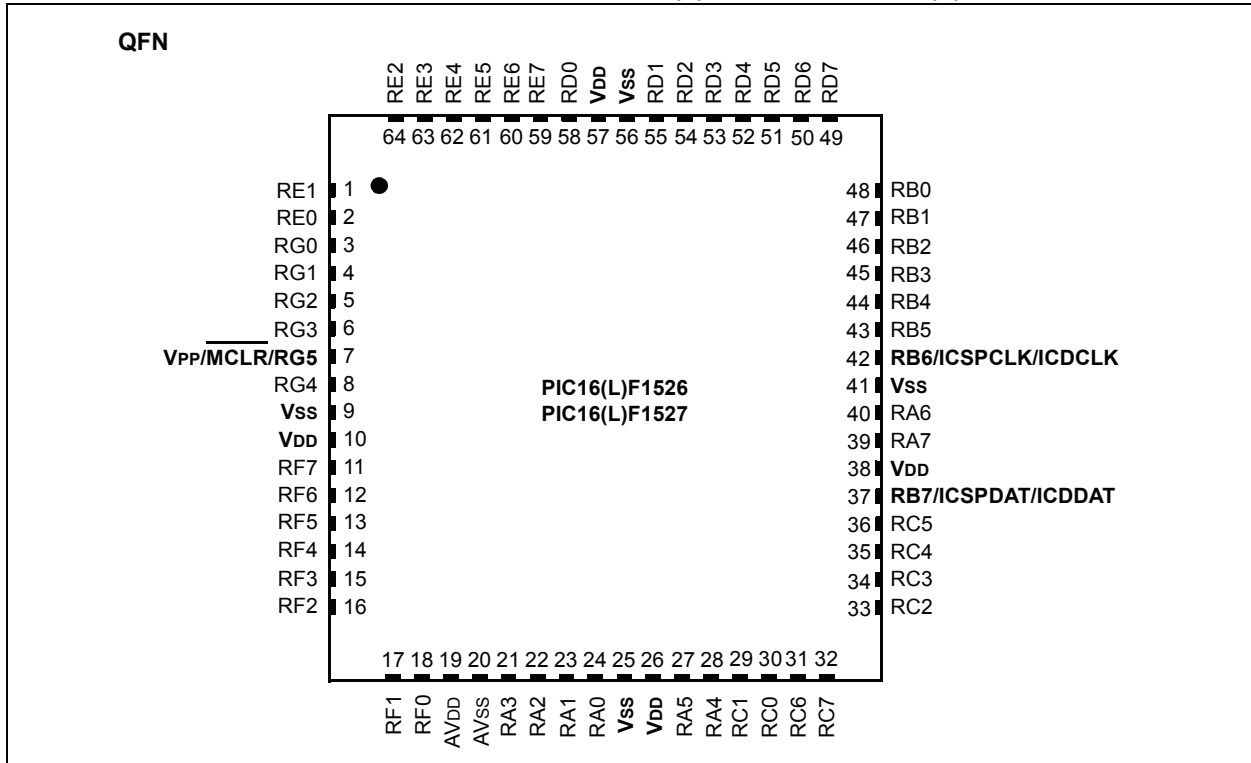PIC16(L)F1526
PIC16(L)F1527

FIGURE 2-7: **64-PIN TQFP DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527**

TQFP

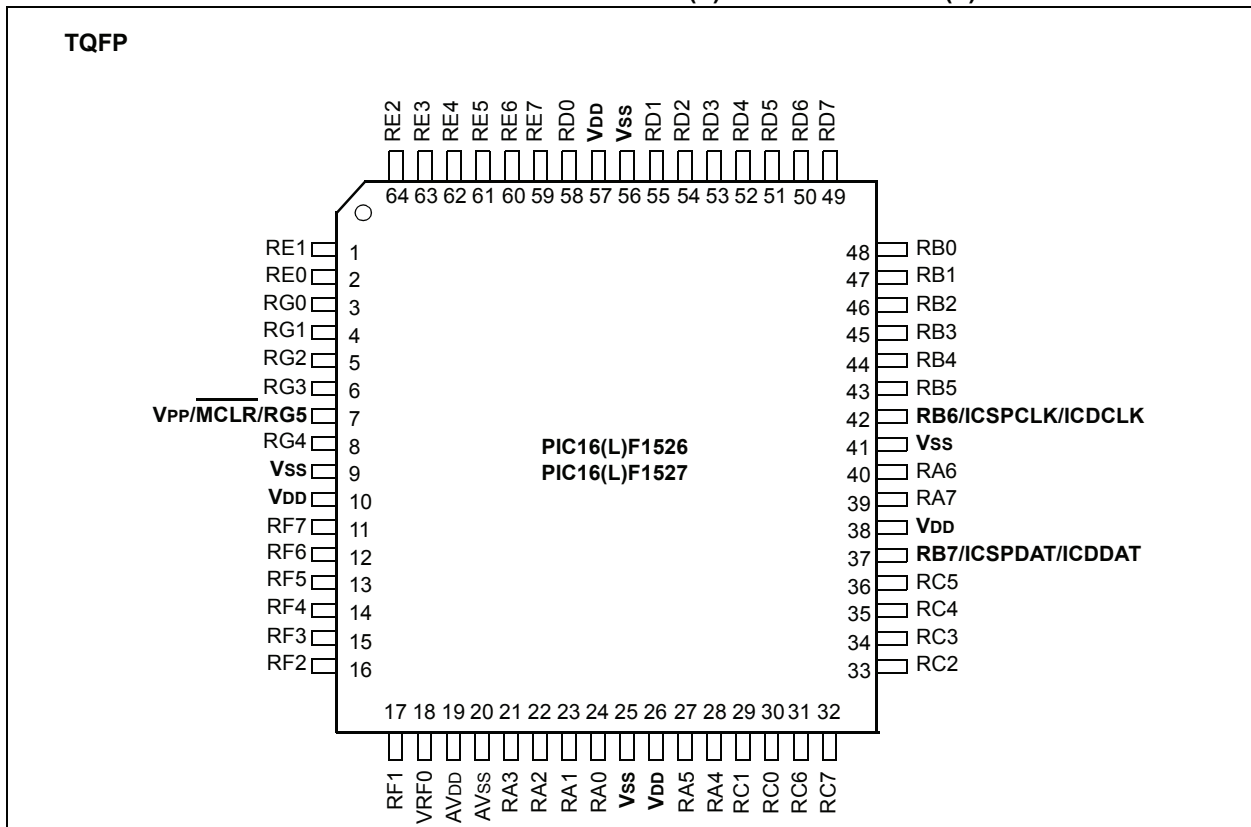PIC16(L)F1526
PIC16(L)F1527

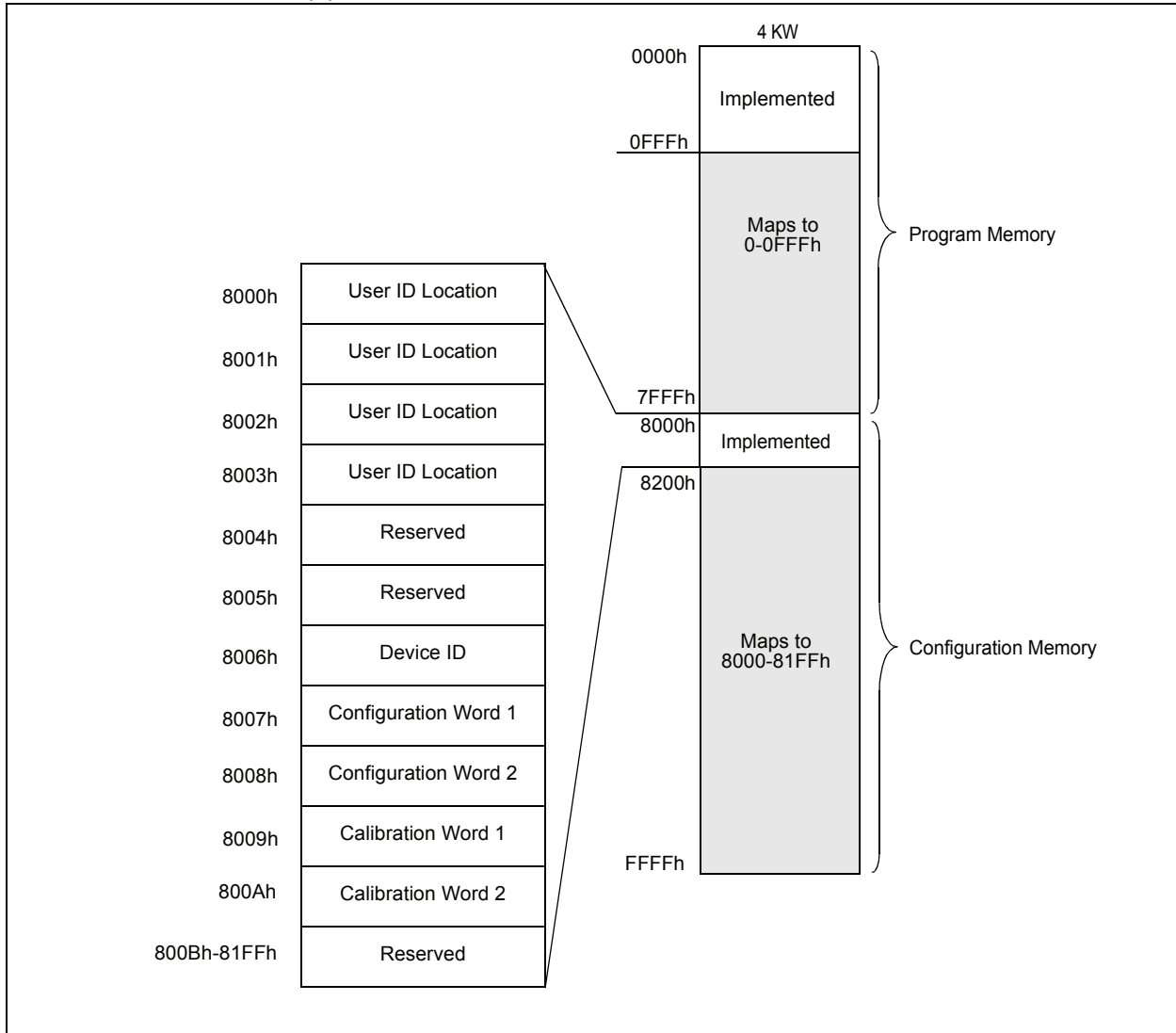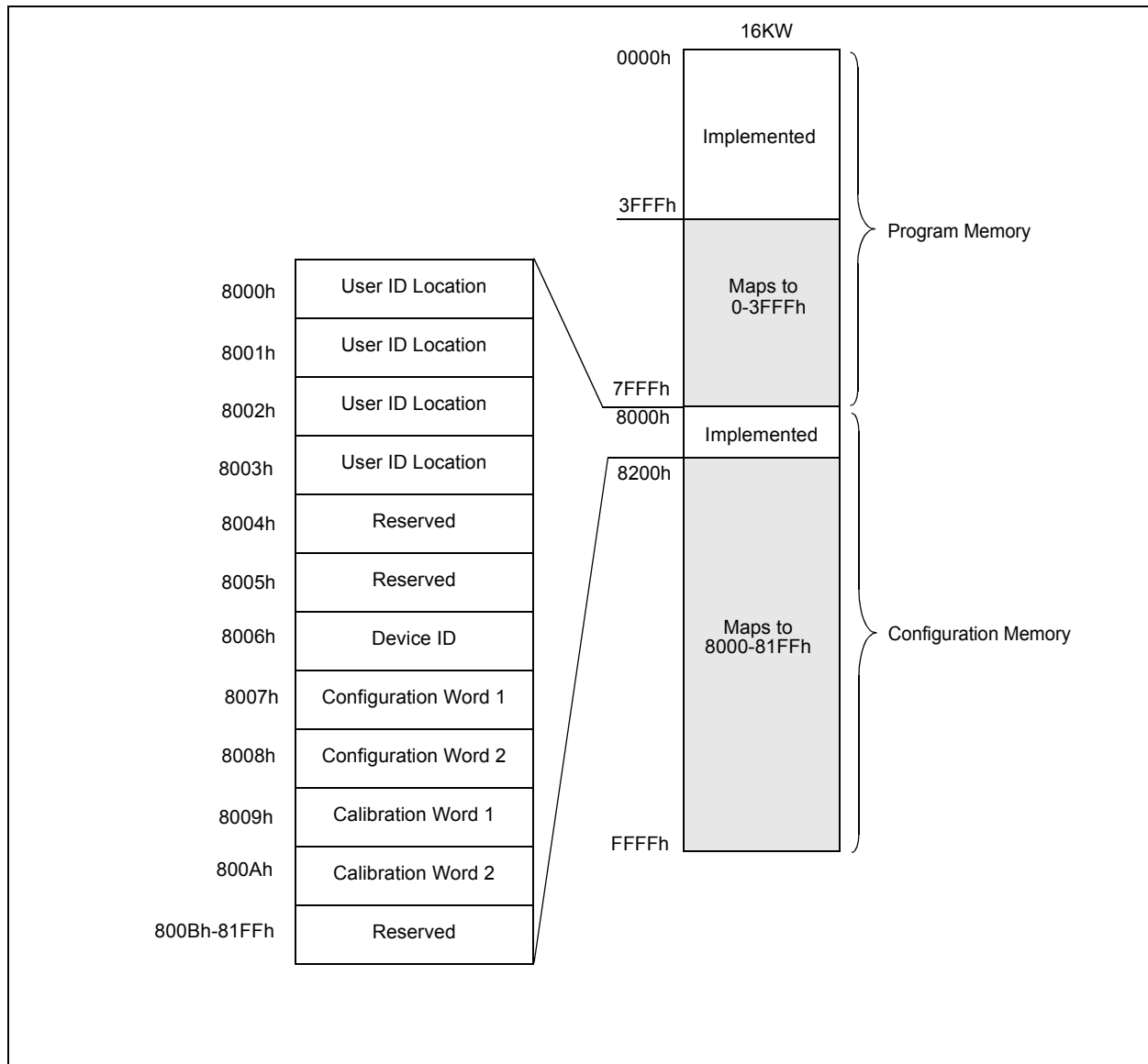**FIGURE 3-2:** **PIC16(L)F1513 PROGRAM MEMORY MAPPING**

FIGURE 3-4: **PIC16(L)F1527, PIC16(L)F1518 AND PIC16(L)F1519 PROGRAM MEMORY MAPPING**

PIC16(L)F151X/152X

REGISTER 3-2: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
FCMEN	IESO	CLKOUTEN	BOREN<1:0>		—
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP	MCLRE	PWRTE	WDTE<1:0>		FOSC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 12 **IESO:** Internal External Switchover bit
1 = Internal/External Switchover mode is enabled
0 = Internal/External Switchover mode is disabled

bit 11 **CLKOUTEN:** Clock Out Enable bit
1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
0 = CLKOUT function is enabled on CLKOUT pin

bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits[1]
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the PCON register
00 = BOR disabled

bit 8 **Unimplemented:** Read as '1'

bit 7 **CP:** Code Protection bit[2]
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6 **MCLRE:** MCLR/VPP Pin Function Select bit
If LVP bit = 1:
    This bit is ignored.
If LVP bit = 0:
    1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
    0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUA register.

bit 5 **PWRTE:** Power-up Timer Enable bit[1]
1 = PWRT disabled
0 = PWRT enabled

bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
11 = WDT enabled
10 = WDT enabled while running and disabled in Sleep
01 = WDT controlled by the SWDTEN bit in the WDTCON register
00 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = ECH: External Clock, High-Power mode: on CLKIN pin
110 = ECM: External Clock, Medium-Power mode: on CLKIN pin
101 = ECL: External Clock, Low-Power mode: on CLKIN pin
100 = INTOSC oscillator: I/O function on OSC1 pin
011 = EXTRC oscillator: RC function on OSC1 pin
010 = HS oscillator: High-speed crystal/resonator on OSC2 pin and OSC1 pin
001 = XT oscillator: Crystal/resonator on OSC2 pin and OSC1 pin
000 = LP oscillator: Low-power crystal on OSC2 pin and OSC1 pin

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire program memory will be erased when the code protection is turned off.

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REGISTER 3-3: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
LVP	$\overline{\text{DEBUG}}$	$\overline{\text{LPBOR}}$	BORV	STVREN	—
bit 13					bit 8

U-1	U-1	U-1	R/P-1	U-1	U-1	R/P-1	R/P-1
—	—	—	$\overline{\text{VCAPEN}}$[(2)]	—	—	WRT<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **LVP:** Low-Voltage Programming Enable bit[(1)]
1 = Low-voltage programming enabled
0 = HV on $\overline{\text{MCLR}}$/VPP must be used for programming

bit 12 **$\overline{\text{DEBUG}}$:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
0 = In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger

bit 11 **$\overline{\text{LPBOR}}$:** Low-Power BOR
1 = Low-Power BOR is disabled
0 = Low-Power BOR is enabled

bit 10 **BORV:** Brown-out Reset Voltage Selection bit
1 = Brown-out Reset voltage (VBOR), low trip point selected
0 = Brown-out Reset voltage (VBOR), high trip point selected

bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
1 = Stack Overflow or Underflow will cause a Reset
0 = Stack Overflow or Underflow will not cause a Reset

bit 8-5 **Unimplemented:** Read as '1'

bit 4 **$\overline{\text{VCAPEN}}$:** Voltage Regulator Capacitor Enable bits[(1)]
0 = VCAP functionality is enabled on VCAP pin
1 = All VCAP pin functions are disabled

bit 3-2 **Unimplemented:** Read as '1'

bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits
2 kW Flash memory (PIC16(L)F1512):
    11 = Write protection off
    10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
    01 = 000h to FFFh write-protected, 400h to 7FFh may be modified by PMCON control
    00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control
4 kW Flash memory (PIC16(L)F1513):
    11 = Write protection off
    10 = 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control
    01 = 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control
    00 = 000h to FFFh write-protected, no addresses may be modified by PMCON control
8 kW Flash memory (PIC16F/LF1516/1517/1526):
    11 = Write protection off
    10 = 000h to 1FFh write-protected, 200h to 1FFFh may be modified by PMCON control
    01 = 000h to FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control
    00 = 000h to 1FFFh write-protected, no addresses may be modified by PMCON control
16 kW Flash memory (PIC16F/LF1518/1519/1527):
    11 = Write protection off
    10 = 000h to 1FFh write-protected, 200h to 3FFFh may be modified by PMCON control
    01 = 000h to 1FFFh write-protected, 2000h to 3FFFh may be modified by PMCON control
    00 = 000h to 3FFFh write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.
    2: Applies to PIC16F151X/152X devices only. On PIC16LF151X/152X, the $\overline{\text{VCAPEN}}$ bit is unimplemented.

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{MCLR}$ from 0V to VIHH.
3. Raise the voltage on VDD FROM 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when Configuration Word 1 has $\overline{MCLR}$ disabled (MCLRE = 0), the power-up time is disabled ($\overline{PWRTE}$ = 0), the internal oscillator is selected (FOSC = 100), and ICSPCLK and ICSPDAT pins are driven by the user application, the device will execute code. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in Figure 8-2.

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{MCLR}$ from VDD or below to VIHH.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-1.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{MCLR}$ to VDD or lower (VIL). See Figures 8-3 and 8-4.

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the PIC16(L)F151X/152X devices to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{MCLR}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{MCLR}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 8-8 and Figure 8-9.

Exiting Program/Verify mode is done by no longer driving $\overline{MCLR}$ to VIL. See Figure 8-8 and Figure 8-9.

> **Note:** To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

4.3 Program/Verify Commands

The PIC16(L)F151X/152X implements 10 programming commands; each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of T_{DLY} between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING

| Command	Mapping							Data/Note
	Binary (MSb … LSb)						Hex	
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data For Program Memory	x	0	0	0	1	0	02h	0, data (14), 0
Read Data From Program Memory	x	0	0	1	0	0	04h	0, data (14), 0
Increment Address	x	0	0	1	1	0	06h	—
Reset Address	x	1	0	1	1	0	16h	—
Begin Internally Timed Programming	x	0	1	0	0	0	08h	—
Begin Externally Timed Programming	x	1	1	0	0	0	18h	—
End Externally Timed Programming	x	0	1	0	1	0	0Ah	—
Bulk Erase Program Memory	x	0	1	0	0	1	09h	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	11h	Internally Timed

4.3.1 LOAD CONFIGURATION

The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

> **Note:** Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

FIGURE 4-1: LOAD CONFIGURATION
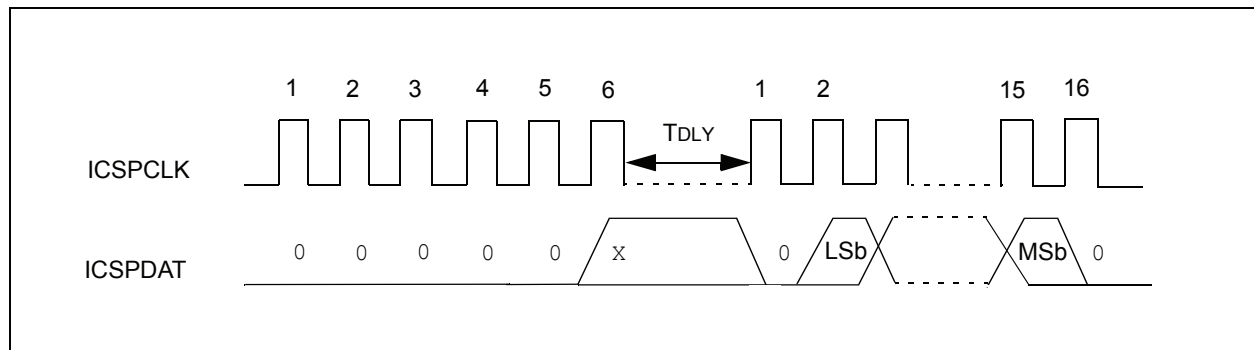
PIC16(L)F151X/152X

4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).
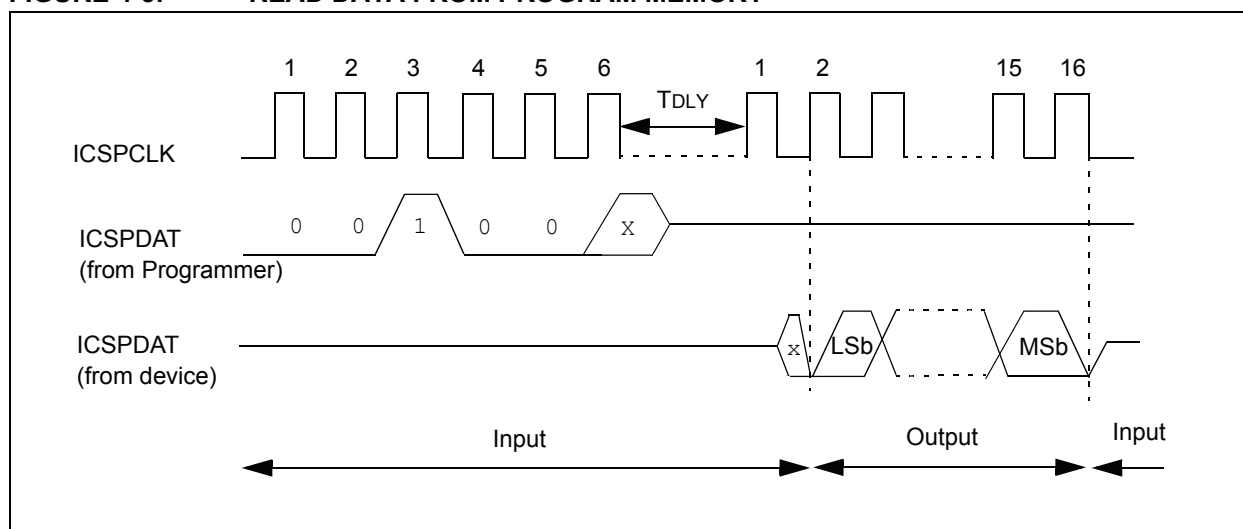
FIGURE 4-2: **LOAD DATA FOR PROGRAM MEMORY**
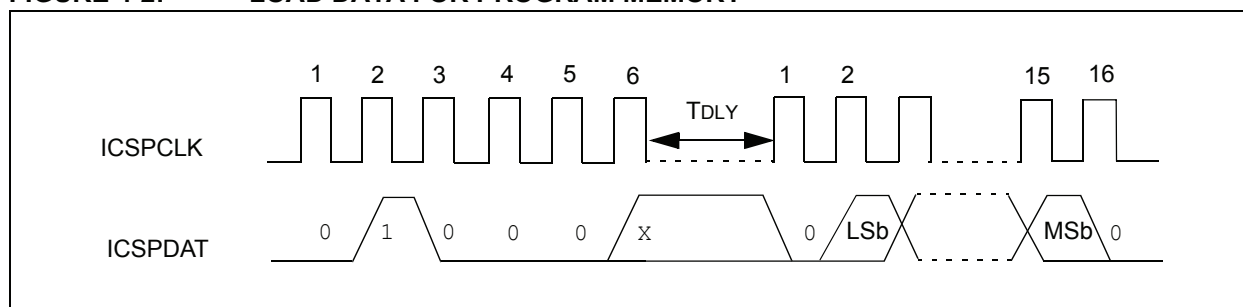
4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected (CP), the data will be read as zeros (see Figure 4-3).

FIGURE 4-3: **READ DATA FROM PROGRAM MEMORY**

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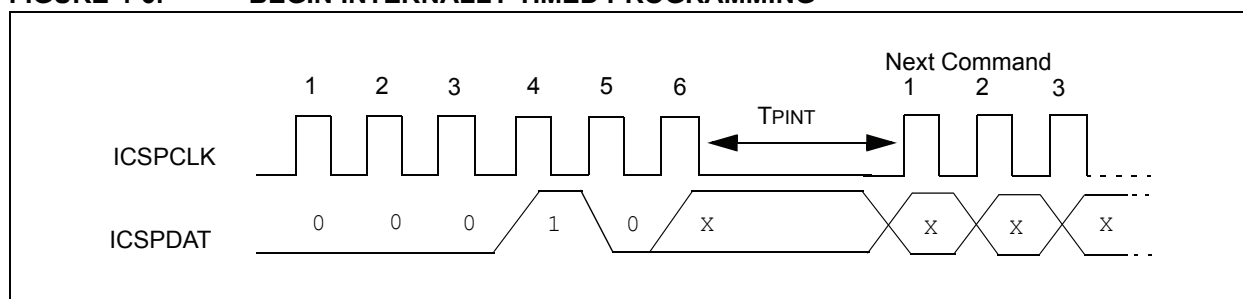
PIC16(L)F151X/152X

4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, T_{PINT}, for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed.

**FIGURE 4-6:   BEGIN INTERNALLY TIMED PROGRAMMING**

4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming the End Externally Timed Programming command must be sent in the specified time window defined by T_{PEXT} (see Figure 4-7).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 4-7:   BEGIN EXTERNALLY TIMED PROGRAMMING

Advance Information
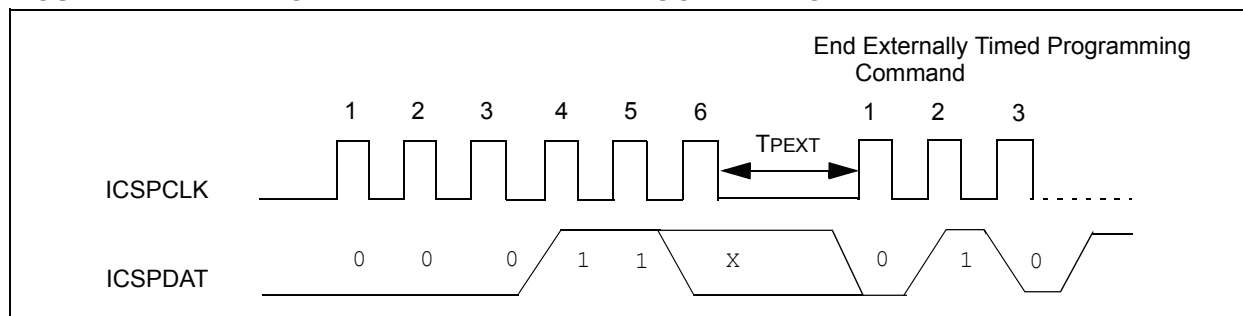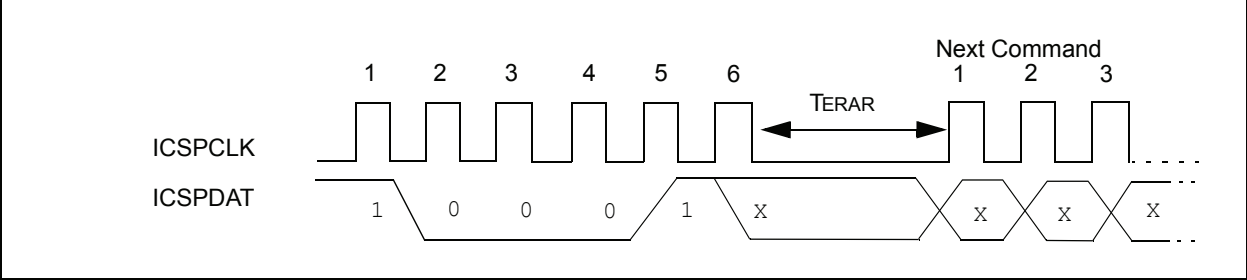
PIC16(L)F151X/152X

4.3.10 ROW ERASE PROGRAM MEMORY

The Row Erase Program Memory command will erase an individual row. Refer to Table 4-2 for row sizes of specific devices and the PC bits used to address them. If the program memory is code-protected the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h the Row Erase Program Memory command will only erase the user ID locations regardless of the setting of the $\overline{\text{CP}}$ Configuration bit.

After receiving the Row Erase Program Memory command the erase will not complete until the time interval, TERAR, has expired.
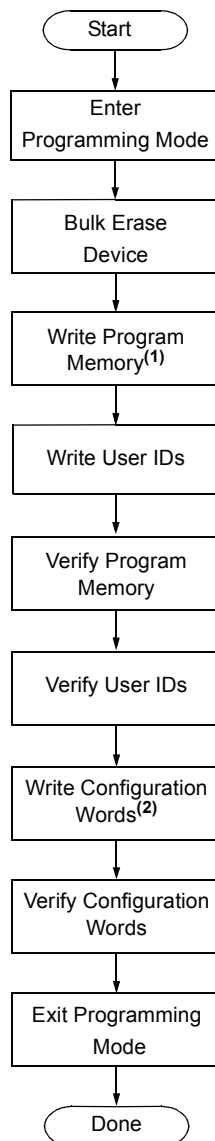
TABLE 4-2: PROGRAMMING ROW SIZE AND LATCHES

Devices	PC	Row Size	Number of Latches
PIC16(L)F151X/152X	<15:5>	32	32

FIGURE 4-10: ROW ERASE PROGRAM MEMORY

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PIC16(L)F151X/152X

Note 1: See Figure 5-2.
   2: See Figure 5-5.

FIGURE 5-2: **PROGRAM MEMORY FLOWCHART**
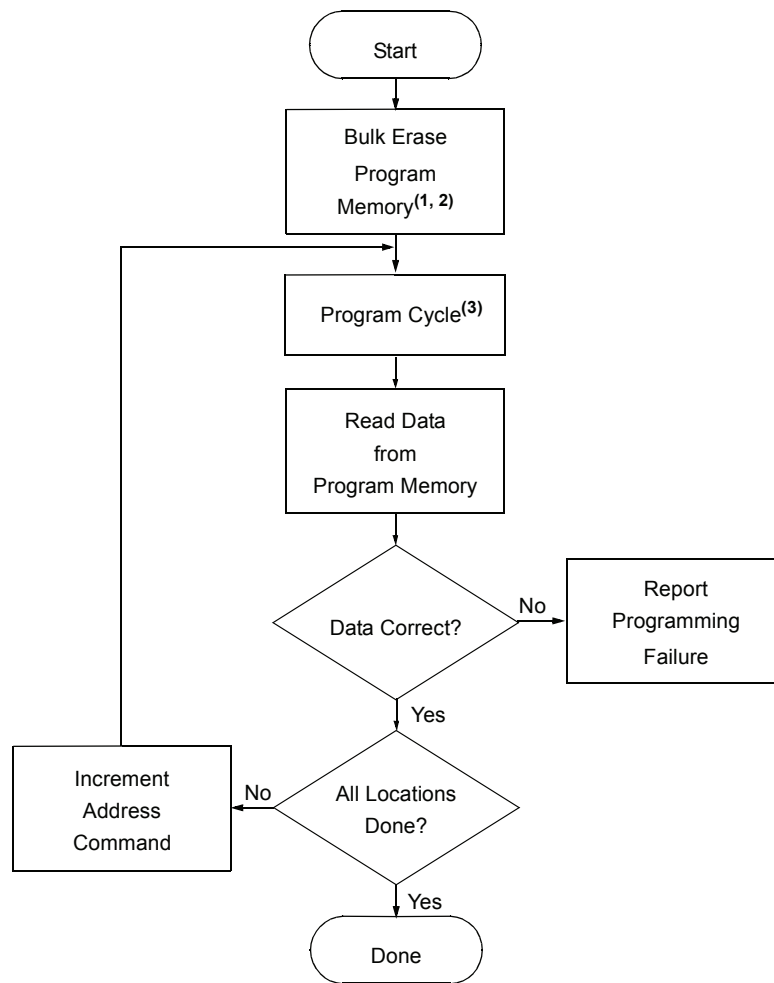
Note 1: This step is optional if device has already been erased or has not been previously programmed.

2: If the device is code-protected or must be completely erased, then Bulk Erase device per Figure 5-6.

3: See Figure 5-3 or Figure 5-4.
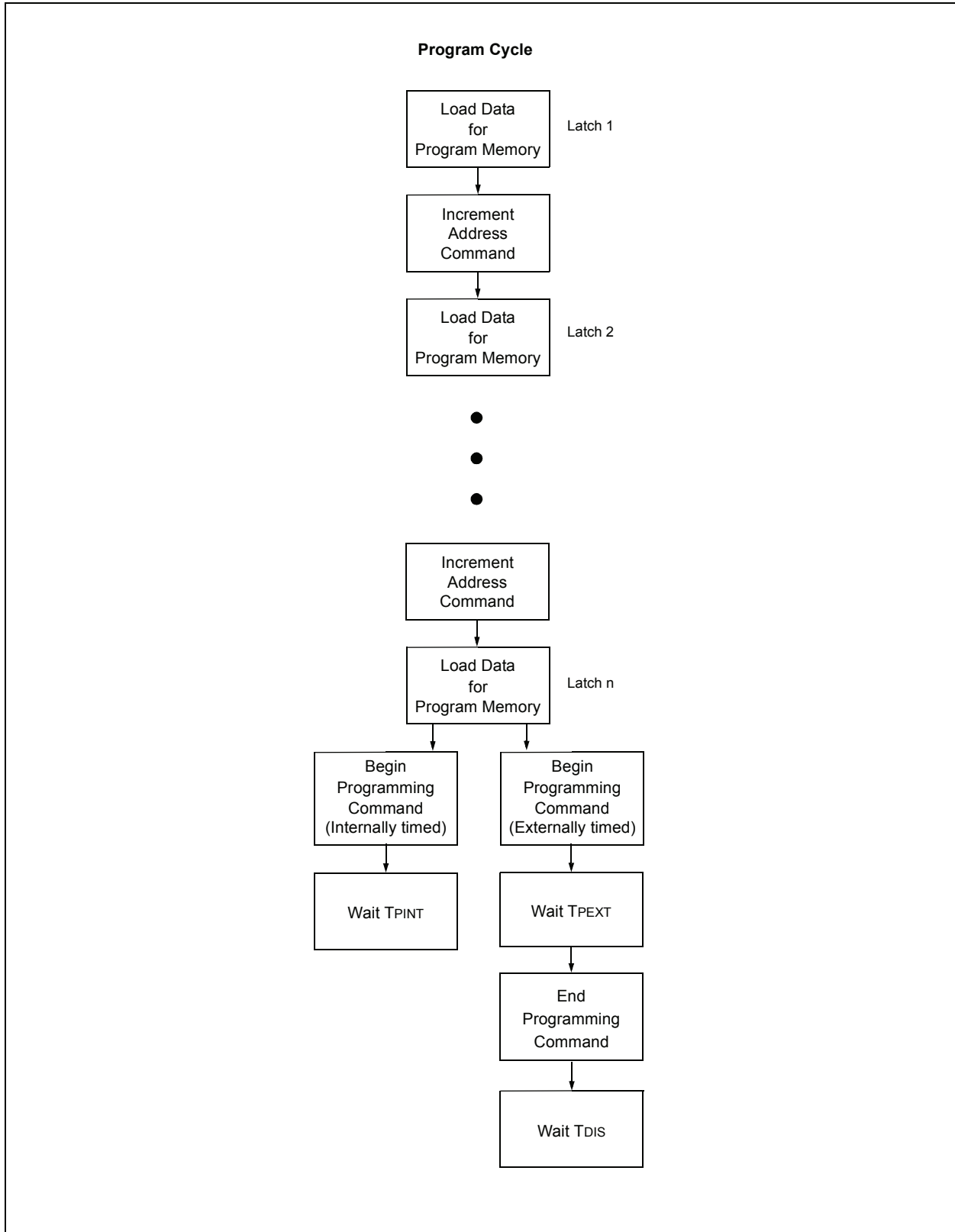
FIGURE 5-4: **MULTIPLE-WORD PROGRAM CYCLE**

Program Cycle

Load Data
for
Program Memory — Latch 1

↓

Increment
Address
Command

↓

Load Data
for
Program Memory — Latch 2

●
●
●

Increment
Address
Command

↓

Load Data
for
Program Memory — Latch n

↓ ↓

Begin
Programming
Command
(Internally timed)

Begin
Programming
Command
(Externally timed)

↓

↓

Wait T_{PINT}

Wait T_{PEXT}

↓

End
Programming
Command

↓

Wait T_{DIS}

FIGURE 5-6: **ERASE FLOWCHART**

Note: This sequence does not erase the Calibration Words.
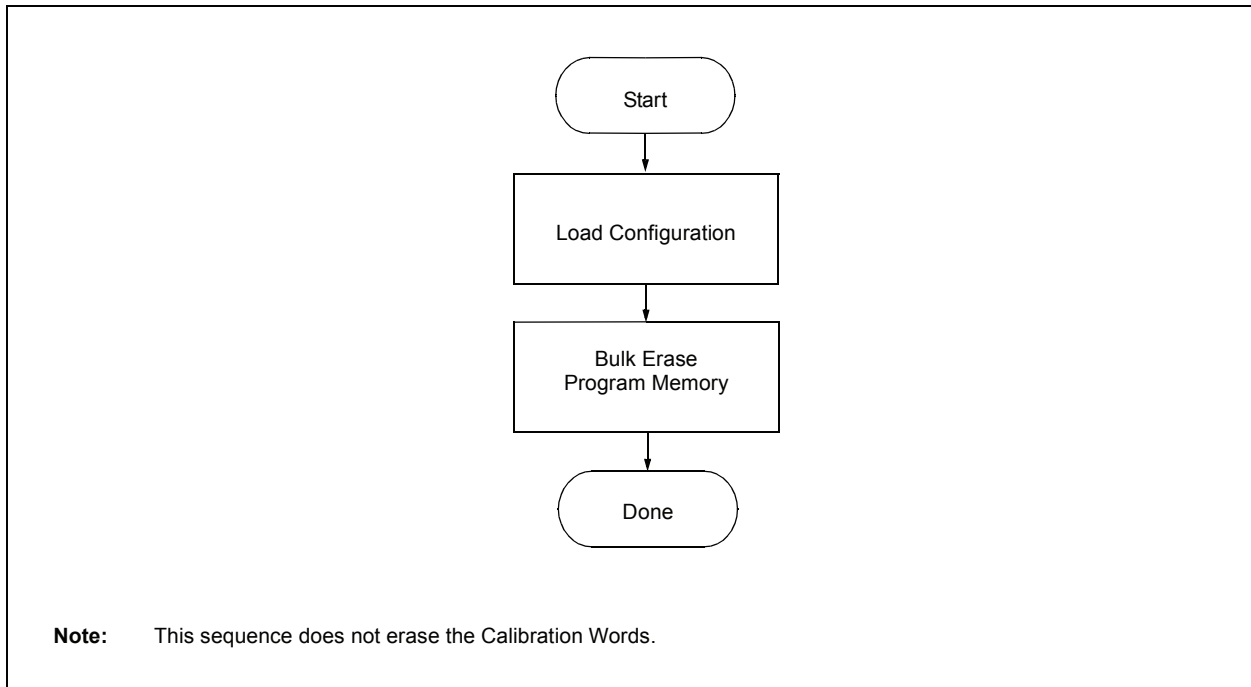
6.0   CODE PROTECTION

Code protection is controlled using the $\overline{CP}$ bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFFh) read as all '0'. Further programming is disabled for the program memory (0000h-7FFFh).

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1   Program Memory

Code protection is enabled by programming the $\overline{CP}$ bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

7.0   HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: Configuration Word 1 is stored at 8007h on the PIC16(L)F151X/152X. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1   Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2   Device ID and Revision

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID (excluding the revision) against the value read from the part. On a mismatch condition the programmer should generate a warning message.

EXAMPLE 7-1: **CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED PIC16F1527, BLANK DEVICE**

PIC16F1527	Sum of Memory addresses 0000h-3FFFh[1]	C000h
	Configuration Word 1[2]	3FFFh
	Configuration Word 1 mask[3]	3EFFh
	Configuration Word 2[2]	3FFFh
	Configuration Word 2 mask[3]	3E13h
	Checksum = C000h + (3FFFh and 3EFFh) + (3FFFh and 3E13h)	
	= C000h + 3EFFh + 3E13h	
	= 3D12h	

Note 1: Sum of memory addresses = (Total number of program memory address locations) x (3FFFh) = C000h, truncated to 16 bits.

   2: Configuration Word 1 and 2 = all bits are '1'; thus, code-protect is disabled.

   3: Configuration Word 1 and 2 Mask = all bits are set to '1', except for unimplemented bits that are '0'.

EXAMPLE 7-2: **CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED PIC16LF1527, 00AAh AT FIRST AND LAST ADDRESS**

PIC16LF1527	Sum of Memory addresses 0000h-3FFFh[1]	4156h
	Configuration Word 1[2]	3FFFh
	Configuration Word 1 mask[3]	3EFFh
	Configuration Word 2[2]	3FFFh
	Configuration Word 2 mask[4]	3E03h
	Checksum = 4156h + (3FFFh and 3EFFh) + (3FFFh and 3E03h)	
	= 4156h + 3EFFh + 3E03h	
	= BE58h	

Note 1: Total number of Program memory address locations: 3FFFh + 1 = 4000h. Then, 4000h - 2 = 3FFEh. Thus, [(3FFEh x 3FFFh) + (2 x 00AAh)] = 4156h, truncated to 16 bits.

   2: Configuration Word 1 and 2 = all bits are '1'; thus, code-protect is disabled.

   3: Configuration Word 1 Mask = all Configuration Word bits are set to '1', except for unimplemented bits that are '0'.

   4: On the PIC16LF1527 device, the $\overline{VCAPEN}$ bit is not implemented in Configuration Word 2; Thus, all unimplemented bits are '0'.

8.0 ELECTRICAL SPECIFICATIONS

Refer to device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
Supply Voltages and Currents						
V_{DD}	Supply Voltage (V_{DDMIN}, V_{DDMAX}) PIC16F151X PIC16F152X	2.3	—	5.5	V	
	PIC16LF151X PIC16LF152X	1.8	—	3.6	V	
V_{PEW}	Read/Write and Row Erase operations	V_{DDMIN}	—	V_{DDMAX}	V	
V_{PBE}	Bulk Erase operations	2.7	—	V_{DDMAX}	V	
I_{DDI}	Current on V_{DD}, Idle	—	—	1.0	mA	
I_{DDP}	Current on V_{DD}, Programming	—	—	3.0	mA	
V_{PP}						
I_{PP}	Current on $\overline{MCLR}$/V_{PP}	—	—	600	µA	
V_{IHH}	High voltage on $\overline{MCLR}$/V_{PP} for Program/Verify mode entry	8.0	—	9.0	V	
T_{VHHR}	$\overline{MCLR}$ rise time (V_{IL} to V_{IHH}) for Program/Verify mode entry	—	—	1.0	µs	
I/O pins						
V_{IH}	(ICSPCLK, ICSPDAT, $\overline{MCLR}$/V_{PP}) input high level	0.8 V_{DD}	—	—	V	
V_{IL}	(ICSPCLK, ICSPDAT, $\overline{MCLR}$/V_{PP}) input low level	—	—	0.2 V_{DD}	V	
V_{OH}	ICSPDAT output high level	V_{DD}-0.7 V_{DD}-0.7 V_{DD}-0.7	—	—	V	I_{OH} = 3.5 mA, V_{DD} = 5V I_{OH} = 3 mA, V_{DD} = 3.3V I_{OH} = 2 mA, V_{DD} = 1.8V
V_{OL}	ICSPDAT output low level	—	—	V_{SS}+0.6 V_{SS}+0.6 V_{SS}+0.6	V	I_{OH} = 8 mA, V_{DD} = 5V I_{OH} = 6 mA, V_{DD} = 3.3V I_{OH} = 3 mA, V_{DD} = 1.8V
Programming Mode Entry and Exit						
T_{ENTS}	Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before V_{DD} or $\overline{MCLR}$↑	100	—	—	ns	
T_{ENTH}	Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after V_{DD} or $\overline{MCLR}$↑	250	—	—	µs	
Serial Program/Verify						
T_{CKL}	Clock Low Pulse Width	100	—	—	ns	
T_{CKH}	Clock High Pulse Width	100	—	—	ns	
T_{DS}	Data in setup time before clock↓	100	—	—	ns	
T_{DH}	Data in hold time after clock↓	100	—	—	ns	
T_{CO}	Clock↑ to data out valid (during a Read Data command)	0	—	80	ns	
T_{LZD}	Clock↓ to data low-impedance (during a Read Data command)	0	—	80	ns	
T_{HZD}	Clock↓ to data high-impedance (during a Read Data command)	0	—	80	ns	
T_{DLY}	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	—	—	µs	
T_{ERAB}	Bulk Erase cycle time	—	—	5	ms	
T_{ERAR}	Row Erase cycle time	—	—	2.5	ms	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

APPENDIX A: REVISION HISTORY

Revision A (08/2010)

Original release of this document.

Revision B (09/2011)

Added PIC16(L)F1512/1513 devices; Added new Figures 3-1 and 3-2; Updated Registers 3-1, 3-2 and 3-3 to new format; Updated Register 3-3 to add 2 kW and 4 kW Flash memory; Added Notes to Examples 7-1 to 7-4; Updated Table 8-1; Other minor corrections.

NOTES:

Advance Information

Note the following details of the code protection feature on Microchip devices:

• Microchip products meet the specification contained in their particular Microchip Data Sheet.

• Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

• There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

• Microchip is willing to work with the customer who is concerned about the integrity of their code.

• Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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