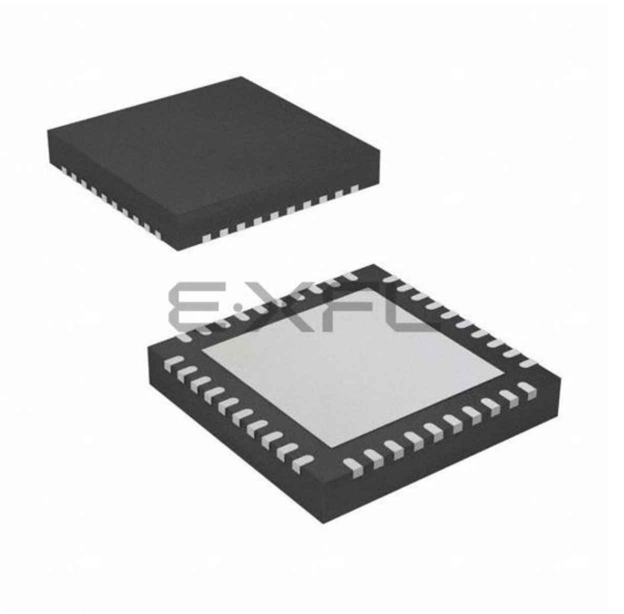


Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1519-e-mv

2.0 DEVICE PINOUTS

The pin diagrams for the PIC16(L)F151X/152X family are shown in Figure 2-1 through Figure 2-7. The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagrams.

FIGURE 2-1: 28-PIN SPDIP, SOIC, SSOP DIAGRAM FOR PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516 AND PIC16(L)F1518

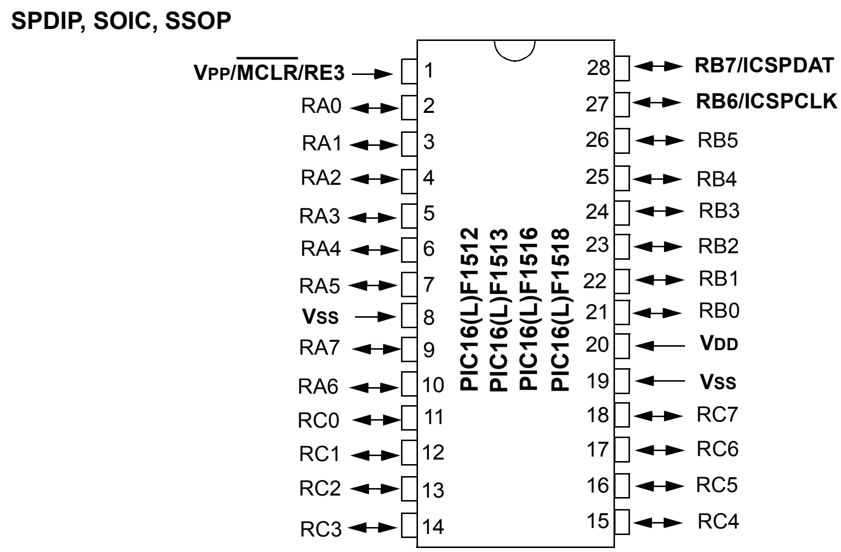


FIGURE 2-3: 40-PIN PDIP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519

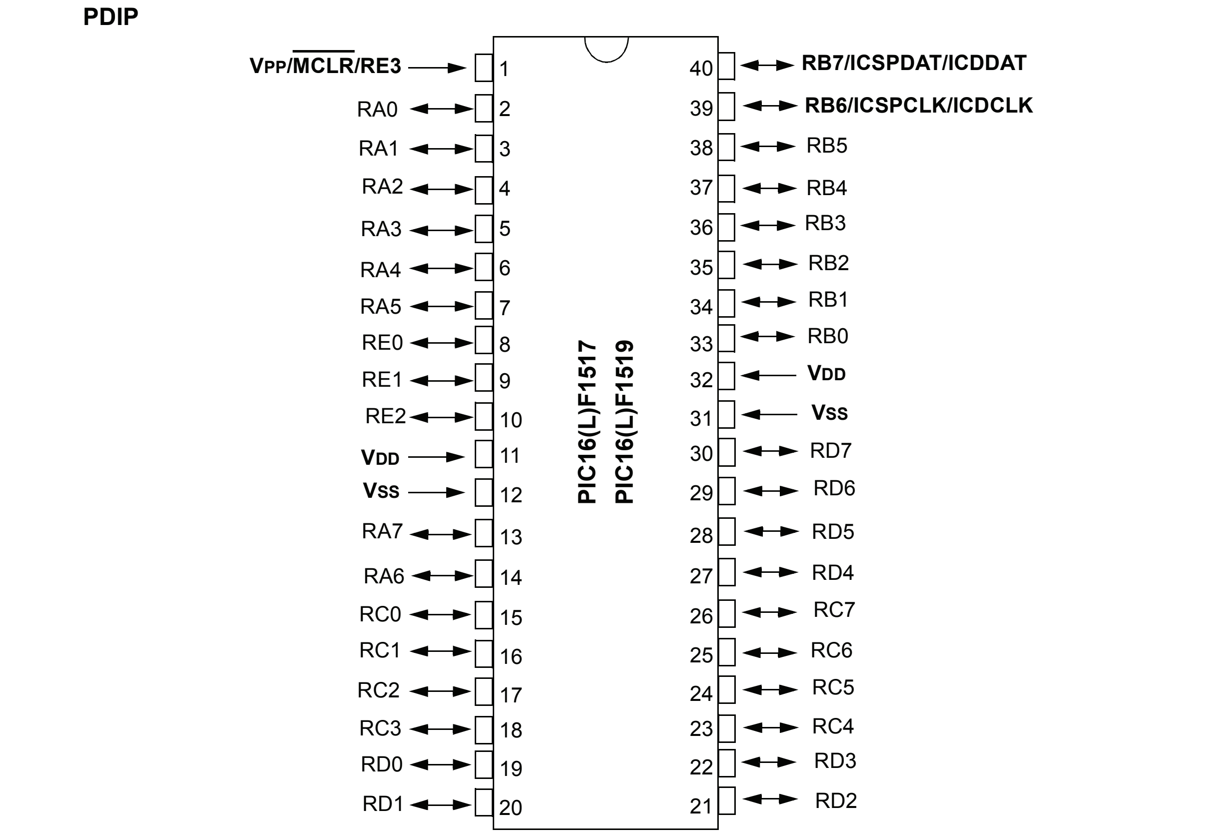


FIGURE 2-4: 40-PIN UQFN DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519

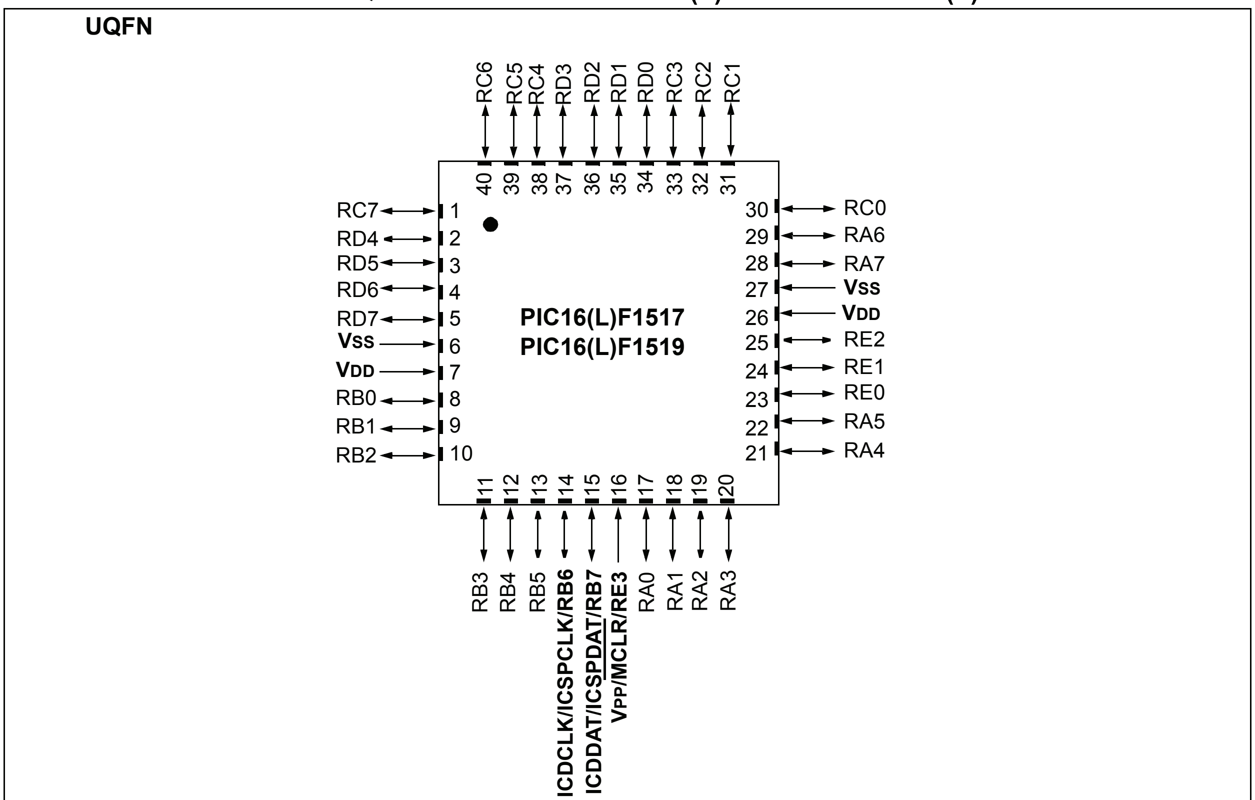


FIGURE 2-5: 44-PIN TQFP DIAGRAM FOR PIC16(L)F1517 AND PIC16(L)F1519

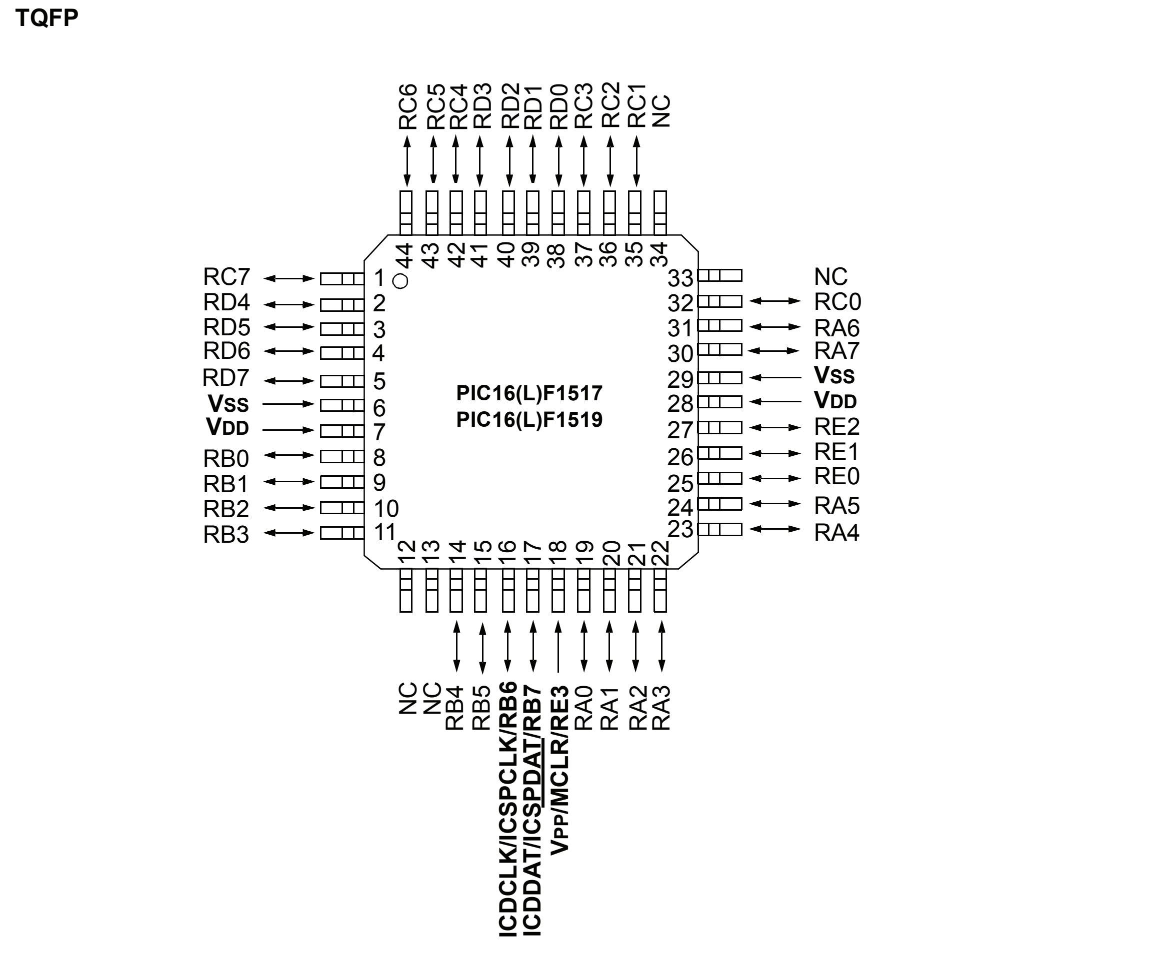


FIGURE 2-6: 64-PIN QFN DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527

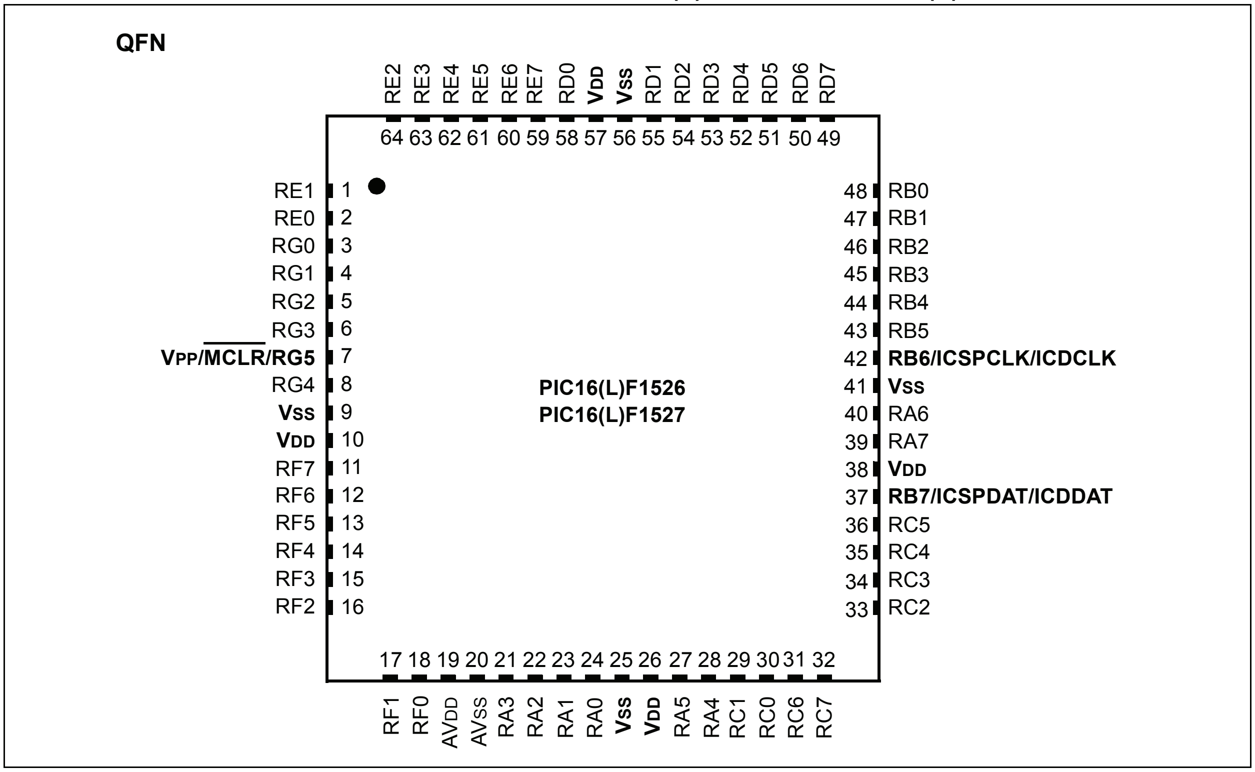


FIGURE 2-7: 64-PIN TQFP DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527

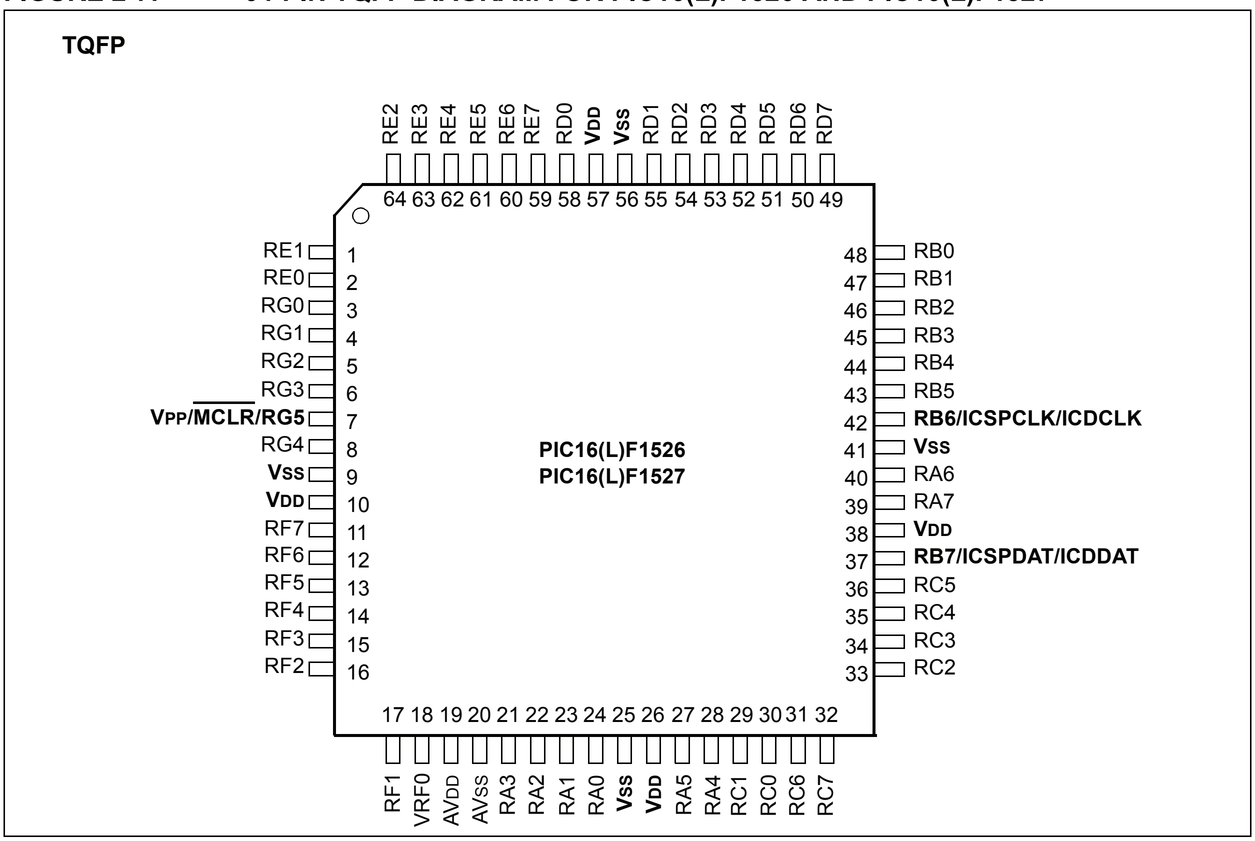


FIGURE 3-2: PIC16(L)F1513 PROGRAM MEMORY MAPPING

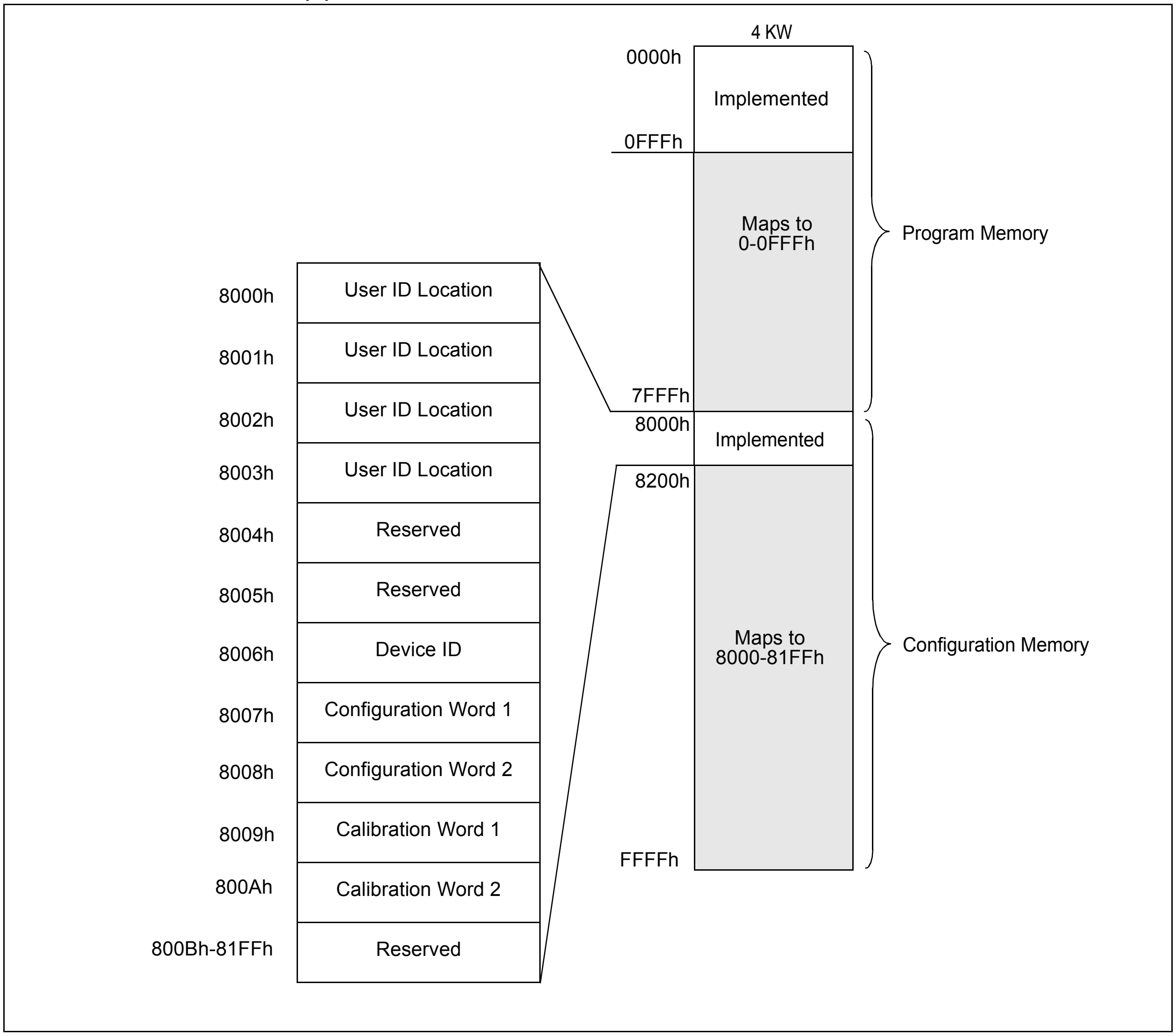


FIGURE 3-4: PIC16(L)F1527, PIC16(L)F1518 AND PIC16(L)F1519 PROGRAM MEMORY MAPPING

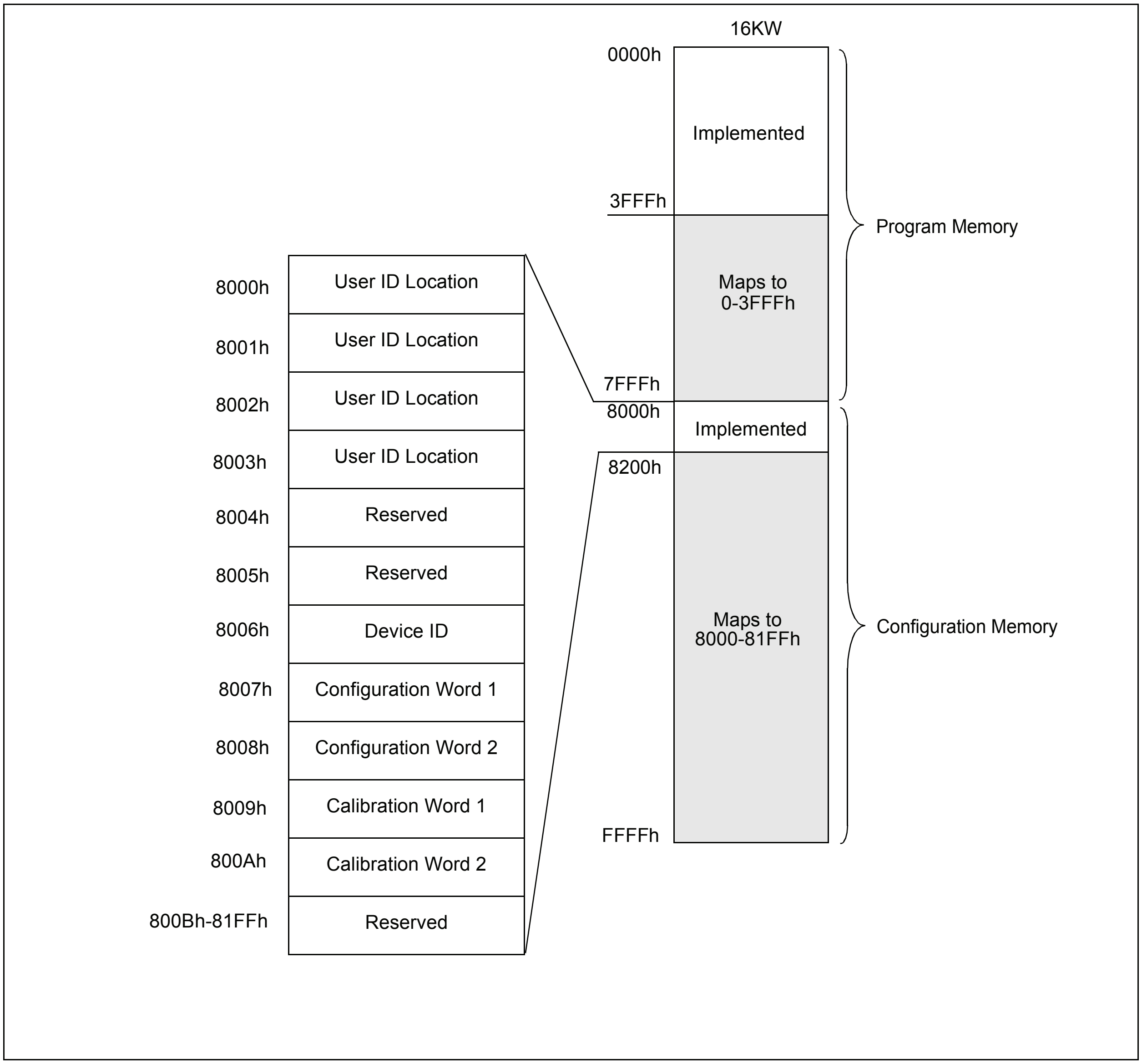


TABLE 3-1: DEVICE ID VALUES

DEVICE	DEVICE ID VALUES	
	DEV	REV
PIC16F1527	0001 0101 101	x xxxx
PIC16F1526	0001 0101 100	x xxxx
PIC16LF1527	0001 0101 111	x xxxx
PIC16LF1526	0001 0101 110	x xxxx
PIC16F1519	0001 0110 111	x xxxx
PIC16F1518	0001 0110 110	x xxxx
PIC16F1517	0001 0110 101	x xxxx
PIC16F1516	0001 0110 100	x xxxx
PIC16F1513	0001 0110 010	x xxxx
PIC16F1512	0001 0111 000	x xxxx
PIC16LF1519	0001 0111 111	x xxxx
PIC16LF1518	0001 0111 110	x xxxx
PIC16LF1517	0001 0111 101	x xxxx
PIC16LF1516	0001 0111 100	x xxxx
PIC16LF1513	0001 0111 010	x xxxx
PIC16LF1512	0001 0111 001	x xxxx

3.3 Configuration Words

There are two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

The internal calibration values are factory calibrated and stored in Calibration Words 1 and 2 (8009h, 800Ah).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

REGISTER 3-2: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘1
‘0’ = Bit is cleared	‘1’ = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 12 **IESO:** Internal External Switchover bit
1 = Internal/External Switchover mode is enabled
0 = Internal/External Switchover mode is disabled

bit 11 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
0 = CLKOUT function is enabled on CLKOUT pin

bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits(1)
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the PCON register
00 = BOR disabled

bit 8 **Unimplemented:** Read as ‘1’

bit 7 **$\overline{\text{CP}}$:** Code Protection bit(2)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6 **MCLRE:** $\overline{\text{MCLR}}$/VPP Pin Function Select bit
If LVP bit = 1:
This bit is ignored.
If LVP bit = 0:
1 = $\overline{\text{MCLR}}$/VPP pin function is $\overline{\text{MCLR}}$; Weak pull-up enabled.
0 = $\overline{\text{MCLR}}$/VPP pin function is digital input; $\overline{\text{MCLR}}$ internally disabled; Weak pull-up under control of WPUA register.

bit 5 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
11 = WDT enabled
10 = WDT enabled while running and disabled in Sleep
01 = WDT controlled by the SWDTEN bit in the WDTCON register
00 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = ECH: External Clock, High-Power mode: on CLKIN pin
110 = ECM: External Clock, Medium-Power mode: on CLKIN pin
101 = ECL: External Clock, Low-Power mode: on CLKIN pin
100 = INTOSC oscillator: I/O function on OSC1 pin
011 = EXTRC oscillator: RC function on OSC1 pin
010 = HS oscillator: High-speed crystal/resonator on OSC2 pin and OSC1 pin
001 = XT oscillator: Crystal/resonator on OSC2 pin and OSC1 pin
000 = LP oscillator: Low-power crystal on OSC2 pin and OSC1 pin

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire program memory will be erased when the code protection is turned off.

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to VIHH.
3. Raise the voltage on VDD FROM 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when Configuration Word 1 has $\overline{\text{MCLR}}$ disabled (MCLRE = 0), the power-up time is disabled ($\overline{\text{PWRTE}}$ = 0), the internal oscillator is selected (FOSC = 100), and ICSPCLK and ICSPDAT pins are driven by the user application, the device will execute code. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in Figure 8-2.

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from VDD or below to VIHH.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-1.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower (VIL). See Figures 8-3 and 8-4.

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the PIC16(L)F151X/152X devices to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 8-8 and Figure 8-9.

Exiting Program/Verify mode is done by no longer driving $\overline{\text{MCLR}}$ to VIL. See Figure 8-8 and Figure 8-9.

Note:	To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

4.3.10 ROW ERASE PROGRAM MEMORY

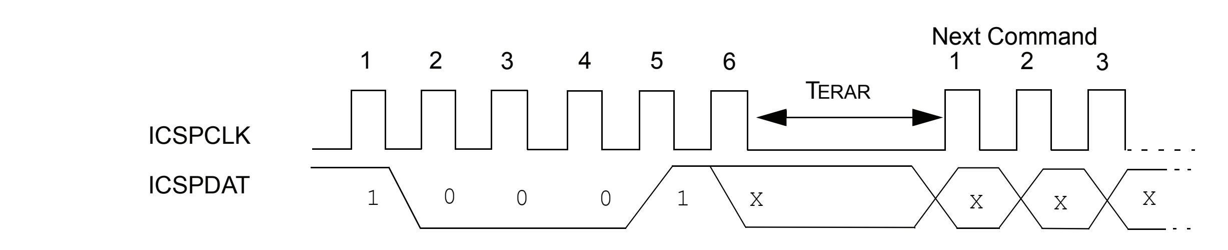
The Row Erase Program Memory command will erase an individual row. Refer to Table 4-2 for row sizes of specific devices and the PC bits used to address them. If the program memory is code-protected the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h the Row Erase Program Memory command will only erase the user ID locations regardless of the setting of the $\overline{CP}$ Configuration bit.

After receiving the Row Erase Program Memory command the erase will not complete until the time interval, TERAR, has expired.

TABLE 4-2: PROGRAMMING ROW SIZE AND LATCHES

Devices	PC	Row Size	Number of Latches
PIC16(L)F151X/152X	<15:5>	32	32

FIGURE 4-10: ROW ERASE PROGRAM MEMORY



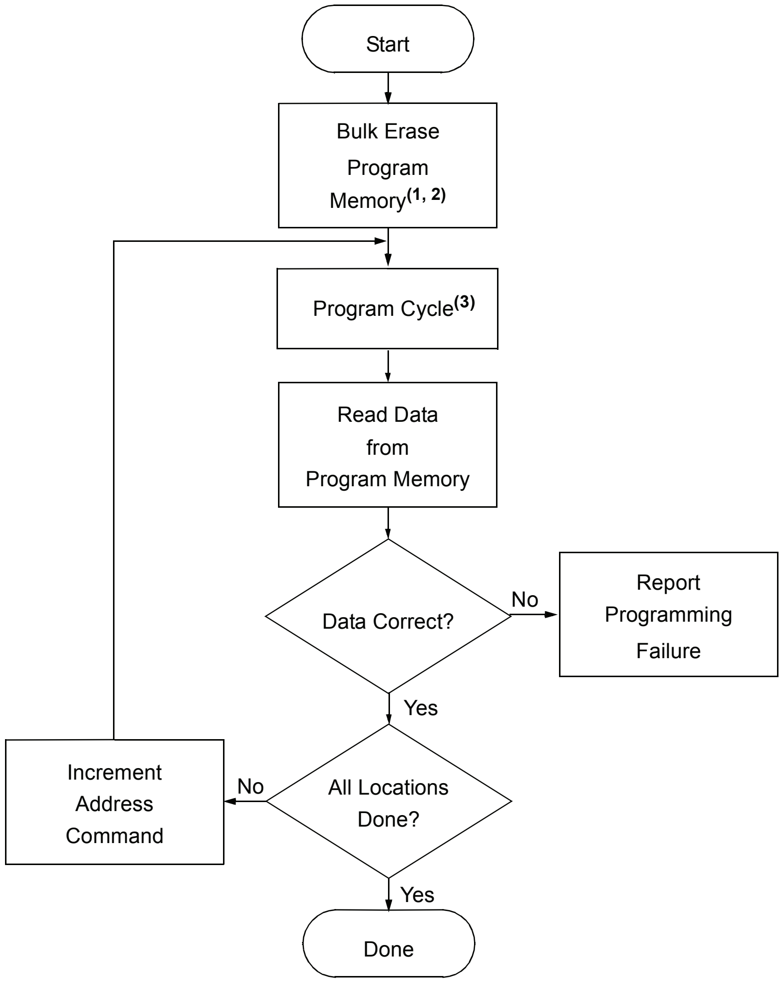
5.0 PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to Table 4-2 for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC's address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes cannot cross the physical boundary. For example, with the PIC16F1527, attempting to write from address 0002h-0009h will result in data being written to 0008h-000Fh.

If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

FIGURE 5-2: PROGRAM MEMORY FLOWCHART

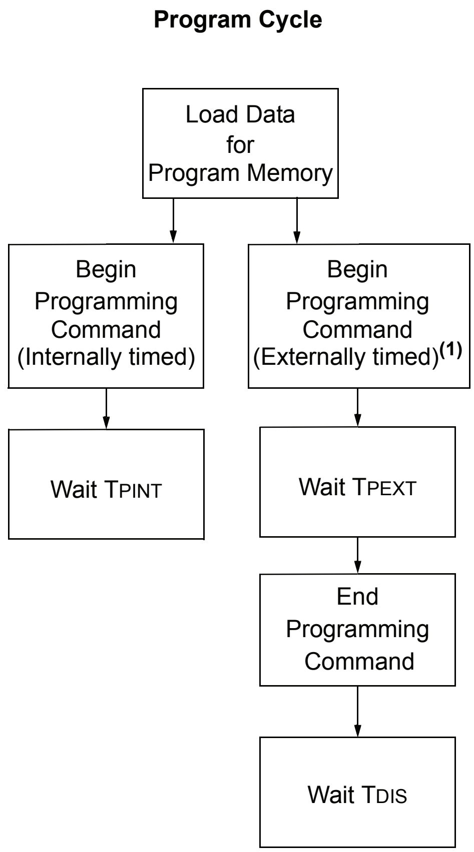


Note 1: This step is optional if device has already been erased or has not been previously programmed.

2: If the device is code-protected or must be completely erased, then Bulk Erase device per Figure 5-6.

3: See Figure 5-3 or Figure 5-4.

FIGURE 5-3: ONE-WORD PROGRAM CYCLE



Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

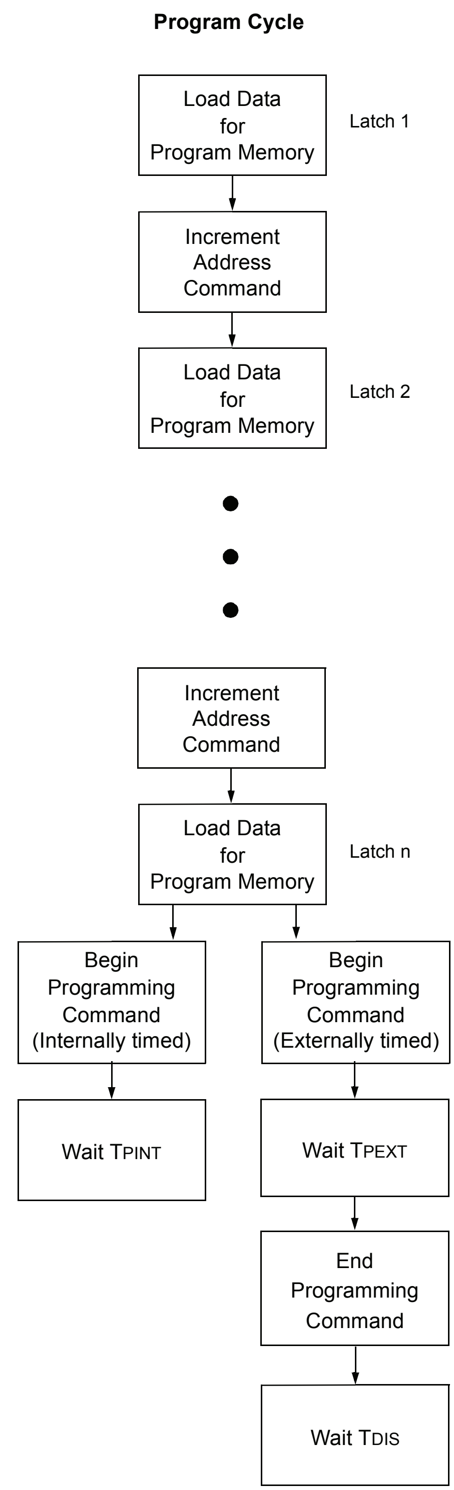
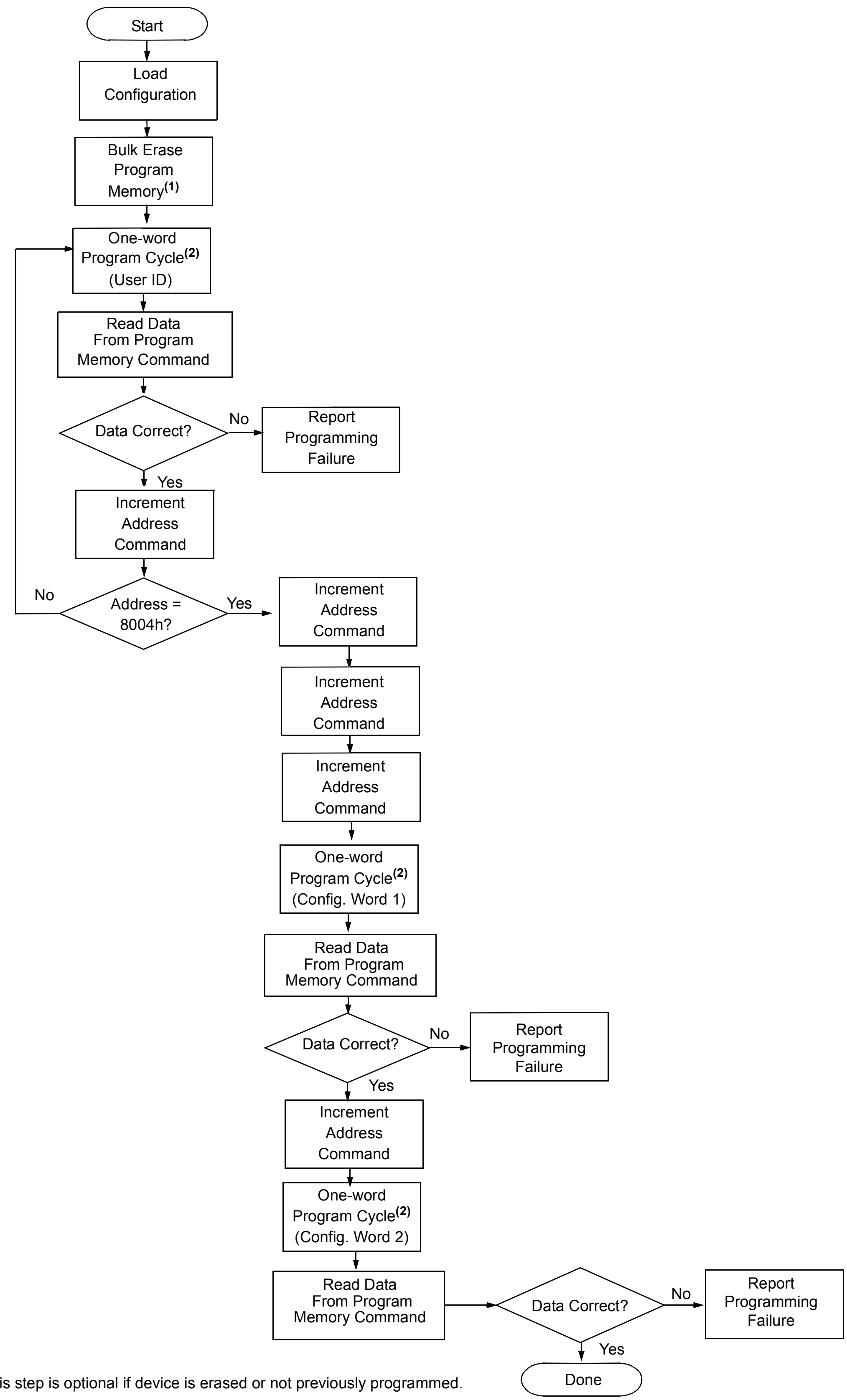


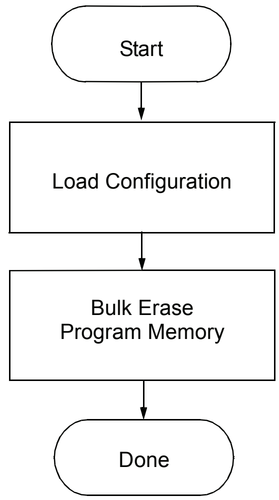
FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART



Note 1: This step is optional if device is erased or not previously programmed.

2: See Figure 5-3.

FIGURE 5-6: ERASE FLOWCHART



Note: This sequence does not erase the Calibration Words.

EXAMPLE 7-1: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED PIC16F1527, BLANK DEVICE

PIC16F1527	Sum of Memory addresses 0000h-3FFFh(1)		C000h
	Configuration Word 1(2)		3FFFh
	Configuration Word 1 mask(3)		3EFFh
	Configuration Word 2(2)		3FFFh
	Configuration Word 2 mask(3)		3E13h
	Checksum	= C000h + (3FFFh and 3EFFh) + (3FFFh and 3E13h)	
		= C000h + 3EFFh + 3E13h	
		= 3D12h	

Note 1: Sum of memory addresses = (Total number of program memory address locations) x (3FFFh) = C000h, truncated to 16 bits.
2: Configuration Word 1 and 2 = all bits are '1'; thus, code-protect is disabled.
3: Configuration Word 1 and 2 Mask = all bits are set to '1', except for unimplemented bits that are '0'.

EXAMPLE 7-2: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED PIC16LF1527, 00AAh AT FIRST AND LAST ADDRESS

PIC16LF1527	Sum of Memory addresses 0000h-3FFFh(1)		4156h
	Configuration Word 1(2)		3FFFh
	Configuration Word 1 mask(3)		3EFFh
	Configuration Word 2(2)		3FFFh
	Configuration Word 2 mask(4)		3E03h
	Checksum	= 4156h + (3FFFh and 3EFFh) + (3FFFh and 3E03h)	
		= 4156h + 3EFFh + 3E03h	
		= BE58h	

Note 1: Total number of Program memory address locations: 3FFFh + 1 = 4000h. Then, 4000h - 2 = 3FFEh. Thus, [(3FFEh x 3FFFh) + (2 x 00AAh)] = 4156h, truncated to 16 bits.
2: Configuration Word 1 and 2 = all bits are '1'; thus, code-protect is disabled.
3: Configuration Word 1 Mask = all Configuration Word bits are set to '1', except for unimplemented bits that are '0'.
4: On the PIC16LF1527 device, the $\overline{\text{VCAPEN}}$ bit is not implemented in Configuration Word 2; Thus, all unimplemented bits are '0'.

EXAMPLE 7-4: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC16LF1527, 00AAh AT FIRST AND LAST ADDRESS

PIC16LF1527	Configuration Word 1(2)	3F7Fh
	Configuration Word 1 mask(3)	3EFFh
	Configuration Word 2(2)	3FFFh
	Configuration Word 2 mask(3), (5)	3E03h
	User ID (8000h)(1)	000Eh
	User ID (8001h)(1)	0008h
	User ID (8002h)(1)	0005h
	User ID (8003h)(1)	0008h

Sum of User IDs(4) = (000Eh and 000Fh) << 12 + (0008h and 000Fh) << 8 + (0005h and 000Fh) << 4 + (0008h and 000Fh)
= E000h + 0800h + 0050h + 0008h
= E858h

Checksum = (3F7Fh and 3EFFh) + (3FFFh and 3E03h) + Sum of User IDs
= 3E7Fh +3E03h + E858h
= 64DAh

Note 1: User ID values in this example are random values.

2: Configuration Word 1 and 2 = all bits are ‘1’ except the code-protect enable bit.

3: Configuration Word 1 and 2 Mask = all Configuration Word bits are set to ‘1’, except for unimplemented bits which read ‘0’.

4: << = shift left, thus the LSb of the first user ID value is the MSb of the sum of user IDs and so on, until the LSb of the last user ID value becomes the LSb of the sum of user IDs.

5: On the PIC16LF1527 device, the $\overline{\text{VCAPEN}}$ bit is not implemented in Configuration Word 2; thus, all unimplemented bits are ‘0’.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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