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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

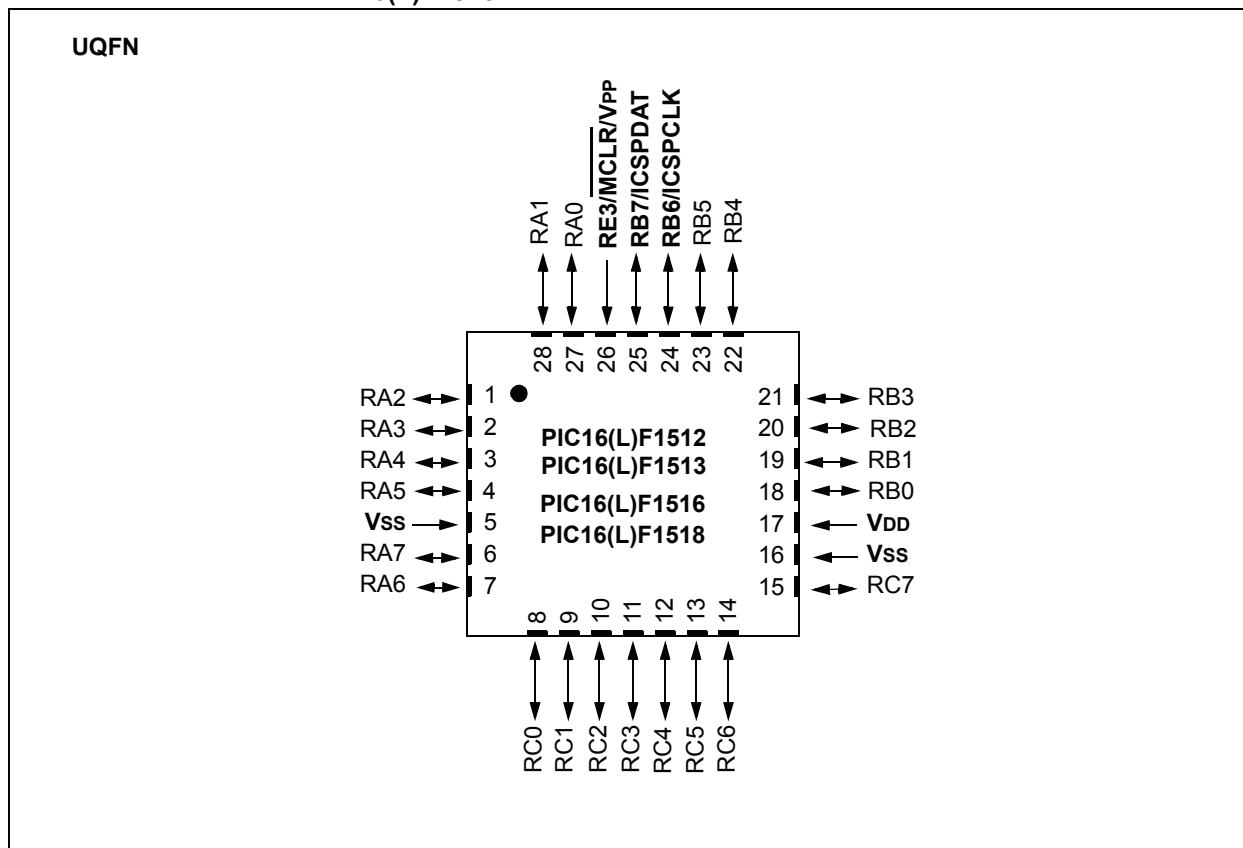
Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I ² C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 36 |
| Program Memory Size | 28KB (16K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 5.5V |
| Data Converters | A/D 28x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 40-UFQFN Exposed Pad |
| Supplier Device Package | 40-UQFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f1519t-i-mv |

PIC16(L)F151X/152X

FIGURE 2-2: 28-PIN UQFN DIAGRAM FOR PIC16(L)F1512, PIC16(L)F1513, PIC16(L)F1516 AND PIC16(L)F1518



PIC16(L)F151X/152X

FIGURE 2-6: 64-PIN QFN DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527

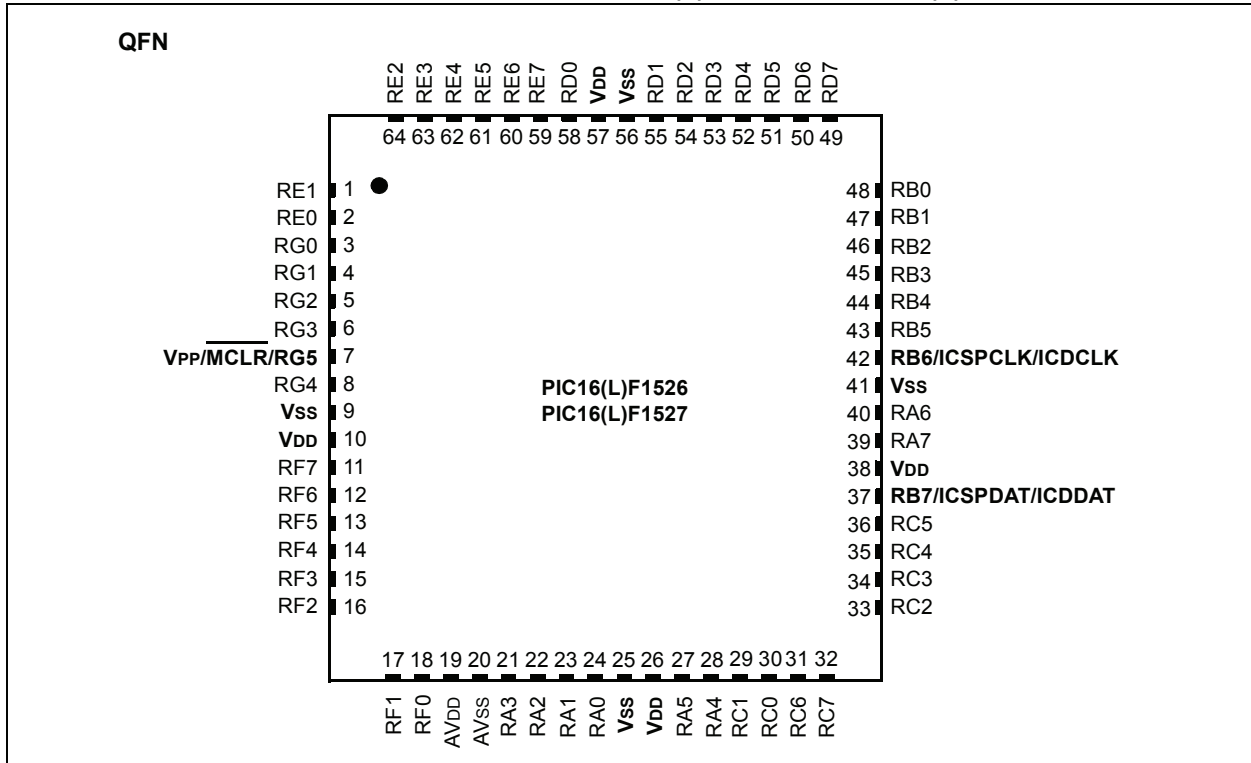
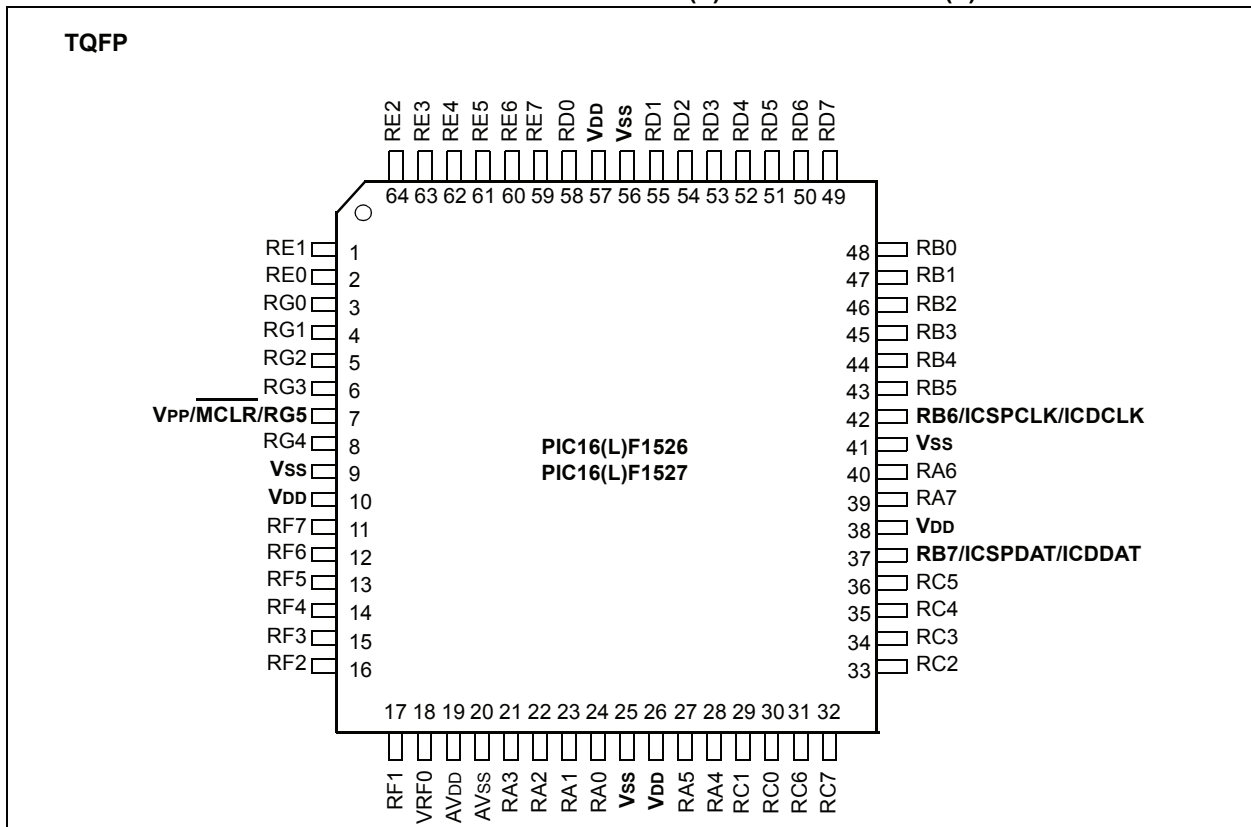


FIGURE 2-7: 64-PIN TQFP DIAGRAM FOR PIC16(L)F1526 AND PIC16(L)F1527



PIC16(L)F151X/152X

3.0 MEMORY MAP

The memory for the PIC16(L)F151X/152X devices is broken into two sections: program memory and configuration memory. Only the size of the program memory changes between devices, the configuration memory remains the same.

FIGURE 3-1: PIC16(L)F1512 PROGRAM MEMORY MAPPING

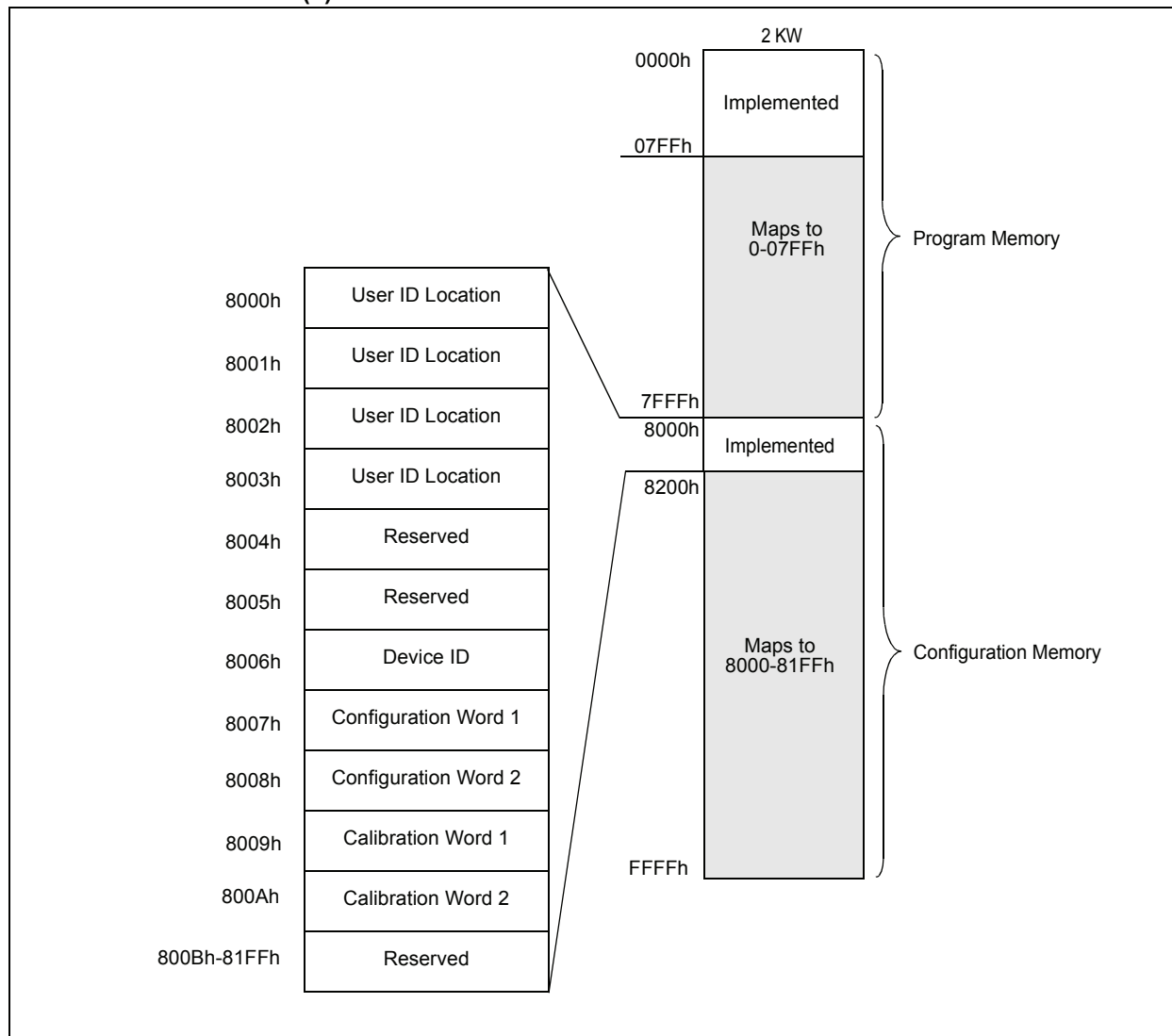
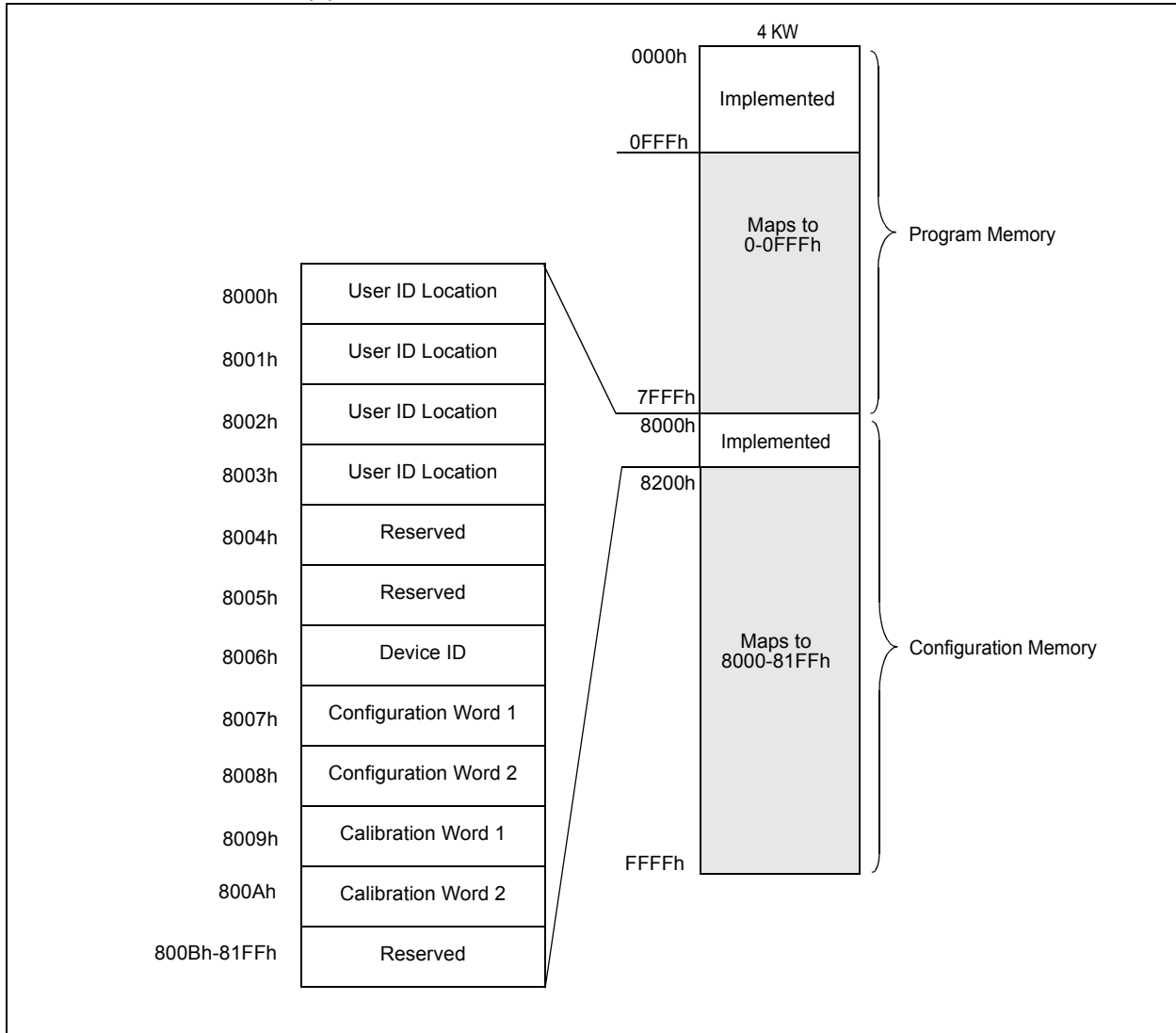


FIGURE 3-2: PIC16(L)F1513 PROGRAM MEMORY MAPPING



PIC16(L)F151X/152X

FIGURE 3-3: PIC16(L)F1526, PIC16(L)F1516 AND PIC16(L)F1517 PROGRAM MEMORY MAPPING

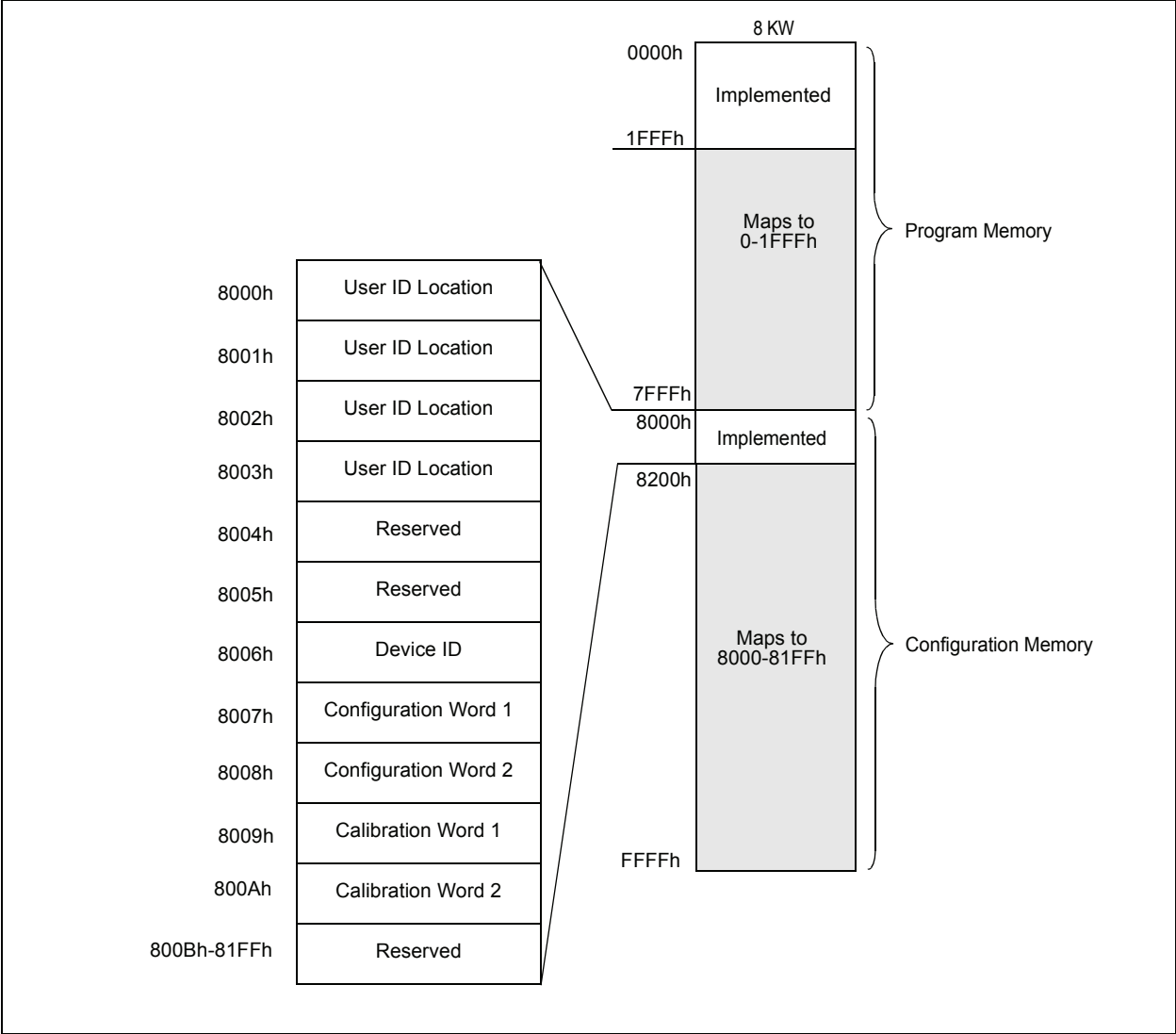


TABLE 3-1: DEVICE ID VALUES

| DEVICE | DEVICE ID VALUES | |
|-------------|------------------|--------|
| | DEV | REV |
| PIC16F1527 | 0001 0101 101 | x xxxx |
| PIC16F1526 | 0001 0101 100 | x xxxx |
| PIC16LF1527 | 0001 0101 111 | x xxxx |
| PIC16LF1526 | 0001 0101 110 | x xxxx |
| PIC16F1519 | 0001 0110 111 | x xxxx |
| PIC16F1518 | 0001 0110 110 | x xxxx |
| PIC16F1517 | 0001 0110 101 | x xxxx |
| PIC16F1516 | 0001 0110 100 | x xxxx |
| PIC16F1513 | 0001 0110 010 | x xxxx |
| PIC16F1512 | 0001 0111 000 | x xxxx |
| PIC16LF1519 | 0001 0111 111 | x xxxx |
| PIC16LF1518 | 0001 0111 110 | x xxxx |
| PIC16LF1517 | 0001 0111 101 | x xxxx |
| PIC16LF1516 | 0001 0111 100 | x xxxx |
| PIC16LF1513 | 0001 0111 010 | x xxxx |
| PIC16LF1512 | 0001 0111 001 | x xxxx |

3.3 Configuration Words

There are two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

The internal calibration values are factory calibrated and stored in Calibration Words 1 and 2 (8009h, 800Ah).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

PIC16(L)F151X/152X

REGISTER 3-2: CONFIGURATION WORD 1

| R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | U-1 |
|--------|-------|----------|------------|-------|-------|
| FCMEN | IESO | CLKOUTEN | BOREN<1:0> | — | |
| bit 13 | | | | | bit 8 |

| R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 |
|-------|-------|-------|-----------|-----------|-------|-------|-------|
| CP | MCLRE | PWRTÉ | WDTE<1:0> | FOSC<2:0> | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '1'
 '0' = Bit is cleared '1' = Bit is set -n = Value when blank or after Bulk Erase

- bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
 1 = Fail-Safe Clock Monitor is enabled
 0 = Fail-Safe Clock Monitor is disabled
- bit 12 **IESO:** Internal External Switchover bit
 1 = Internal/External Switchover mode is enabled
 0 = Internal/External Switchover mode is disabled
- bit 11 **CLKOUTEN:** Clock Out Enable bit
 1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
 0 = CLKOUT function is enabled on CLKOUT pin
- bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits⁽¹⁾
 11 = BOR enabled
 10 = BOR enabled during operation and disabled in Sleep
 01 = BOR controlled by SBOREN bit of the PCON register
 00 = BOR disabled
- bit 8 **Unimplemented:** Read as '1'
- bit 7 **CP:** Code Protection bit⁽²⁾
 1 = Program memory code protection is disabled
 0 = Program memory code protection is enabled
- bit 6 **MCLRE:** MCLR/VPP Pin Function Select bit
 If LVP bit = 1:
 This bit is ignored.
 If LVP bit = 0:
 1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
 0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUA register.
- bit 5 **PWRTÉ:** Power-up Timer Enable bit⁽¹⁾
 1 = PWRT disabled
 0 = PWRT enabled
- bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
 11 = WDT enabled
 10 = WDT enabled while running and disabled in Sleep
 01 = WDT controlled by the SWDTEN bit in the WDTCON register
 00 = WDT disabled
- bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
 111 = ECH: External Clock, High-Power mode: on CLKIN pin
 110 = ECM: External Clock, Medium-Power mode: on CLKIN pin
 101 = ECL: External Clock, Low-Power mode: on CLKIN pin
 100 = INTOSC oscillator: I/O function on OSC1 pin
 011 = EXTRC oscillator: RC function on OSC1 pin
 010 = HS oscillator: High-speed crystal/resonator on OSC2 pin and OSC1 pin
 001 = XT oscillator: Crystal/resonator on OSC2 pin and OSC1 pin
 000 = LP oscillator: Low-power crystal on OSC2 pin and OSC1 pin

- Note** 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
 2: The entire program memory will be erased when the code protection is turned off.

PIC16(L)F151X/152X

REGISTER 3-3: CONFIGURATION WORD 2

| | | | | | |
|--------|-------|-------|-------|--------|-------|
| R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | U-1 |
| LVP | DEBUG | LPBOR | BORV | STVREN | — |
| bit 13 | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----------------------|-----|-----|----------|-------|
| U-1 | U-1 | U-1 | R/P-1 | U-1 | U-1 | R/P-1 | R/P-1 |
| — | — | — | VCAPEN ⁽²⁾ | — | — | WRT<1:0> | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '1'

'0' = Bit is cleared

'1' = Bit is set

-n = Value when blank or after Bulk Erase

- bit 13 **LVP:** Low-Voltage Programming Enable bit⁽¹⁾
 1 = Low-voltage programming enabled
 0 = HV on MCLR/VPP must be used for programming
- bit 12 **DEBUG:** In-Circuit Debugger Mode bit
 1 = In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
 0 = In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger
- bit 11 **LPBOR:** Low-Power BOR
 1 = Low-Power BOR is disabled
 0 = Low-Power BOR is enabled
- bit 10 **BORV:** Brown-out Reset Voltage Selection bit
 1 = Brown-out Reset voltage (VBOR), low trip point selected
 0 = Brown-out Reset voltage (VBOR), high trip point selected
- bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
 1 = Stack Overflow or Underflow will cause a Reset
 0 = Stack Overflow or Underflow will not cause a Reset
- bit 8-5 **Unimplemented:** Read as '1'
- bit 4 **VCAPEN:** Voltage Regulator Capacitor Enable bits⁽¹⁾
 0 = VCAP functionality is enabled on VCAP pin
 1 = All VCAP pin functions are disabled
- bit 3-2 **Unimplemented:** Read as '1'
- bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits
2 kW Flash memory (PIC16(L)F1512):
 11 = Write protection off
 10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
 01 = 000h to FFFh write-protected, 400h to 7FFh may be modified by PMCON control
 00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control
4 kW Flash memory (PIC16(L)F1513):
 11 = Write protection off
 10 = 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control
 01 = 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control
 00 = 000h to FFFh write-protected, no addresses may be modified by PMCON control
8 kW Flash memory (PIC16F/LF1516/1517/1526):
 11 = Write protection off
 10 = 000h to 1FFh write-protected, 200h to 1FFFh may be modified by PMCON control
 01 = 000h to FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control
 00 = 000h to 1FFFh write-protected, no addresses may be modified by PMCON control
16 kW Flash memory (PIC16F/LF1518/1519/1527):
 11 = Write protection off
 10 = 000h to 1FFh write-protected, 200h to 3FFFh may be modified by PMCON control
 01 = 000h to 1FFFh write-protected, 2000h to 3FFFh may be modified by PMCON control
 00 = 000h to 3FFFh write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.

Note 2: Applies to PIC16F151X/152X devices only. On PIC16LF151X/152X, the VCAPEN bit is unimplemented.

4.3 Program/Verify Commands

The PIC16(L)F151X/152X implements 10 programming commands; each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING

| Command | Mapping | | Data/Note |
|------------------------------------|----------------------|-----|------------------|
| | Binary (MSb ... LSb) | Hex | |
| Load Configuration | x 0 0 0 0 0 | 00h | 0, data (14), 0 |
| Load Data For Program Memory | x 0 0 0 1 0 | 02h | 0, data (14), 0 |
| Read Data From Program Memory | x 0 0 1 0 0 | 04h | 0, data (14), 0 |
| Increment Address | x 0 0 1 1 0 | 06h | — |
| Reset Address | x 1 0 1 1 0 | 16h | — |
| Begin Internally Timed Programming | x 0 1 0 0 0 | 08h | — |
| Begin Externally Timed Programming | x 1 1 0 0 0 | 18h | — |
| End Externally Timed Programming | x 0 1 0 1 0 | 0Ah | — |
| Bulk Erase Program Memory | x 0 1 0 0 1 | 09h | Internally Timed |
| Row Erase Program Memory | x 1 0 0 0 1 | 11h | Internally Timed |

4.3.1 LOAD CONFIGURATION

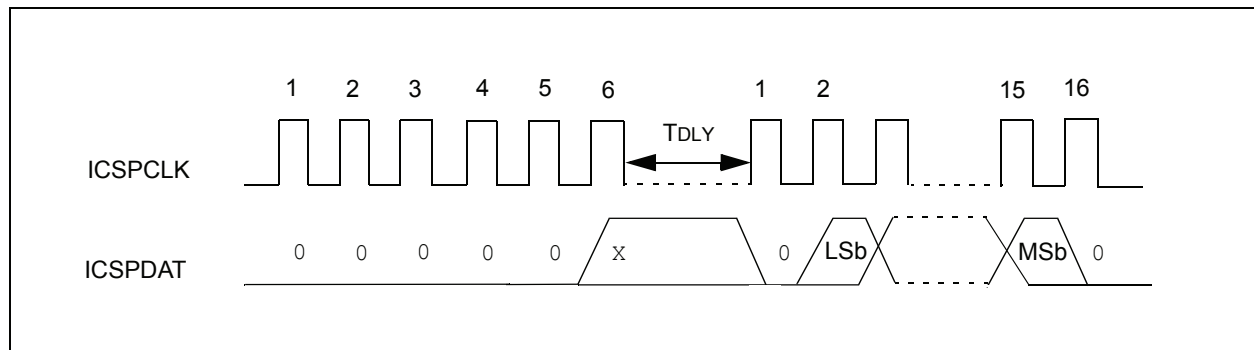
The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

Note: Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

FIGURE 4-1: LOAD CONFIGURATION

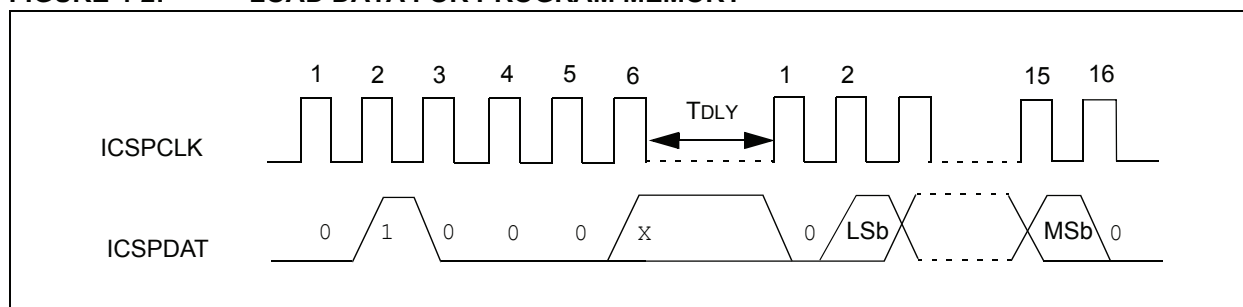


PIC16(L)F151X/152X

4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

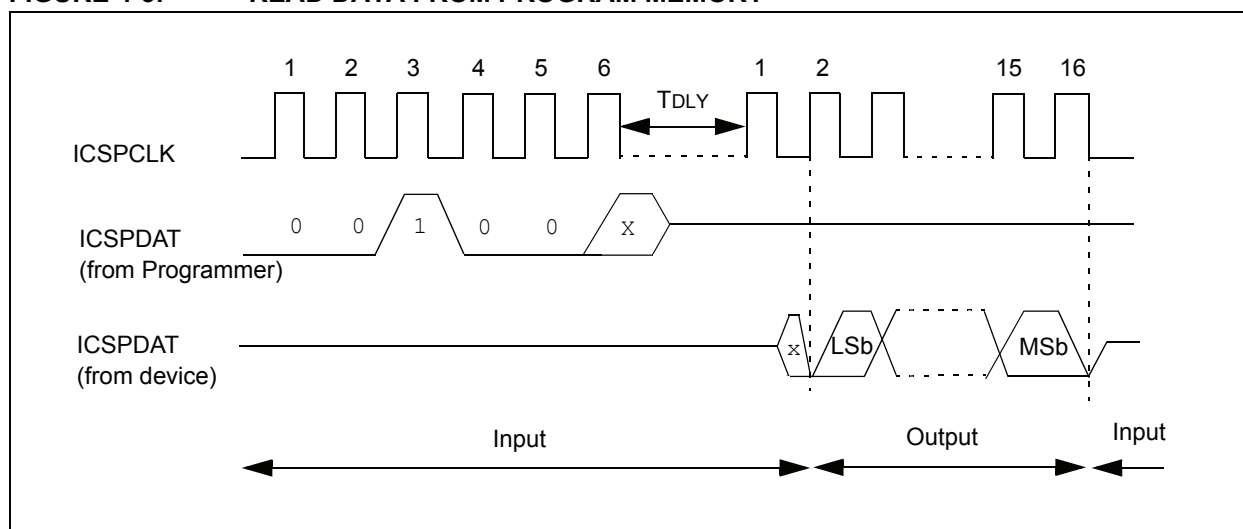
FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY



4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected (\overline{CP}), the data will be read as zeros (see Figure 4-3).

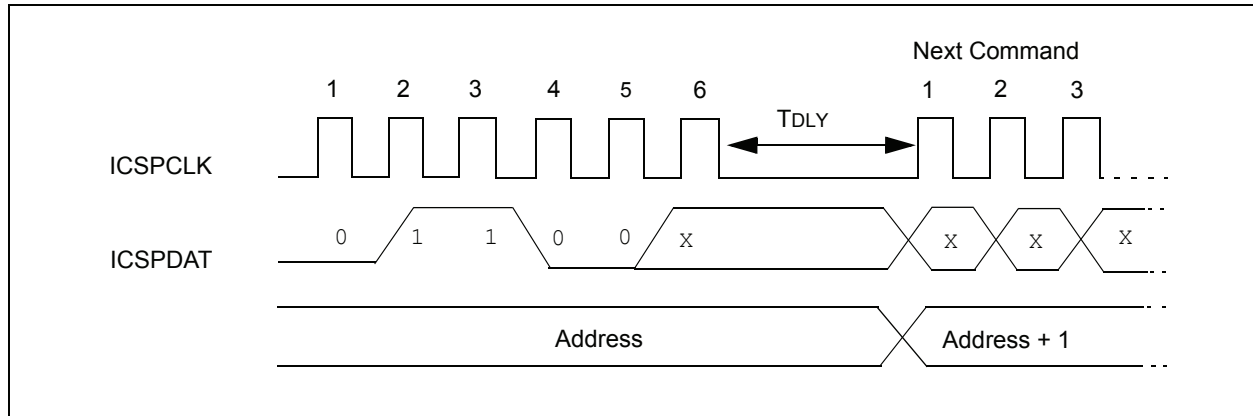
FIGURE 4-3: READ DATA FROM PROGRAM MEMORY



4.3.4 INCREMENT ADDRESS

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it. If the address is incremented from address 7FFFh, it will wrap-around to location 0000h. If the address is incremented from FFFFh, it will wrap-around to location 8000h.

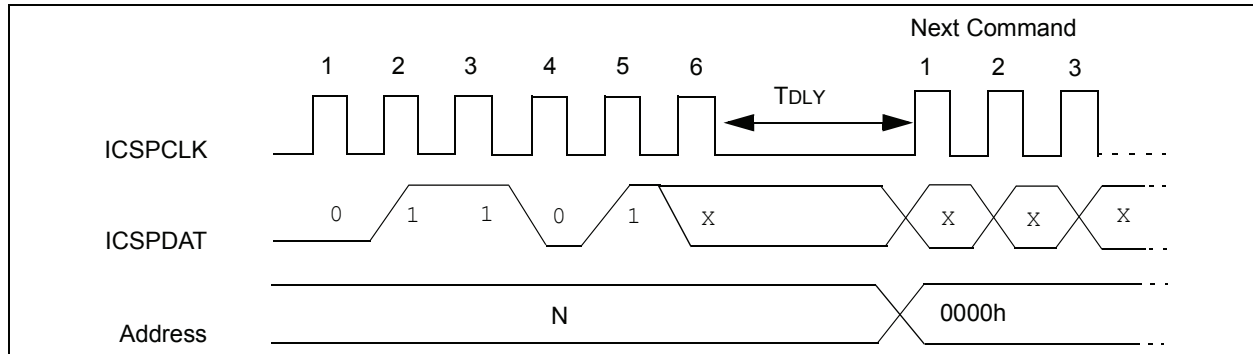
FIGURE 4-4: INCREMENT ADDRESS



4.3.5 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory.

FIGURE 4-5: RESET ADDRESS



PIC16(L)F151X/152X

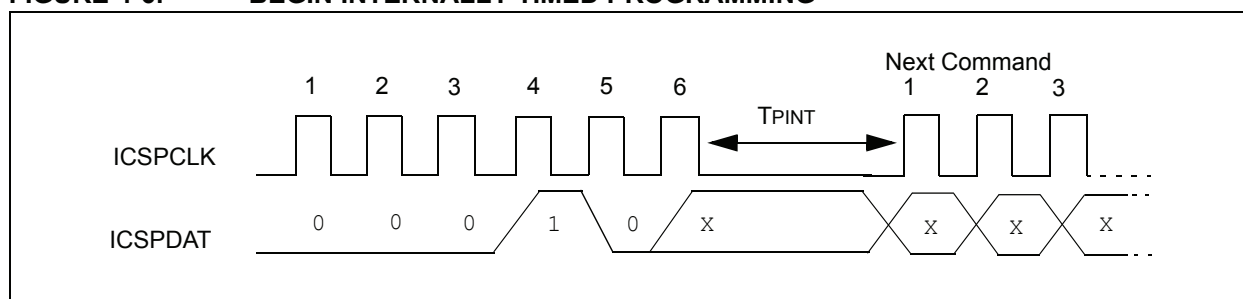
4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, T_{PINT} , for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed.

FIGURE 4-6: BEGIN INTERNALLY TIMED PROGRAMMING

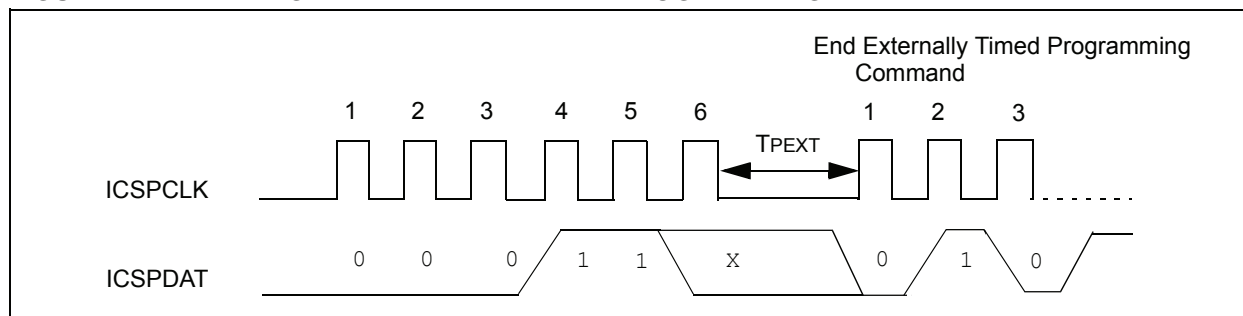


4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming the End Externally Timed Programming command must be sent in the specified time window defined by T_{PEXT} (see [Figure 4-7](#)).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 4-7: BEGIN EXTERNALLY TIMED PROGRAMMING

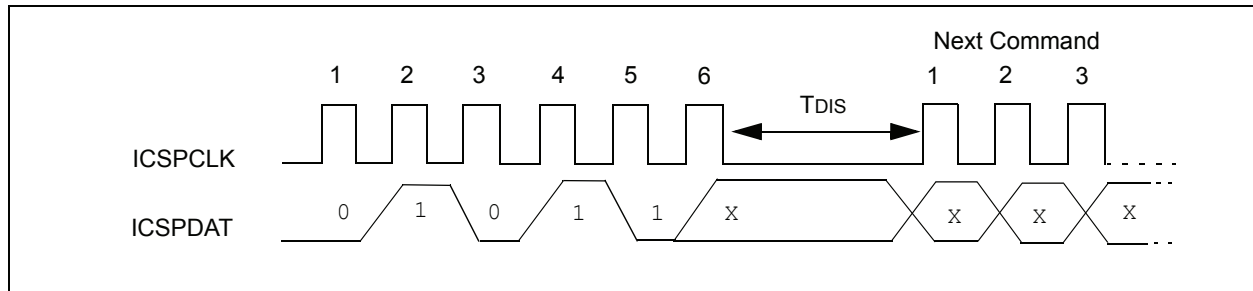


4.3.8 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPEXT after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 4-8).

FIGURE 4-8: END EXTERNALLY TIMED PROGRAMMING



4.3.9 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-7FFFh:

- Program Memory is erased
- Configuration Words are erased

Address 8000h-8008h:

- Program Memory is erased
- Configuration Words are erased
- User ID Locations are erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

After receiving the Bulk Erase Program Memory command the erase will not complete until the time interval, TERAB, has expired.

Note: The code protection Configuration bit (CP) has no effect on the Bulk Erase Program Memory command.

FIGURE 4-9: BULK ERASE PROGRAM MEMORY

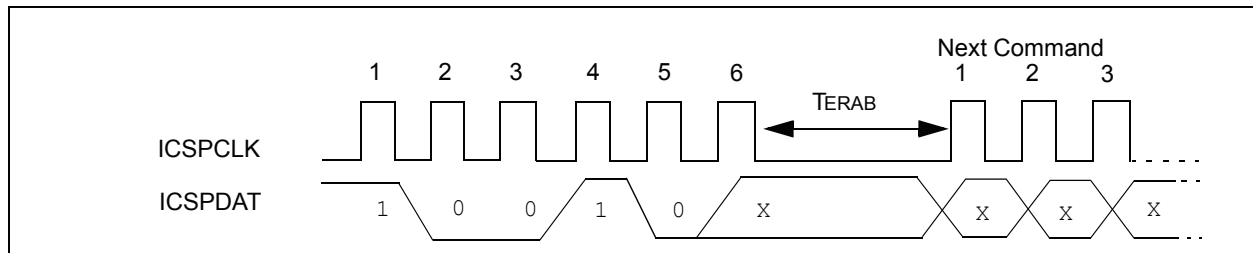
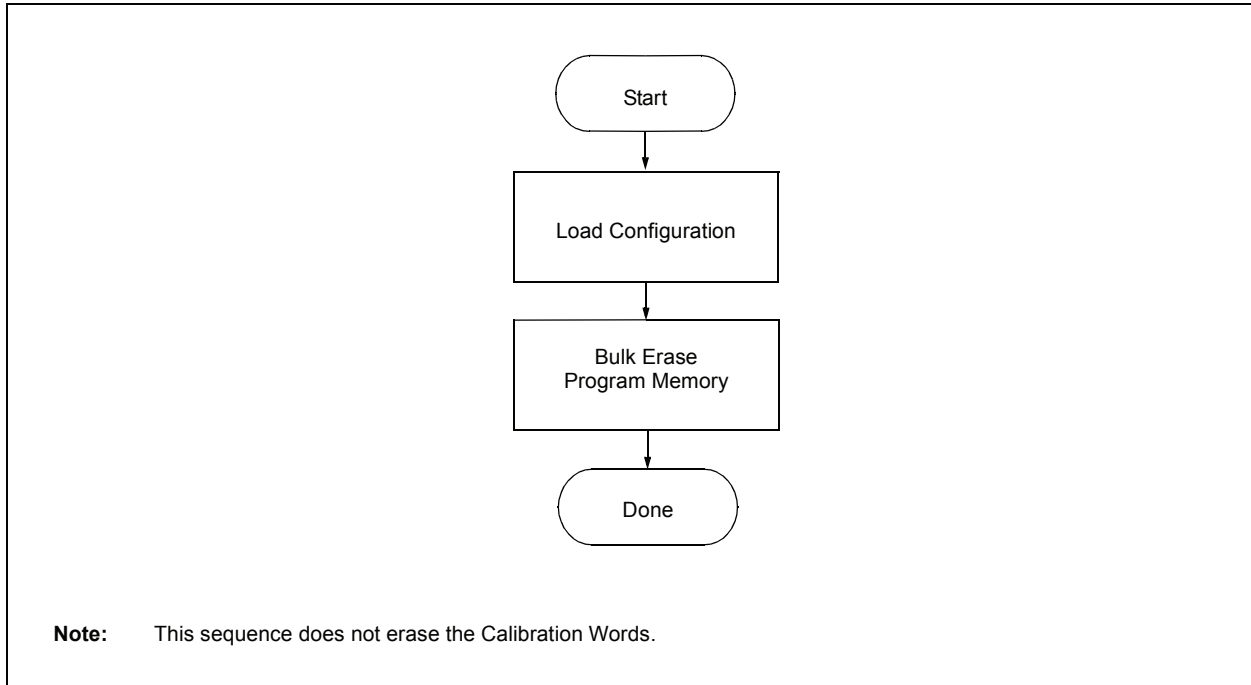


FIGURE 5-6: ERASE FLOWCHART



PIC16(L)F151X/152X

EXAMPLE 7-4: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED PIC16LF1527, 00AAh AT FIRST AND LAST ADDRESS

| | | |
|-------------|---|--|
| PIC16LF1527 | Configuration Word 1 ⁽²⁾ | 3F7Fh |
| | Configuration Word 1 mask ⁽³⁾ | 3EFFh |
| | Configuration Word 2 ⁽²⁾ | 3FFFh |
| | Configuration Word 2 mask ^{(3), (5)} | 3E03h |
| | User ID (8000h) ⁽¹⁾ | 000Eh |
| | User ID (8001h) ⁽¹⁾ | 0008h |
| | User ID (8002h) ⁽¹⁾ | 0005h |
| | User ID (8003h) ⁽¹⁾ | 0008h |
| | Sum of User IDs ⁽⁴⁾ | $= (000Eh \text{ and } 000Fh) \ll 12 + (0008h \text{ and } 000Fh) \ll 8 +$ $(0005h \text{ and } 000Fh) \ll 4 + (0008h \text{ and } 000Fh)$ $= E000h + 0800h + 0050h + 0008h$ $= E858h$ |
| | Checksum | $= (3F7Fh \text{ and } 3EFFh) + (3FFFh \text{ and } 3E03h) + \text{Sum of User IDs}$ $= 3E7Fh + 3E03h + E858h$ $= 64DAh$ |

- Note 1:** User ID values in this example are random values.
- 2:** Configuration Word 1 and 2 = all bits are '1' except the code-protect enable bit.
- 3:** Configuration Word 1 and 2 Mask = all Configuration Word bits are set to '1', except for unimplemented bits which read '0'.
- 4:** \ll = shift left, thus the LSb of the first user ID value is the MSb of the sum of user IDs and so on, until the LSb of the last user ID value becomes the LSb of the sum of user IDs.
- 5:** On the PIC16LF1527 device, the $\overline{\text{VCPEN}}$ bit is not implemented in Configuration Word 2; thus, all unimplemented bits are '0'.

8.0 ELECTRICAL SPECIFICATIONS

Refer to device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

| AC/DC CHARACTERISTICS | | | Standard Operating Conditions Production tested at 25°C | | | | |
|---------------------------------|--|----------------------------|--|------|-------------------------------|-------|--|
| Sym. | Characteristics | | Min. | Typ. | Max. | Units | Conditions/Comments |
| Supply Voltages and Currents | | | | | | | |
| VDD | Supply Voltage (VDDMIN, VDDMAX) | PIC16F151X PIC16F152X | 2.3 | — | 5.5 | V | |
| | | PIC16LF151X PIC16LF152X | 1.8 | — | 3.6 | V | |
| | | | | | | | |
| VPEW | Read/Write and Row Erase operations | | VDDMIN | — | VDDMAX | V | |
| VPBE | Bulk Erase operations | | 2.7 | — | VDDMAX | V | |
| IDDI | Current on VDD, Idle | | — | — | 1.0 | mA | |
| IDDP | Current on VDD, Programming | | — | — | 3.0 | mA | |
| IPP | VPP | | | | | | |
| | Current on MCLR/VPP | | — | — | 600 | μA | |
| VIHH | High voltage on MCLR/VPP for Program/Verify mode entry | | 8.0 | — | 9.0 | V | |
| TVHHR | MCLR rise time (VIL to VIH) for Program/Verify mode entry | | — | — | 1.0 | μs | |
| I/O pins | | | | | | | |
| VIH | (ICSPCLK, ICSPDAT, MCLR/VPP) input high level | | 0.8 VDD | — | — | V | |
| VIL | (ICSPCLK, ICSPDAT, MCLR/VPP) input low level | | — | — | 0.2 VDD | V | |
| VOH | ICSPDAT output high level | | VDD-0.7 VDD-0.7 VDD-0.7 | — | — | V | IOH = 3.5 mA, VDD = 5V IOH = 3 mA, VDD = 3.3V IOH = 2 mA, VDD = 1.8V |
| VOL | ICSPDAT output low level | | — | — | VSS+0.6 VSS+0.6 VSS+0.6 | V | IOH = 8 mA, VDD = 5V IOH = 6 mA, VDD = 3.3V IOH = 3 mA, VDD = 1.8V |
| Programming Mode Entry and Exit | | | | | | | |
| TENTS | Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before VDD or MCLR↑ | | 100 | — | — | ns | |
| TENTH | Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after VDD or MCLR↑ | | 250 | — | — | μs | |
| Serial Program/Verify | | | | | | | |
| TCKL | Clock Low Pulse Width | | 100 | — | — | ns | |
| TCKH | Clock High Pulse Width | | 100 | — | — | ns | |
| TDS | Data in setup time before clock↓ | | 100 | — | — | ns | |
| TDH | Data in hold time after clock↓ | | 100 | — | — | ns | |
| TCO | Clock↑ to data out valid (during a Read Data command) | | 0 | — | 80 | ns | |
| TLZD | Clock↓ to data low-impedance (during a Read Data command) | | 0 | — | 80 | ns | |
| THZD | Clock↓ to data high-impedance (during a Read Data command) | | 0 | — | 80 | ns | |
| TDLY | Data input not driven to next clock input (delay required between command/data or command/command) | | 1.0 | — | — | μs | |
| TERAB | Bulk Erase cycle time | | — | — | 5 | ms | |
| TERAR | Row Erase cycle time | | — | — | 2.5 | ms | |

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

PIC16(L)F151X/152X

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY

| AC/DC CHARACTERISTICS | | Standard Operating Conditions Production tested at 25°C | | | | |
|-----------------------|---|--|------|----------|----------|---------------------------------------|
| Sym. | Characteristics | Min. | Typ. | Max. | Units | Conditions/Comments |
| TPINT | Internally timed programming operation time | — | — | 2.5 5 | ms ms | Program memory Configuration Words |
| TPEXT | Externally timed programming pulse | 1.0 | — | 2.1 | ms | Note 1 |
| TDIS | Time delay from program to compare (HV discharge time) | 300 | — | — | μs | |
| TEXT | Time delay when exiting Program/Verify mode | 1 | — | — | μs | |

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – VDD FIRST

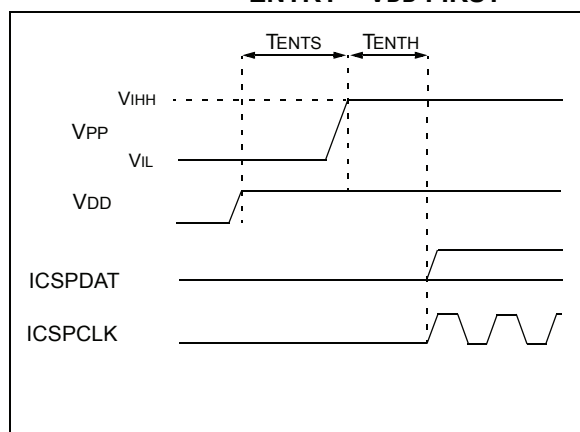


FIGURE 8-2: PROGRAMMING MODE ENTRY – VPP FIRST

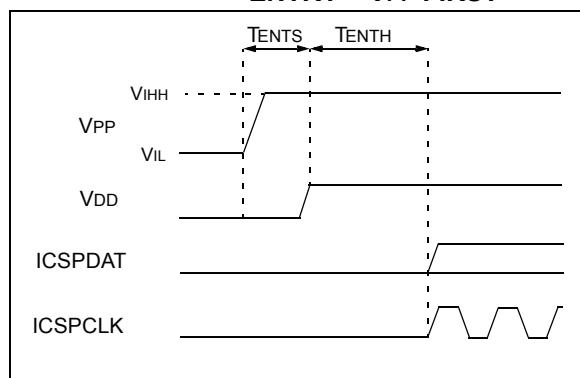


FIGURE 8-3: PROGRAMMING MODE EXIT – VPP LAST

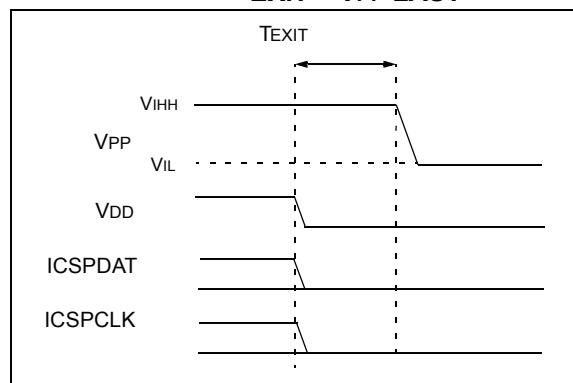
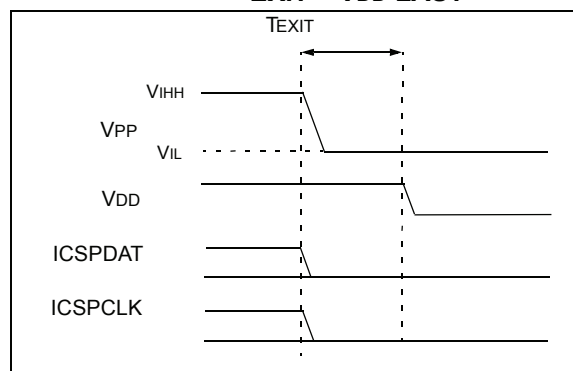


FIGURE 8-4: PROGRAMMING MODE EXIT – VDD LAST



APPENDIX A: REVISION HISTORY

Revision A (08/2010)

Original release of this document.

Revision B (09/2011)

Added PIC16(L)F1512/1513 devices; Added new Figures 3-1 and 3-2; Updated Registers 3-1, 3-2 and 3-3 to new format; Updated Register 3-3 to add 2 kW and 4 kW Flash memory; Added Notes to Examples 7-1 to 7-4; Updated Table 8-1; Other minor corrections.

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ISBN: 978-1-61341-635-8

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