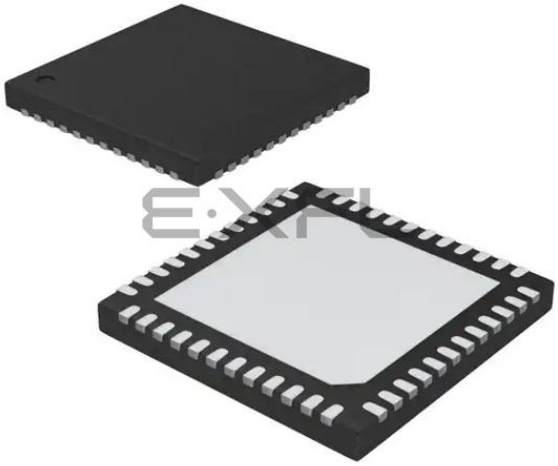
Analog Devices Inc./Maxim Integrated - MAXQ7665BATM+ Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	16-Bit
Speed	8MHz
Connectivity	CANbus, LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	8
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 16
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-SQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq7665batm

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

ABSOLUTE MAXIMUM RATINGS

DV_{DD} to DGND, AGND, or GNDIO .....-0.3V to +4V
DGND to GNDIO or AGND.....-0.3V to +0.3V
DV_{DDIO} to DGND, AGND, or GNDIO .....-0.3V to +6V
AV_{DD} to DGND, AGND, or GNDIO.....-0.3V to +6V
Digital Inputs/Outputs to DGND, AGND, or GNDIO
.....-0.3V to (DV_{DDIO} + 0.3V)
Analog Inputs/Outputs to DGND, AGND, or GNDIO
.....-0.3V to (AV_{DD} + 0.3V)
$\overline{RESET}$, XIN, XOUT to DGND, AGND, or GNDIO
.....-0.3V to (DV_{DD} + 0.3V)
Continuous Current into Any Pin.....±50mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFN (derate 40mW/°C above +70°C) 3200mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIRMENTS						
Supply Voltage Range	DV_{DD}	Safe mode (RC/2 = 3.8MHz)	2.7	3.3	3.6	V
		Normal mode	3.0	3.3	3.6	
	AV_{DD}		4.75	5.0	5.25	
	DV_{DDIO}		4.75	5.0	5.25	
AV_{DD} Supply Current	I_{AVDD}	Shutdown (Note 2)		0.1	10	µA
		All analog functions enabled		6.7	8	mA
Analog Module Subfunction Incremental Supply Current		ADC enabled, f_{ADC} = 1ksps, f_{SYSCLK} = 8MHz		4.2		µA
		ADC enabled, f_{ADC} = 500ksps, f_{SYSCLK} = 8MHz		1890		
		DAC enabled (zero scale)		305		
		Internal temperature sensor enabled		502		
		Additional current when one or more of the ADC, DAC, and/or temperature sensor is enabled (only counted once)		128		
		PGA enabled		4.5		mA
DV_{DD} Supply Current	I_{DVDD}	CPU in stop mode, all peripherals disabled		3	20	µA
		High-speed mode (Note 3)			28	mA
		Flash erase or write mode		35	50	
DV_{DD} Module Subfunction Incremental Supply Current		DV_{DD} supervisor and brownout monitor		2		µA
		HF crystal oscillator		150		
		Internal RC oscillator		200		
DV_{DDIO} Supply Current	I_{DVDDIO}	All digital I/Os static at GND or DV_{DDIO}			10	µA
		(Note 4)			1000	

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range	SFDR	PGA gain = 1V/V			-91		dB
Conversion Clock Frequency	f_{ADCCLK}	f_{SYSCLK} = 8MHz		0.5		8.0	MHz
Sample Rate	f_{SAMPLE}	PGA gain = 1V/V, $R_{SOURCE} \le 1k\Omega$				500	ksps
		Any PGA gain setting > 1V/V, $R_{SOURCE} \le 5k\Omega$				142	
Conversion Time	t_{CONV}	t_{ACQ} plus 13 ADCCLK cycles at 8MHz				t_{ACQ} + 1.625	µs
Channel/Gain Select Plus Conversion Time		PGA gain = 1V/V, $R_{SOURCE} \le 1k\Omega$				2	µs
		Any PGA gain setting, $R_{SOURCE} \le 5k\Omega$				7	
Track-and-Hold Acquisition Time	t_{ACQ}	PGA gain = 1V/V, $R_{SOURCE} \le 1k\Omega$				375	ns
		Any PGA gain setting > 1V/V, $R_{SOURCE} \le 5k\Omega$				5	µs
Turn-On Time	t_{RECOV}				5		µs
Aperture Delay					30		ns
Aperture Jitter					50		ps_{P-P}
Input-Voltage Range		Unipolar mode	PGA gain = 1	0		AV_{DD}	V
			PGA gain = 2	0		1.6	
			PGA gain = 4	0		0.8	
			PGA gain = 8	0		0.4	
			PGA gain = 16	0		0.2	
			PGA gain = 32	0		0.1	
		Bipolar mode, AIN+ to AIN-	PGA gain = 1	$-V_{REFADC}/2$		$+V_{REFADC}/2$	
			PGA gain = 2	$-V_{REFADC}/4$		$+V_{REFADC}/4$	
			PGA gain = 4	$-V_{REFADC}/8$		$+V_{REFADC}/8$	
			PGA gain = 8	$-V_{REFADC}/16$		$+V_{REFADC}/16$	
			PGA gain = 16	$-V_{REFADC}/32$		$+V_{REFADC}/32$	
			PGA gain = 32	$-V_{REFADC}/64$		$+V_{REFADC}/64$	
Absolute Input-Voltage Range				AGND		AV_{DD}	V
Input Leakage Current		AIN15–AIN0			±20		nA
Small-Signal Bandwidth (-3dB)		V_{IN} x gain = $100mV_{P-P}$	PGA gain = 1		180		MHz
			PGA gain = 2		140		
			PGA gain = 4		120		
			PGA gain = 8		100		
			PGA gain = 16		82		
			PGA gain = 32		80		

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC Glitch Impulse		From 7FFh to 800h			12		nV•s
DAC Power-On Time		Excluding reference, settling to ±0.5 LSB			14		µs
Power-Supply Rejection		AV_{DD} step from +4.75V to +5.25V			62		µV/V
Output Noise		C_L = 200pF			200		$µV_{RMS}$
EXTERNAL REFERENCE INPUTS							
REFADC Input-Voltage Range				1.0	5.0	AV_{DD}	V
REFDAC Input-Voltage Range				0	5.0	AV_{DD}	V
REFDAC Input Impedance					200		kΩ
REFADC Leakage Current		ADC disabled			1		µA
TEMPERATURE SENSOR (Remote NPN Transistor 2N3904)							
Temperature Error		Internal diode	T_A = +25°C		±1		°C
			T_A = -30°C to +85°C		±2		
			T_A = -40°C to +125°C		±5		
		External diode, differential configuration (Note 6)	T_A = +25°C, T_{RJ} = +25°C		±2		
			T_A = -30°C to +85°C, T_{RJ} = +25°C		±3		
			T_A = -40°C to +125°C, T_{RJ} = +25°C		±3		
			T_A = -30°C to +85°C, T_{RJ} = -30°C to +85°C		±3		
			T_A = -40°C to +125°C, T_{RJ} = -40°C to +125°C		±5		
Internal (Die) or External Temperature Measurement Error vs. V_{REFADC} Variation					0.095		°C/mV
External Diode Source Current		High level			74.7		µA
		Low level			4		
External Diode Drive Current Ratio					18.7:1		µA/µA
Conversion Time		f_{ADCCLK} = f_{SYSCLK} = 8MHz, no interrupts, internal utility ROM tempConv			70		µs
Temperature Resolution		12-bit ADC			0.125		°C/LSB
+3.3V LINEAR REGULATOR (C_{DVDD} = 4.7µF)							
DV_{DDIO} Input-Voltage Range				4.25	5.0	5.25	V
DV_{DD} Output Voltage		$\overline{REGEN}$ = GNDIO		3.0	3.4	3.6	V
DV_{DD} Input-Voltage Range		$\overline{REGEN}$ = DV_{DDIO}		3.0		3.6	V
No-Load Quiescent Current		CPU in sleep mode; all digital peripherals disabled			15		µA
Output Short-Circuit Current		Short to DGND			110		mA

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

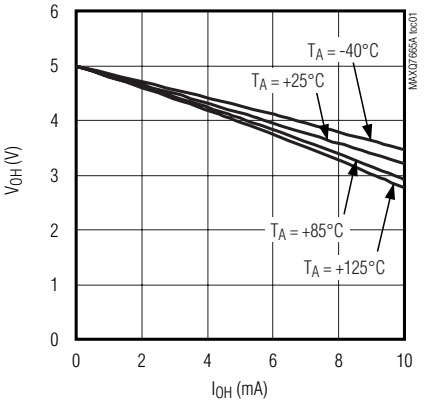
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE SUPERVISORS AND BROWNOUT DETECTION							
DV_{DD} Voltage-Supervisor Reset Rising Threshold		Power-on default, DV_{DD} voltage rising (Note 7)		2.70		2.99	V
DV_{DD} Voltage-Supervisor Brownout Reset Falling Threshold	V_{VDBR}	DV_{DD} voltage falling, firmware selectable, measured with CPU active at 8MHz (Note 8)	VDBR = 00b (default)	2.70		2.99	V
			VDBR = 01b	2.77		3.06	
			VDBR = 10b	2.84		3.13	
			VDBR = 11b	2.91		3.20	
Software-Selectable DV_{DD} Voltage-Supervisor Brownout Interrupt Falling Threshold	V_{VDBI}	DV_{DD} voltage falling, firmware selectable, measured with CPU active at 8MHz (Note 9)	VDBI = 00b (default)	2.77		3.06	V
			VDBI = 01b	2.84		3.13	
			VDBI = 10b	2.91		3.20	
			VDBI = 11b	2.99		3.27	
DV_{DDIO} Voltage-Supervisor Brownout Interrupt Threshold	V_{VIOBI}	DV_{DDIO} voltage falling, firmware selectable, measured with CPU active at 8MHz (Note 10)	VIOBI = 00b (default)	4.25		4.74	V
			VIOBI = 01b	4.30		4.79	
			VIOBI = 10b	4.35		4.84	
			VIOBI = 11b	4.40		4.89	
Voltage-Supervisor Hysteresis		DV_{DD}, DV_{DDIO}			1		%
DV_{DD} Brownout-Interrupt to Brownout Reset Falling Threshold		Voltage difference between V_{VDBI} and V_{VDBR}, time allowing software clean-up before reset asserted, VDBI = 11b and VDBR = 10b		155			mV
Voltage Monitor Range		DV_{DD}		1.0		3.6	V
		DV_{DDIO}		0		5.25	
DV_{DD} Ramp-Up Rate		DV_{DD} must rise faster than this rate between +2.7V and +3.0V		35			mV/ms
$\overline{RESET}$ Hold Time		After DV_{DD} rises above the V_{VDBR} voltage trip threshold			16		ms
CAN INTERFACE							
CAN Baud Rate		CANCLK = 8MHz				1	Mbps
CANCLK Mean Frequency Error		50ppm external crystal error, 8MHz crystal			60		ppm
CANCLK Total Frequency Error		50ppm external crystal error, 8MHz crystal, clock divided and measured over 500µs interval, mean plus peak cycle jitter			< 0.5		%
HIGH-FREQUENCY CRYSTAL OSCILLATOR							
Clock Frequency		Using external crystal		7.6		8.12	MHz
		External clock source		7.6		8.12	
Crystal Oscillator Startup Time		8MHz crystal			10		ms
External Clock Input Duty Cycle		Ratio high-to-low or low-to-high		45		55	%

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

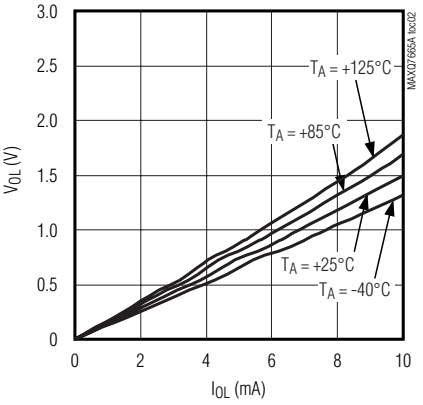
Typical Operating Characteristics

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{ADCCLK} = 8MHz, f_{ADC} = 500kHz, T_A = +25°C, unless otherwise noted.)

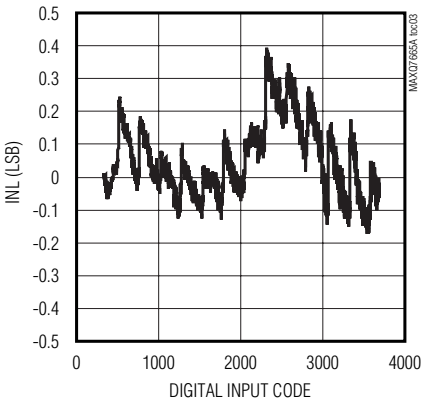
GPO._ OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



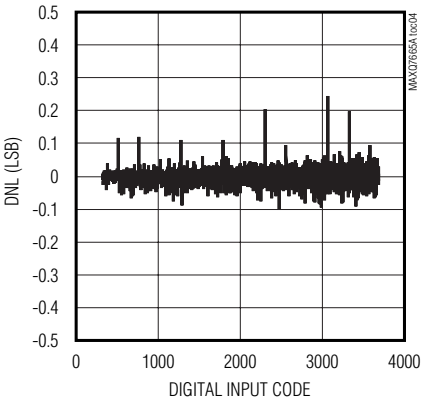
GPO._ OUTPUT LOW VOLTAGE vs. SINK CURRENT



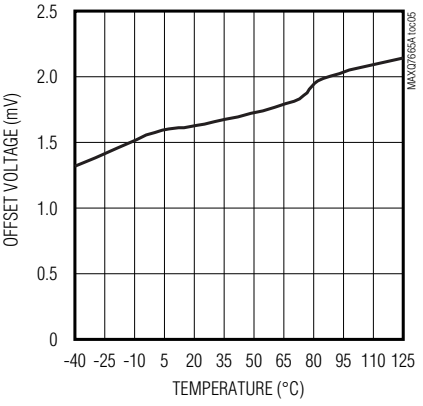
DAC INL vs. INPUT CODE (REFDAC = +5V)



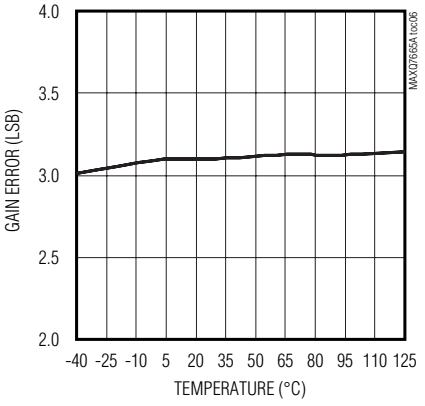
DAC DNL vs. INPUT CODE (REFDAC = +5V)



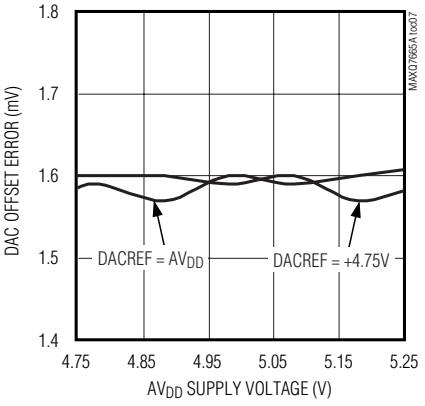
DAC OFFSET VOLTAGE vs. TEMPERATURE



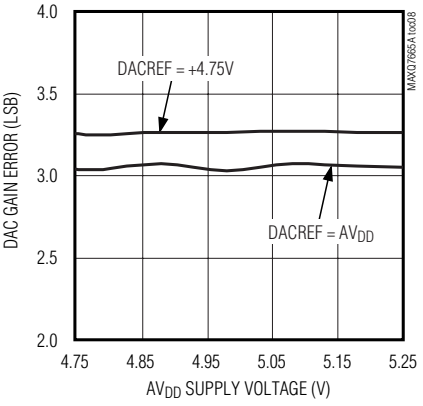
DAC GAIN ERROR vs. TEMPERATURE



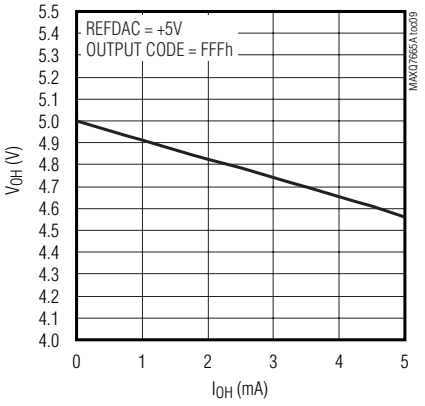
DAC OFFSET ERROR vs. AV_{DD} SUPPLY VOLTAGE



DAC GAIN ERROR vs. AV_{DD} SUPPLY VOLTAGE



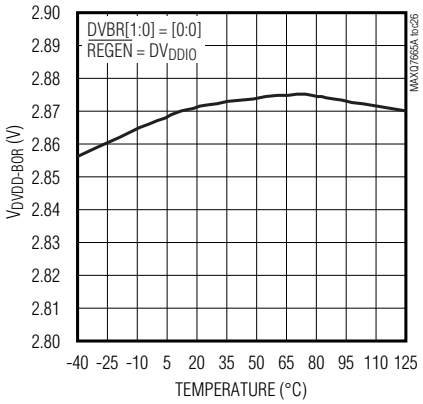
DACOUT OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



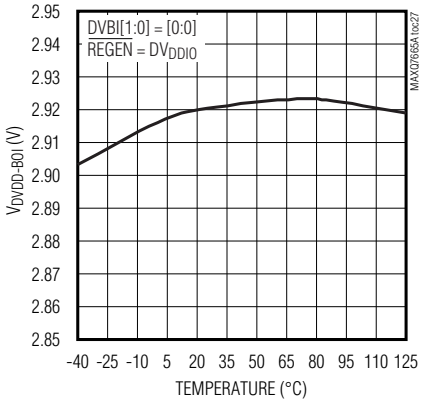
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{ADCCLK} = 8MHz, f_{ADC} = 500kHz, T_A = +25°C, unless otherwise noted.)

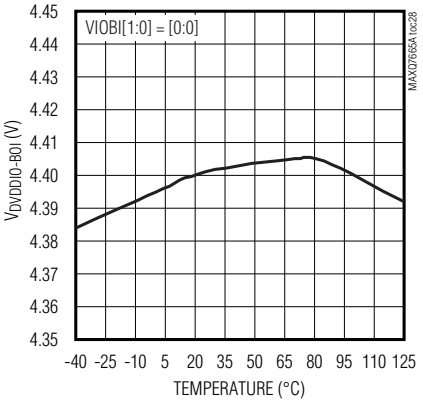
DV_{DD} BOR THRESHOLD VOLTAGE vs. TEMPERATURE



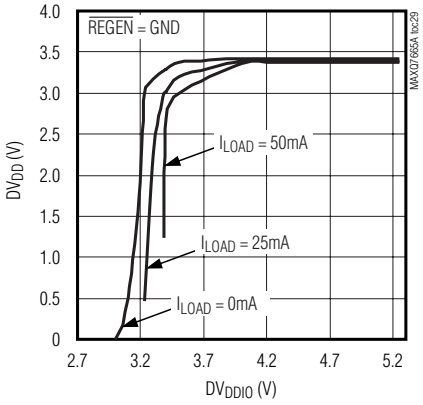
DV_{DD} BOI THRESHOLD VOLTAGE vs. TEMPERATURE



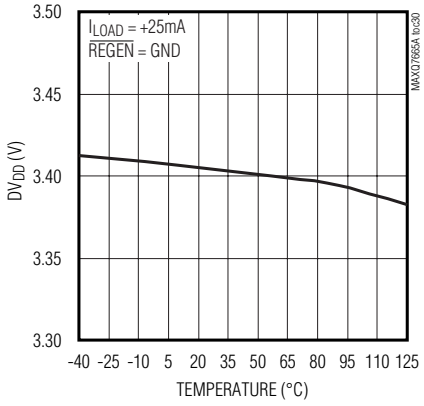
DV_{DDIO} BOI THRESHOLD VOLTAGE vs. TEMPERATURE



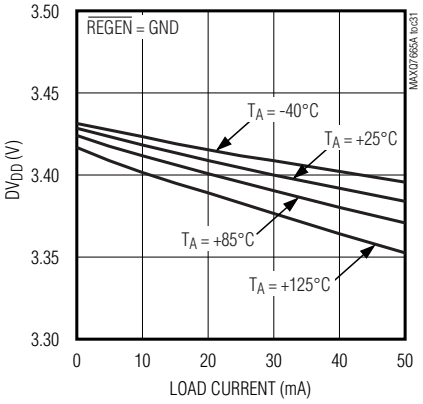
DV_{DD} LINEAR REGULATOR OUTPUT VOLTAGE vs. DV_{DDIO} SUPPLY VOLTAGE



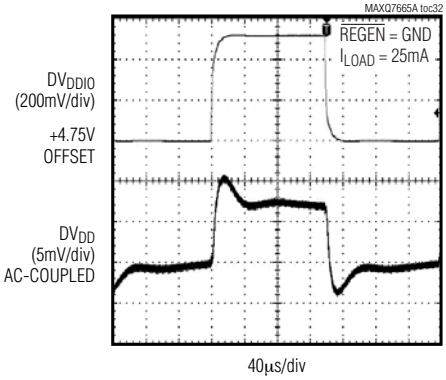
DV_{DD} LINEAR REGULATOR OUTPUT VOLTAGE vs. TEMPERATURE



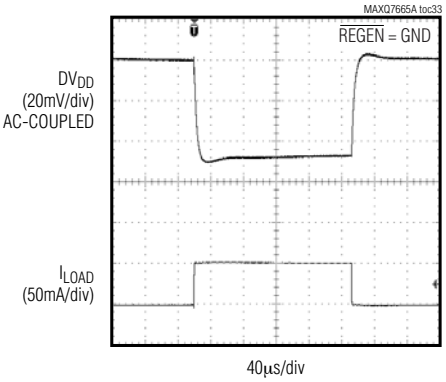
DV_{DD} LINEAR REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



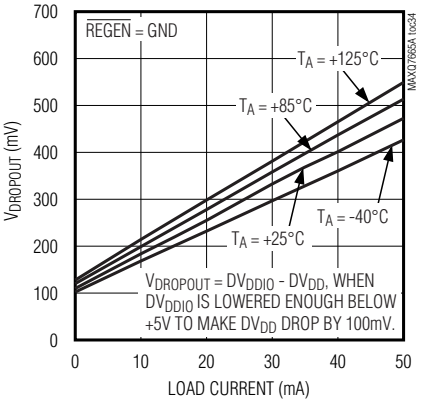
DV_{DD} LINEAR REGULATOR OUTPUT VOLTAGE LINE TRANSIENT (DV_{DDIO} = +4.75V TO +5.25V STEP)



DV_{DD} LINEAR REGULATOR OUTPUT VOLTAGE LOAD TRANSIENT (I_{DVDD} = 0 TO 50mA STEP)



DV_{DD} LINEAR REGULATOR DROPOUT VOLTAGE vs. LOAD CURRENT

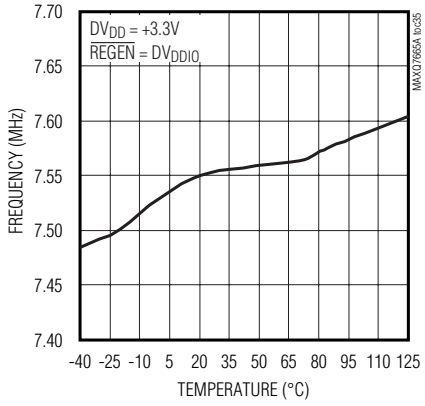


16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

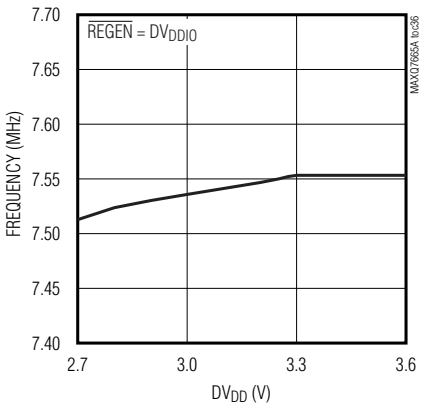
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{ADCCLK} = 8MHz, f_{ADC} = 500kHz, T_A = +25°C, unless otherwise noted.)

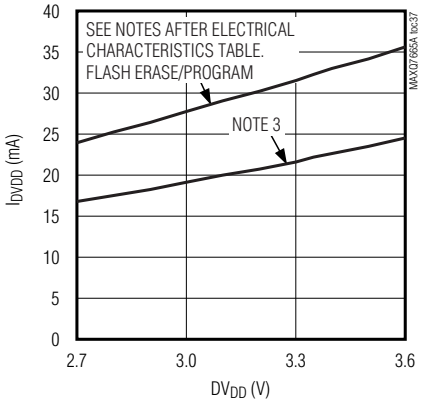
RC OSCILLATOR OUTPUT FREQUENCY vs. TEMPERATURE



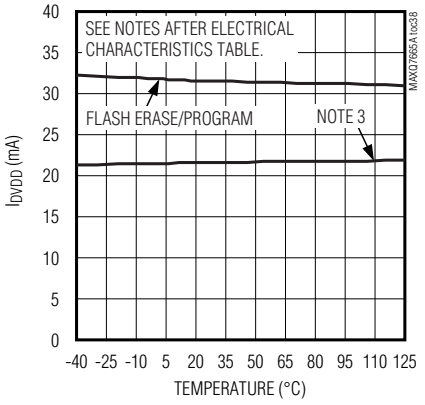
RC OSCILLATOR OUTPUT FREQUENCY vs. DV_{DD} SUPPLY VOLTAGE



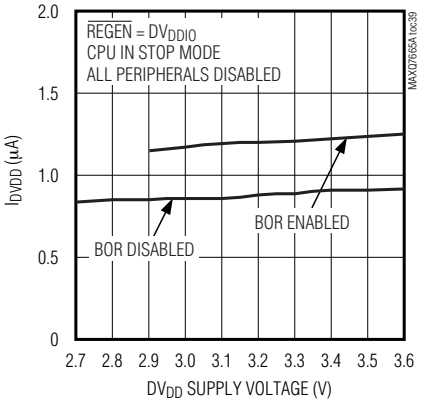
DV_{DD} ACTIVE SUPPLY CURRENT vs. DV_{DD} SUPPLY VOLTAGE



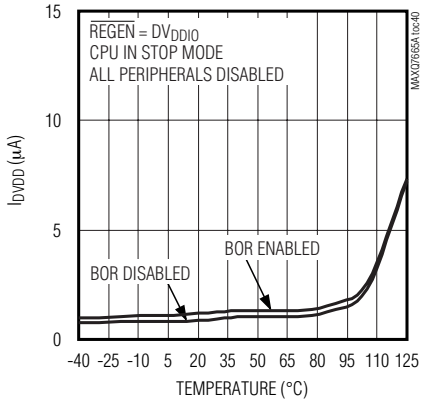
DV_{DD} ACTIVE SUPPLY CURRENT vs. TEMPERATURE



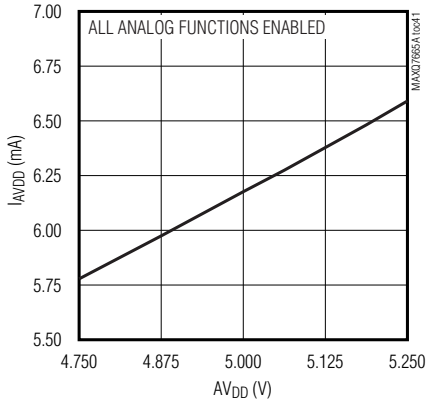
DV_{DD} STOP-MODE SUPPLY CURRENT vs. DV_{DD} SUPPLY VOLTAGE



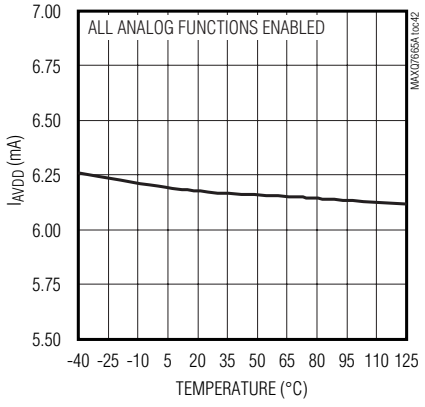
DV_{DD} STOP-MODE SUPPLY CURRENT vs. TEMPERATURE



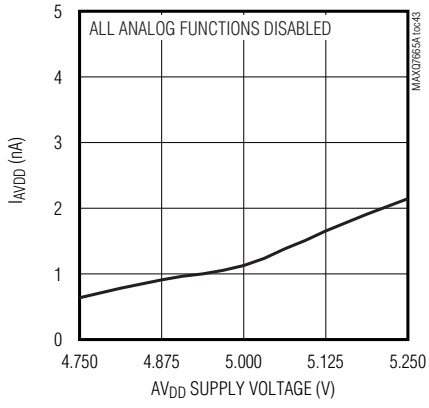
AV_{DD} ENABLED SUPPLY CURRENT vs. AV_{DD} SUPPLY VOLTAGE



AV_{DD} ENABLED SUPPLY CURRENT vs. TEMPERATURE



AV_{DD} DISABLED SUPPLY CURRENT vs. AV_{DD} SUPPLY VOLTAGE



16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

Pin Description

PIN	NAME	FUNCTION
1	AIN11	Analog Input Channel 11. AIN11 is multiplexed to the PGA as a differential input with AIN10.
2	AIN10	Analog Input Channel 10. AIN10 is multiplexed to the PGA as a differential input with AIN11.
3	AIN9	Analog Input Channel 9. AIN9 is multiplexed to the PGA as a differential input with AIN8.
4	AIN8	Analog Input Channel 8. AIN8 is multiplexed to the PGA as a differential input with AIN9.
5, 8	AGND	Analog Ground
6	REFADC	ADC External Reference Input. Connect an external reference voltage between 1V and AV_{DD} to REFADC.
7	REFDAC	DAC External Reference Input. Connect an external reference voltage between 0V and AV_{DD} to REFDAC.
9	AIN7	Analog Input Channel 7. AIN7 is multiplexed to the PGA as a differential input with AIN6.
10	AIN6	Analog Input Channel 6. AIN6 is multiplexed to the PGA as a differential input with AIN7.
11	AIN5	Analog Input Channel 5. AIN5 is multiplexed to the PGA as a differential input with AIN4.
12	AIN4	Analog Input Channel 4. AIN4 is multiplexed to the PGA as a differential input with AIN5.
13	AIN3	Analog Input Channel 3. AIN3 is multiplexed to the PGA as a differential input with AIN2. AIN3–AIN0 have remote temperature sensor capability.
14	AIN2	Analog Input Channel 2. AIN2 is multiplexed to the PGA as a differential input with AIN3. AIN3–AIN0 have remote temperature sensor capability.
15	AIN1	Analog Input Channel 1. AIN1 is multiplexed to the PGA as a differential input with AIN0. AIN3–AIN0 have remote temperature sensor capability.
16	AIN0	Analog Input Channel 0. AIN0 is multiplexed to the PGA as a differential input with AIN1. AIN3–AIN0 have remote temperature sensor capability.
17	DACOUT	DAC Buffer Output. DACOUT is the DAC voltage buffer output.
18, 19, 31	DGND	Digital Ground for the Digital Core and Flash
20	CANRXD	CAN Bus Receiver Input. Control area network receiver input.
21	CANTXD	CAN Bus Transmitter Output. Control area network transmitter output.
22	UTX	UART Transmitter Output
23	URX	UART Receiver Input
24	P0.6/T0	Port 0 Bit 6/Timer 0. P0.6 is a general-purpose digital I/O with interrupt/wake-up input capability. T0 is a primary timer/PWM input or output.
25	P0.7/T1	Port 0 Bit 7/Timer 1. P0.7 is a general-purpose digital I/O with interrupt/wake-up input capability. T1 is a primary timer/PWM input or output.
26, 39	DV_{DDIO}	Digital I/O Supply Voltage. Supplies all digital I/O except for XIN, XOUT, and $\overline{RESET}$. Bypass DV_{DDIO} to GNDIO with a 0.1µF capacitor placed as close as possible to the device. DV_{DDIO} is also connected to the input of the linear regulator.
27	GNDIO	Digital I/O Ground
28, 29	I.C.	Internal Connection. Connect I.C. to GNDIO or DV_{DDIO}.
30	N.C.	No Connection. No internal connection. Leave N.C. unconnected.
32	P0.0/TDO	Port 0 Data 0/JTAG Serial Test Data Output. P0.0 is a general-purpose digital I/O with interrupt/wake-up capability. TDO is the JTAG serial test, data output.

Pin Description (continued)

PIN	NAME	FUNCTION
33	P0.1/TMS	Port 0 Data 1/JTAG Test Mode Select. P0.1 is a general-purpose digital I/O with interrupt/wake-up capability. TMS is the JTAG test mode, select input.
34	P0.2/TDI	Port 0 Data 2/JTAG Serial Test Data Input. P0.2 is a general-purpose digital I/O with interrupt/wake-up capability. TDI is the JTAG serial test, data input.
35	P0.3/TCK	Port 0 Data 3/JTAG Serial Test Clock Input. P0.3 is a general-purpose digital I/O with interrupt/wake-up capability. TCK is the JTAG serial test, clock input.
36	P0.4/ADCCNV	Port 0 Data 4/ADC Start Conversion Control. P0.4 is a general-purpose digital I/O. ADCCNV is firmware configurable for a rising or falling edge start/convert to trigger ADC conversions.
37	P0.5/DACLOAD	Port 0 Data 5/DAC Data Register Load/Update Input. P0.5 is a general-purpose digital I/O with interrupt/wake-up capability. DACLOAD is firmware configurable for a rising or falling edge to update the DACOUT register.
38	$\overline{\text{REGEN}}$	Active-Low Linear Regulator Enable Input. Connect $\overline{\text{REGEN}}$ to GNDIO to enable the linear regulator. Connect to DV_{DDIO} to disable the linear regulator.
40	DV_{DD}	Digital Supply Voltage. DV_{DD} supplies the internal digital core and flash memory. DV_{DD} is internally connected to the output of the internal 3.3V linear regulator. Disable the internal regulator to connect DV_{DD} to an external supply. When using the on-chip linear regulator, bypass DV_{DD} to DGND with a 4.7µF ±20% capacitor with a maximum ESR of 0.5Ω. In addition, bypass DV_{DD} with a 0.1µF capacitor. Place both bypass capacitors as close as possible to the device.
41	$\overline{\text{RESET}}$	Reset Input and Output. Active-low open-drain input/output with internal 360kΩ pullup to DV_{DD}. Drive low to reset the µC. $\overline{\text{RESET}}$ is low during power-up reset and during DV_{DD} brownout conditions.
42	XOUT	High-Frequency Crystal Output. Connect an external crystal to XIN and XOUT for normal operation. Leave XOUT unconnected if XIN is driven with an external clock source. XOUT is not driven when using the internal RC oscillator.
43	XIN	High-Frequency Crystal Input. Connect an external crystal or resonator to XIN and XOUT for normal operation, or drive XIN with an external clock source. XIN is not driven when using the internal RC oscillator.
44	AV_{DD}	Analog Supply Voltage Input. Connect AV_{DD} to a +5V supply. Bypass AV_{DD} to AGND with a 0.1µF capacitor placed as close as possible to the device.
45	AIN15	Analog Input Channel 15. AIN15 is multiplexed to the PGA as a differential input with AIN14.
46	AIN14	Analog Input Channel 14. AIN14 is multiplexed to the PGA as a differential input with AIN15.
47	AIN13	Analog Input Channel 13. AIN13 is multiplexed to the PGA as a differential input with AIN12.
48	AIN12	Analog Input Channel 12. AIN12 is multiplexed to the PGA as a differential input with AIN13.
—	EP	Exposed Pad. EP is internally connected to AGND. Connect EP to AGND externally.

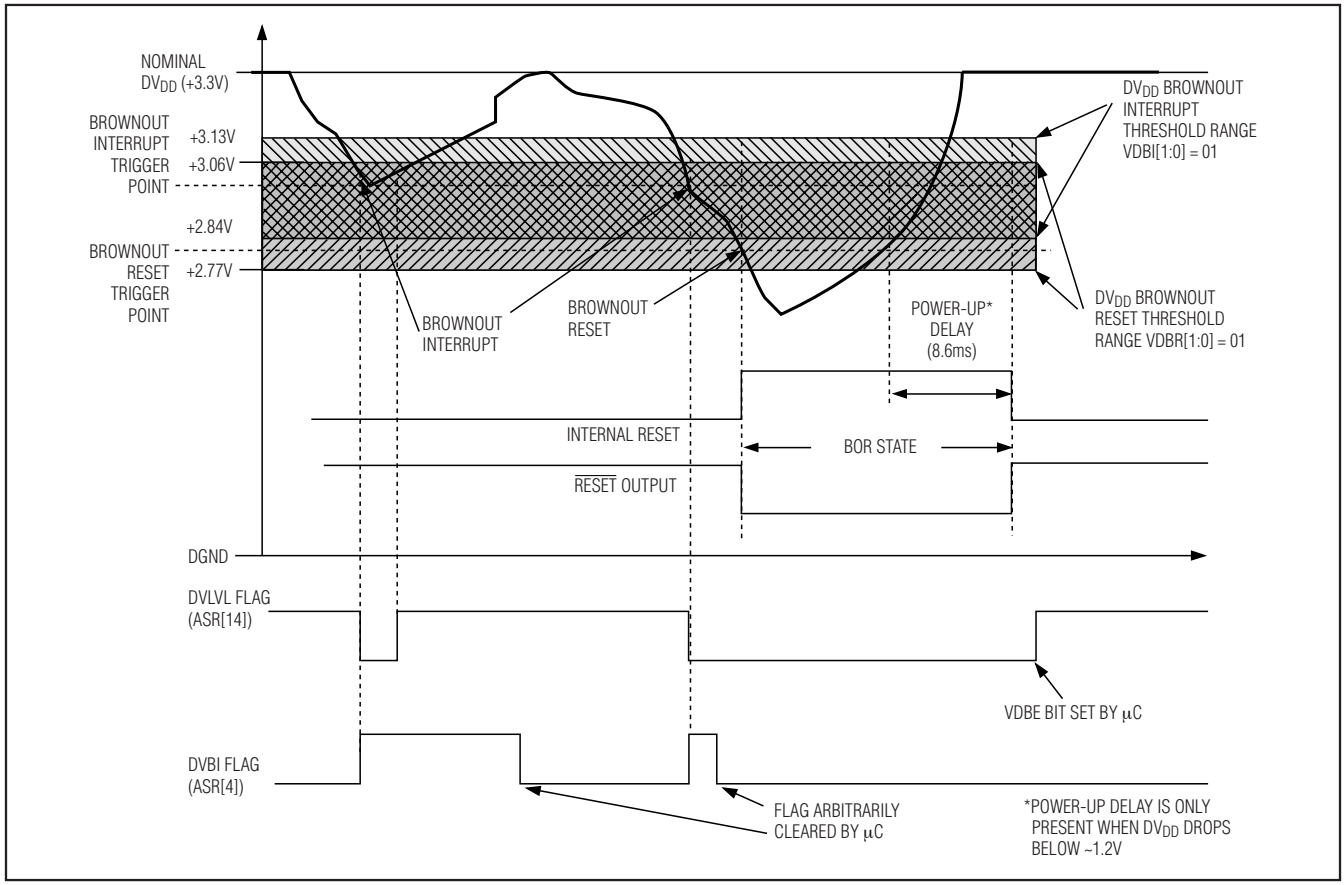


Figure 5. DV_{DD} Brownout Interrupt Detection

During power-up, $\overline{RESET}$ is held low once DV_{DD} rises above +1.0V. All internal register bits are set to their default, POR state after DV_{DD} exceeds a threshold of approximately +1.2V. This includes the VDBR bits which reset to 00b, resulting in a default, DV_{DD} brownout reset (BOR) threshold in the +2.7V to +2.99V range following POR. Once DV_{DD} rises above this DV_{DD} brownout threshold, the 7.6MHz RC oscillator starts driving the power-up counter, and 8.6ms (typ) later, the $\overline{RESET}$ pin is released and allowed to go high if nothing external is holding it low. An important system-design consideration at power-up is the DV_{DD} ramp-up rate should be at least 35mV/ms between +2.7V and +3.0V. This ensures $\overline{RESET}$ is not released before DV_{DD} reaches a minimum flash operating level of +3.0V. After DV_{DD} has reached a valid level and $\overline{RESET}$ is released, the µC jumps to the reset vector (8000h in the utility ROM), and the desired BOI and BOR threshold values can be set by the user through the VIOBI, VDBI, and VDBR bits.

If a valid DV_{DD} drops below its BOI threshold (set by the VDBI bits), an interrupt is generated. This offers the possibility of limited software cleanup before the DV_{DD} BOR occurs. The amount of cleanup time depends on the VDBI and VDBR brownout threshold bit settings, the size of the DV_{DD} bypass capacitors, and the application-dependent, µC power management and software cleanup tasks. Note that if the internal, +3.3V linear regulator is being used to provide DV_{DD}, additional software cleanup time is possible by using the DV_{DDIO} brownout monitor as an early warning that the regulator's DV_{DDIO} (+5V) input voltage is falling, and its DV_{DD} (+3.3V) will subsequently drop (unless DV_{DDIO} recovers).

As DV_{DD} continues to fall below the DV_{DD} BOR threshold set by the VDBR bits, the $\overline{RESET}$ pin is pulled low, µC and peripheral activity stops, and most, but not all of the register bits are set to their default state. This includes the VDBR bits, which retain their value if DV_{DD} falls below the BOR threshold, but not below the POR threshold.

Once DV_{DD} has entered BOR, there are a few possible scenarios:

- If DV_{DD} remains below the BOR threshold, the $\overline{RESET}$ pin remains low, and the µC remains in the reset state.
- If DV_{DD} stops falling before reaching the POR threshold, then begins rising above the BOR threshold, the $\overline{RESET}$ pin is released, and the µC jumps to the reset vector (8000h in the utility ROM). This is similar to the DV_{DD} power-up case described in the previous scenario, except there is no power-up counter delay and some of the register bits are set to BOR values rather than POR values. See Tables 3 and 5 for the reset behavior of specific bits. In particular, the retained VDBR setting, if higher than the default value of 00b, allows a potentially more robust brownout recovery closer to or above the minimum flash operating level of +3.0V.
- If DV_{DD} falls below the 1.2V POR threshold, all register bits are reset, and any DV_{DD} recovery from that point is identical to the power-up case described above. See Tables 3 and 5 for reset behavior of specific bits.

Refer to the *MAXQ7665/MAXQ7666 User's Guide* for detailed programming information, and a more thorough description of POR and brownout behavior.

Internal 3.3V Linear Regulator

The MAXQ7665A–MAXQ7665D core logic supply, DV_{DD}, can be supplied by a 3.3V external supply or the on-chip 3.3V, 50mA linear regulator. To use the on-chip linear regulator, ensure the DV_{DDIO} supply can support a load of approximately 50mA and connect digital input $\overline{REGEN}$ to GNDIO. If using an external supply, connect the regulated 3.3V supply to DV_{DD} and connect digital input $\overline{REGEN}$ to DV_{DDIO}. If the linear regulator is not used, bring up DV_{DDIO} before DV_{DD}.

System Clock Generator

The MAXQ7665A–MAXQ7665D oscillator module is the master clock generator that supplies the system clock for the µC core and all of the peripheral modules. The high-frequency (HF) oscillator is designed to operate with an 8MHz crystal. Alternatively, the on-chip RC oscillator can be used in applications that do not require precise timing. Due to its RISC design, the MAXQ7665A–MAXQ7665D execute most instructions in a single SYSCLK period. The oscillator module contains all of the primary clock-generation circuitry. Figure 6 shows a block diagram of the system clock module.

The MAXQ7665A–MAXQ7665D contain many features for generating a master clock signal timing source:

- Internal, fast-starting, 7.6MHz RC oscillator eliminates external crystal
- Internal high-frequency oscillator that can drive an external 8MHz crystal
- External high-frequency clock input (8MHz)
- Selectable internal capacitors for HF crystal oscillator
- Power-up timer
- Power-saving management modes
- Fail-safe modes

Watchdog Timer

The watchdog timer serves as a time-base generator, an event timer, or a system supervisor. The primary function of the watchdog timer is to supervise software execution, watching for stalled or stuck software. The watchdog timer performs a controlled system restart when the µP fails to write to the watchdog timer register before a selectable timeout interval expires. In some designs, the watchdog timer is also used to implement a real-time operating system (RTOS) in the µC. When used to implement an RTOS, a watchdog timer typically has four objectives:

1) To detect if a system is operating normally
2) To detect an infinite loop in any of the tasks
3) To detect an arbitration deadlock involving two or more tasks
4) To detect if some lower priority tasks are not getting to run because of higher priority tasks

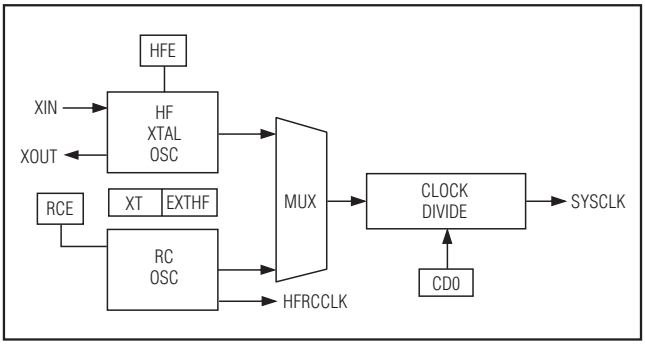


Figure 6. High-Frequency and RC Oscillator Block Diagram

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As illustrated in Figure 7, the high-frequency internal RC oscillator (HFRCCLK) drives the watchdog timer through a series of dividers. The divider output is programmable and determines the timeout interval. When enabled, the interrupt flag WDIF is set when a timeout is reached. A system reset then occurs after a time delay (based on the divider ratio).

The watchdog timer functions as the source of both the watchdog interrupt and the watchdog reset. The interrupt timeout has a default divide ratio of 2^{12} of the HFRCCLK, with the watchdog reset set to timeout 2^9 clock cycles later. With the nominal RC oscillator value of 7.6MHz, an interrupt timeout occurs every 539µs, followed by a watchdog reset 67.4µs later. The watchdog timer is reset to the default divide ratio following any reset. Using the WD0 and WD1 bits in the WDCN register, other divide ratios can be selected for longer watchdog interrupt periods. If the WD[1:0] bits are changed before the watchdog interrupt timeout occurs (i.e. before the watchdog reset counter begins), the watchdog timer count is reset. All watchdog timer reset timeouts follow the programmed interrupt timeout 512 source clock cycles later. For more information on the MAXQ7665A–MAXQ7665D watchdog timer, refer to the *MAXQ7665/MAXQ7666 User's Guide.*

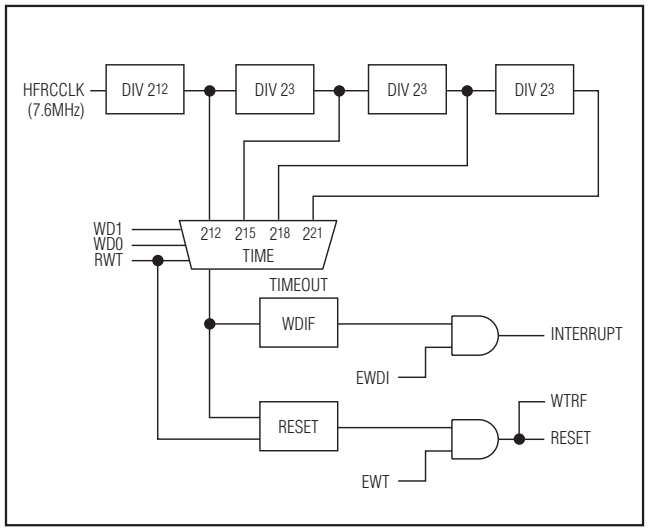

Figure 7. Watchdog Functional Diagram

Timer and PWM

The MAXQ7665A–MAXQ7665D include three 16-bit timer channels. Each timer is a type 2 timer implemented in the MAXQ family (see Figure 8). Two of the timers are accessible through I/Os, and one is accessible only through software. Type 2 timers are auto-reload 16-bit timers/counters offering the following functions:

- 8-bit/16-bit timer/counter
- Up/down auto-reload
- Counter function of external pulse
- Capture
- Compare

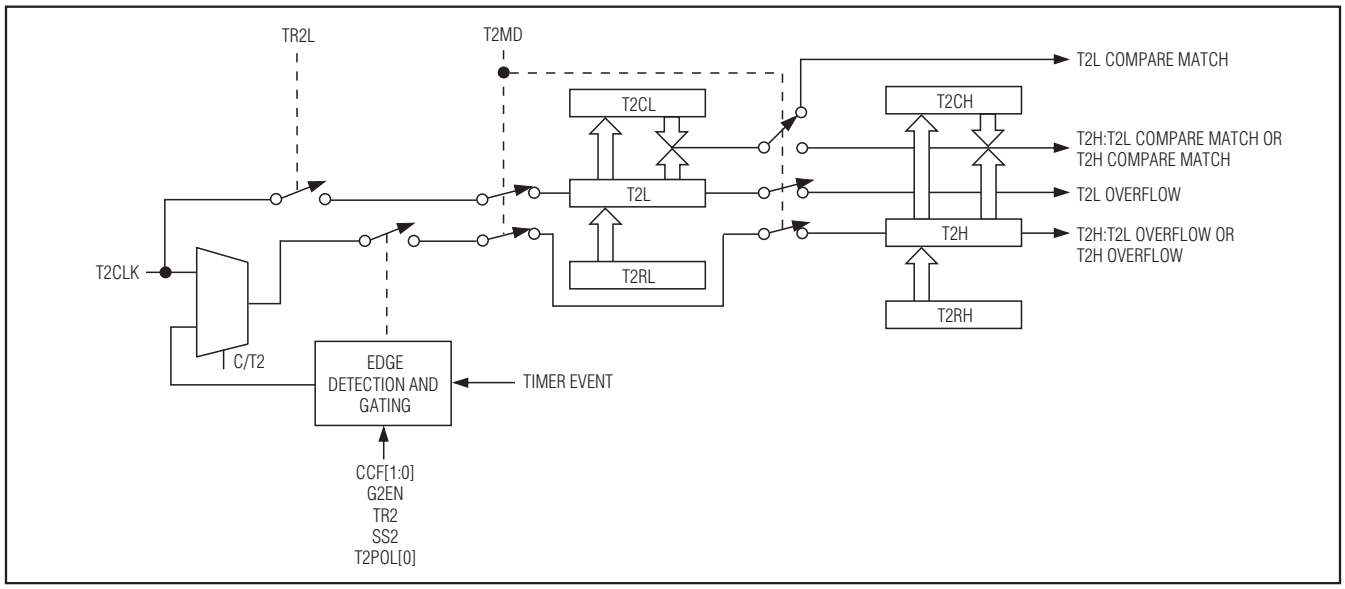

Figure 8. Type 2 Timer Functional Diagram

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CAN Functional Description

The basic functions covered by the CAN controller include the use of 11-bit standard or 29-bit extended acceptance identifiers, as programmed by the µC for each message center, as shown in Figure 10. The CAN unit provides storage for up to 15 messages, with the standard 8-byte data field, in each message.

Each of the first 14 message centers is programmable in either transmit or receive mode. Message center 15 is designed as a receive-only message center with a buffer FIFO arrangement to help prevent the inadvertent loss of data when the µC is busy and is not allowed time to retrieve the incoming message prior to the acceptance of a second message into message center 15. Message center 15 also utilizes an independent set of mask registers and identification registers, which are only applied once an incoming message has not been accepted by any of the first 14 message centers. A second filter test is also supported for all message centers (1–15) to allow the CAN controller to use two separate 8-bit media masks and media arbitration fields to verify the contents of the first 2 bytes of data of

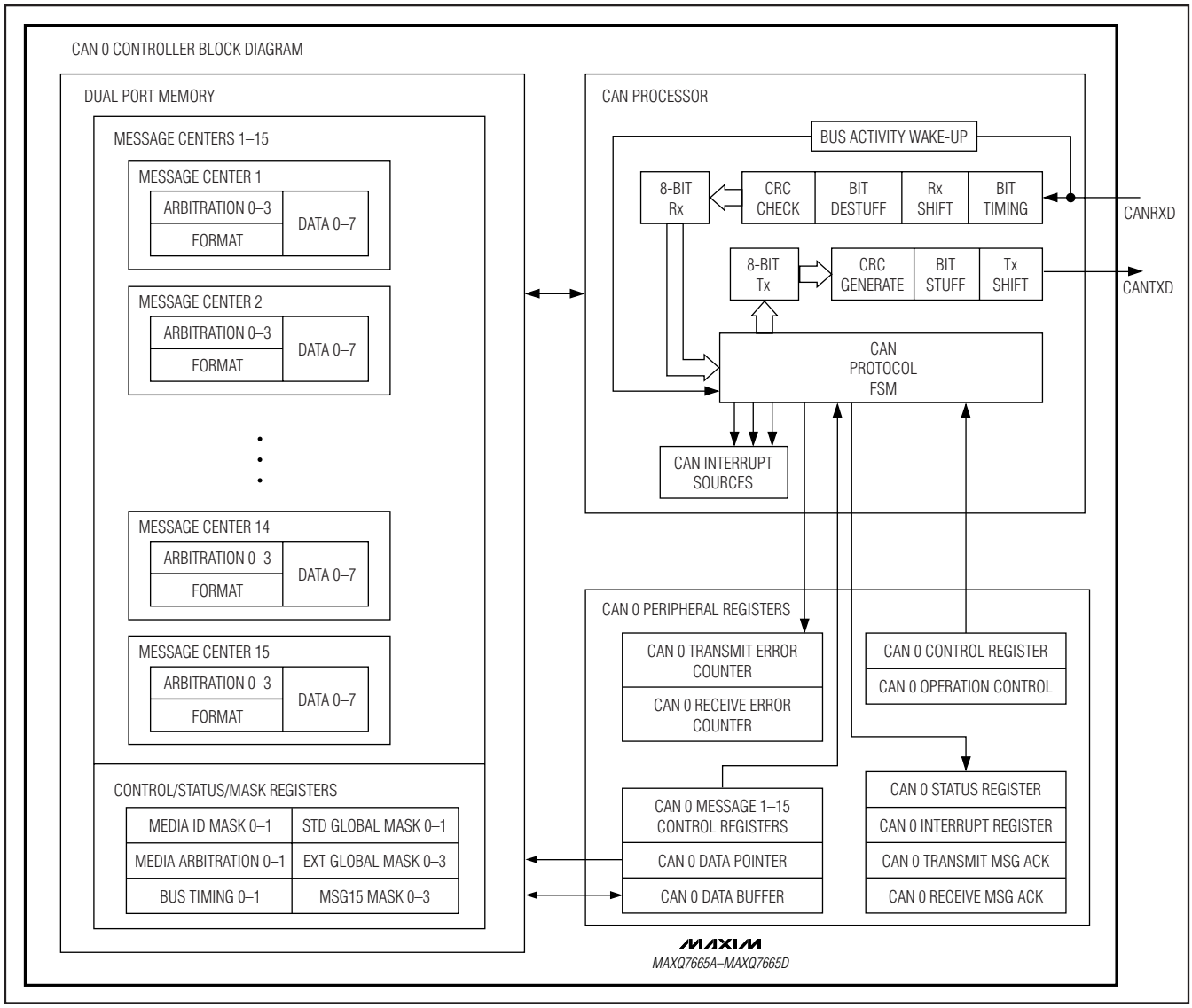

Figure 10. CAN 0 Controller Block Diagram

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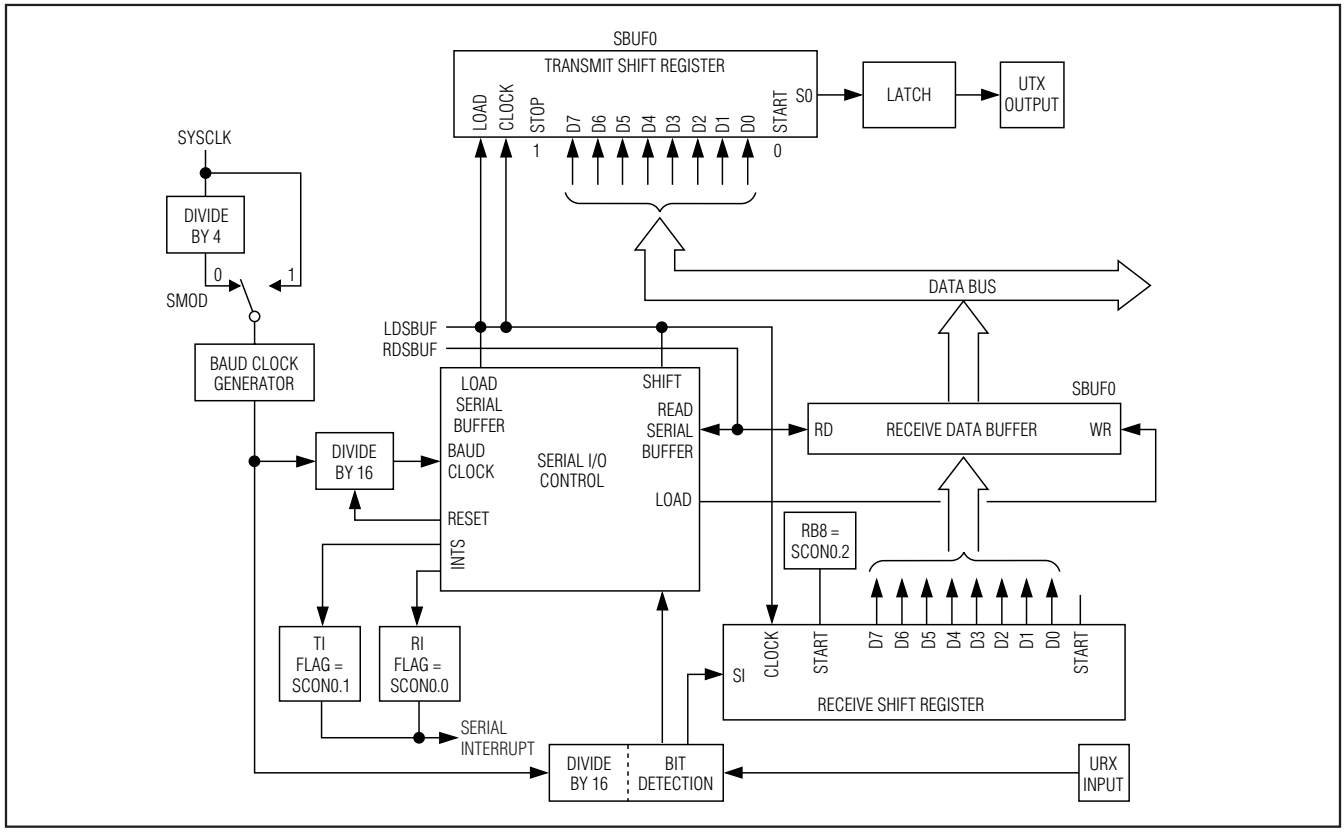

Figure 11b. UART Asynchronous Mode (Mode 1)

detection. Table 1 summarizes the operating characteristics as well as the maximum baud rate of each mode.

JTAG Interface Bus

The joint test action group (JTAG) IEEE 1149.1 standard defines a unique method for in-circuit testing and programming. The MAXQ7665A–MAXQ7665D conform to this standard, implementing an external test access port (TAP) and internal TAP controller for communication with a JTAG bus master, such as an automatic test equipment (ATE) system. For detailed information on the TAP and TAP controller, refer to *IEEE Standard 1149.1* on the IEEE website at http://standards.ieee.org. The JTAG on the MAXQ7665A–MAXQ7665D is used for in-circuit emulation and debug support, but does not support boundary scan test capability.

The TAP controller communicates synchronously with the host system (bus master) through four digital I/O pins: test mode select (TMS), test clock (TCK), test data input (TDI), and test data output (TDO). The internal TAP module consists of several shift registers and a

Table 1. Operating Characteristics and Mode Baud Rate

MODE	TYPE	BAUD CLOCK	START BITS	DATA BITS	STOP BITS	MAX BAUD RATE AT 8MHz
Mode 0	Synchronous	4 or 12 clock	N/A	8	N/A	2Mbps
Mode 1	Asynchronous	Baud generation	1	8	1	250kbps
Mode 2	Asynchronous	32 or 64 clock	1	8 + 1	1	250kbps
Mode 3	Asynchronous	Baud generation	1	8 + 1	1	250kbps

the host to the internal TAP module shift registers. Data is transferred LSB first.

- TCK—Serial clock for the test logic.
- TMS—Test mode selection. Test signals received at TMS are sampled at the rising edge of TCK and decoded by the TAP controller to control the test operation.

General-Purpose Digital I/Os

The MAXQ7665A–MAXQ7665D provide eight general-purpose digital I/Os (GPIOs). All GPIOs have an additional special function (SF), such as a timer input/output, or TAP signal for JTAG communication. For example, the state of pin P0.6/T0 can be programmed to depend on timer channel 0 logic. When programmed as a port, each I/O is configurable for high-impedance or weak pullup to DV_{DDIO}. At power-up, each GPIO is configured as an input with pullups to DV_{DDIO}. Note that at power-up, the JTAG function is enabled and should be turned off before normal operation. In addition, each GPIO can be programmed to cause an interrupt (on falling or rising edges). In stop mode, any interrupt can be used to wake up the device.

The data input/output direction in a port is independently controlled by the port direction register (PD). Each I/O within the port can be individually set as an output or input. The port output register (PO) contains the current state of the logic output buffers. When an I/O is configured as an output, writing to the PO register controls the output logic state. Reading the PO register shows the current state of the output buffers, independent of the data direction. The port input register (PI) is a read-only register that always reflects the logic state of the I/Os. When an I/O is configured as an input, writing to the PO register enables/disables the pull-up resistor. Refer to the *MAXQ7665/MAXQ7666 User's Guide* for more detailed information.

Port Characteristics

The MAXQ7665A–MAXQ7665D contain only one port (P0). It is a bidirectional 8-bit I/O port, which contains the following features:

- Schmitt trigger input circuitry with software-selectable high-impedance or weak pullup to DV_{DDIO}
- Software-selectable push-pull CMOS output drivers capable of sinking and sourcing 1.6mA
- Software-selectable open-drain output drivers capable of sinking 1.6mA
- Falling or rising edge interrupt capability
- All I/Os contain an additional special function, such as a logic input/output for a timer channel. Selecting an I/O for a special function alters the port characteristics of that I/O (refer to the *MAXQ7665/MAXQ7666 User's Guide* for more details). Figure 13 illustrates the functional blocks of an I/O.

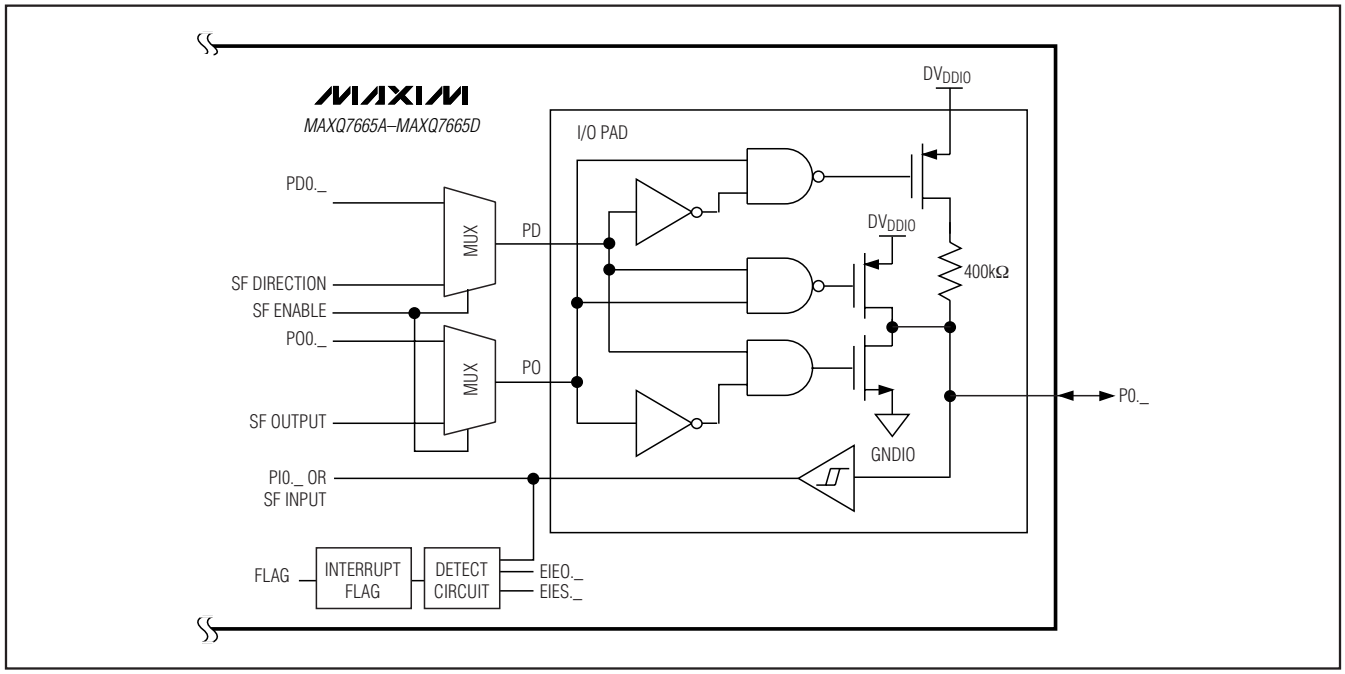

Figure 13. Digital I/O Circuitry

Power Management

Power consumption reaches its minimum in stop mode. In this mode, the external oscillator, internal RC oscillator, system clock, and all processing activity is halted. Stop mode is exited when an enabled external interrupt input is triggered or an external reset signal is applied to $\overline{\text{RESET}}$. Upon exiting stop mode, the µC can choose to wait for the external high-frequency crystal to complete its warmup period, or it can start execution immediately from its internal RC oscillator while the warmup period completes.

Table 2. System Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)						
	AP (8h)	**A (9h)**	**PFX (Bh)**	**IP (Ch)**	**SP (Dh)**	**DPC (Eh)**	**DP (Fh)**
0h	AP	**A[0]**	**PFX[0]**	**IP**	—	—	—
1h	APC	**A[1]**	**PFX[1]**	—	**SP**	—	—
2h	—	**A[2]**	**PFX[2]**	—	**IV**	—	—
3h	—	**A[3]**	**PFX[3]**	—	—	OFFS	**DP0**
4h	PSF	**A[4]**	**PFX[4]**	—	—	**DPC**	—
5h	IC	**A[5]**	**PFX[5]**	—	—	**GR**	—
6h	IMR	**A[6]**	**PFX[6]**	—	**LC0**	GRL	—
7h	—	**A[7]**	**PFX[7]**	—	**LC1**	**BP**	**DP1**
8h	SC	**A[8]**		—	—	***GRS***	—
9h	—	**A[9]**	—	—	—	GRH	—
Ah	—	**A[10]**	—	—	—	***GRXL***	—
Bh	*IIR*	**A[11]**	—	—	—	***FP***	—
Ch	—	**A[12]**	—	—	—	—	—
Dh	—	**A[13]**	—	—	—	—	—
Eh	CKCN	**A[14]**	—	—	—	—	—
Fh	WDCN	**A[15]**	—	—	—	—	—

Note: Names that appear in italics indicate that all bits of a register are read-only. Names that appear in bold indicate that a register is 16 bits wide.

Table 5. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTERED BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T2RH0	—	—	—	—	—	—	—	—	T2RH0.7	T2RH0.6	T2RH0.5	T2RH0.4	T2RH0.3	T2RH0.2	T2RH0.1	T2RH0.0
(M2, 2h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CH0	—	—	—	—	—	—	—	—	T2CH0.7	T2CH0.6	T2CH0.5	T2CH0.4	T2CH0.3	T2CH0.2	T2CH0.1	T2CH0.0
(M2, 3h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNA1	—	—	—	—	—	—	—	—	ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
(M2, 4h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2H1	—	—	—	—	—	—	—	—	T2H1.7	T2H1.6	T2H1.5	T2H1.4	T2H1.3	T2H1.2	T2H1.1	T2H1.0
(M2, 5h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2RH1	—	—	—	—	—	—	—	—	T2RH1.7	T2RH1.6	T2RH1.5	T2RH1.4	T2RH1.3	T2RH1.2	T2RH1.1	T2RH1.0
(M2, 6h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CH1	—	—	—	—	—	—	—	—	T2CH1.7	T2CH1.6	T2CH1.5	T2CH1.4	T2CH1.3	T2CH1.2	T2CH1.1	T2CH1.0
(M2, 7h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNB0	—	—	—	—	—	—	—	—	ET2L	—	—	—	TF2	TF2L	TCC2	TC2L
(M2, 8h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2V0	T2V0.15	T2V0.14	T2V0.13	T2V0.12	T2V0.11	T2V0.10	T2V0.9	T2V0.8	T2V0.7	T2V0.6	T2V0.5	T2V0.4	T2V0.3	T2V0.2	T2V0.1	T2V0.0
(M2, 9h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R0	T2R0.15	T2R0.14	T2R0.13	T2R0.12	T2R0.11	T2R0.10	T2R0.9	T2R0.8	T2R0.7	T2R0.6	T2R0.5	T2R0.4	T2R0.3	T2R0.2	T2R0.1	T2R0.0
(M2, Ah)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C0	T2C0.15	T2C0.14	T2C0.13	T2C0.12	T2C0.11	T2C0.10	T2C0.9	T2C0.8	T2C0.7	T2C0.6	T2C0.5	T2C0.4	T2C0.3	T2C0.2	T2C0.1	T2C0.0
(M2, Bh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNB1	—	—	—	—	—	—	—	—	ET2L	—	—	—	TF2	TF2L	TCC2	TC2L
(M2, Ch)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2V1	T2V1.15	T2V1.14	T2V1.13	T2V1.12	T2V1.11	T2V1.10	T2V1.9	T2V1.8	T2V1.7	T2V1.6	T2V1.5	T2V1.4	T2V1.3	T2V1.2	T2V1.1	T2V1.0
(M2, Dh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R1	T2R1.15	T2R1.14	T2R1.13	T2R1.12	T2R1.11	T2R1.10	T2R1.9	T2R1.8	T2R1.7	T2R1.6	T2R1.5	T2R1.4	T2R1.3	T2R1.2	T2R1.1	T2R1.0
(M2, Eh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C1	T2C1.15	T2C1.14	T2C1.13	T2C1.12	T2C1.11	T2C1.10	T2C1.9	T2C1.8	T2C1.7	T2C1.6	T2C1.5	T2C1.4	T2C1.3	T2C1.2	T2C1.1	T2C1.0
(M2, Fh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG0	—	—	—	—	—	—	—	—	—	T2DIV2	T2DIV1	T2DIV0	T2MD	CCF1	CCF0	C/T2
(M2, 10h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG1	—	—	—	—	—	—	—	—	—	T2DIV2	T2DIV1	T2DIV0	T2MD	CCF1	CCF0	C/T2
(M2, 11b)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDT0	ICDT0.15	ICDT0.14	ICDT0.13	ICDT0.12	ICDT0.11	ICDT0.10	ICDT0.9	ICDT0.8	ICDT0.7	ICDT0.6	ICDT0.5	ICDT0.4	ICDT0.3	ICDT0.2	ICDT0.1	ICDT0.0
(M2, 18h)	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB
ICDT1	ICDT1.15	ICDT1.14	ICDT1.13	ICDT1.12	ICDT1.11	ICDT1.10	ICDT1.9	ICDT1.8	ICDT1.7	ICDT1.6	ICDT1.5	ICDT1.4	ICDT1.3	ICDT1.2	ICDT1.1	ICDT1.0
(M2, 19h)	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB
ICDC	—	—	—	—	—	—	—	—	DME	—	REGE	—	CMD3	CMD2	CMD1	CMD0
(M2, 1Ah)	0	0	0	0	0	0	0	0	DW	0	DW	0	DW	DW	DW	DW
ICDF	—	—	—	—	—	—	—	—	—	—	—	—	PSS1	PSS0	SPE	TXC
(M2, 1Bh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDB	—	—	—	—	—	—	—	—	ICDB.7	ICDB.6	ICDB.5	ICDB.4	ICDB.3	ICDB.2	ICDB.1	ICDB.0
(M2, 1Ch)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDA	ICDA.15	ICDA.14	ICDA.13	ICDA.12	ICDA.11	ICDA.10	ICDA.9	ICDA.8	ICDA.7	ICDA.6	ICDA.5	ICDA.4	ICDA.3	ICDA.2	ICDA.1	ICDA.0
M2, 1Dh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDD	ICDD.15	ICDD.14	ICDD.13	ICDD.12	ICDD.11	ICDD.10	ICDD.9	ICDD.8	ICDD.7	ICDD.6	ICDD.5	ICDD.4	ICDD.3	ICDD.2	ICDD.1	ICDD.0
(M2, 1Eh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNA2	—	—	—	—	—	—	—	—	ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
(M3, 0h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2H2	—	—	—	—	—	—	—	—	T2H2.7	T2H2.6	T2H2.5	T2H2.4	T2H2.3	T2H2.2	T2H2.1	T2H2.0
(M3, 1h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2RH2	—	—	—	—	—	—	—	—	T2RH2.7	T2RH2.6	T2RH2.5	T2RH2.4	T2RH2.3	T2RH2.2	T2RH2.1	T2RH2.0
(M3, 2h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CH2	—	—	—	—	—	—	—	—	T2CH2.7	T2CH2.6	T2CH2.5	T2CH2.4	T2CH2.3	T2CH2.2	T2CH2.1	T2CH2.0
(M3, 3h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
T2CNB2 (M3, 8h)	—	—	—	—	—	—	—	—	ET2L	—	—	—	TF2	TF2L	TCC2	TC2L
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2V2 (M3, 9h)	T2V2.15	T2V2.14	T2V2.13	T2V2.12	T2V2.11	T2V2.10	T2V2.9	T2V2.8	T2V2.7	T2V2.6	T2V2.5	T2V2.4	T2V2.3	T2V2.2	T2V2.1	T2V2.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R2 (M3, Ah)	T2R2.15	T2R2.14	T2R2.13	T2R2.12	T2R2.11	T2R2.10	T2R2.9	T2R2.8	T2R2.7	T2R2.6	T2R2.5	T2R2.4	T2R2.3	T2R2.2	T2R2.1	T2R2.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C2 (M3, Dh)	T2C2.15	T2C2.14	T2C2.13	T2C2.12	T2C2.11	T2C2.10	T2C2.9	T2C2.8	T2C2.7	T2C2.6	T2C2.5	T2C2.4	T2C2.3	T2C2.2	T2C2.1	T2C2.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG2 (M3, 10h)	—	—	—	—	—	—	—	—	—	T2DIV2	T2DIV1	T2DIV0	T2MD	CCF1	CCF0	C/T2
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0C (M4, 0h)	—	—	—	—	—	—	—	—	ERIE	STIE	PDE	SIESTA	CRST	AUTOB	ERCS	SWINT
	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
C0S (M4, 1h)	—	—	—	—	—	—	—	—	BSS	EC96/128	WKS	RXS	TXS	ER2	ER1	ER0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0IR (M4, 2h)	—	—	—	—	—	—	—	—	INTIN7	INTIN6	INTIN5	INTIN4	INTIN3	INTIN2	INTIN1	INTIN0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0TE (M4, 3h)	—	—	—	—	—	—	—	—	C0TE.7	C0TE.6	C0TE.5	C0TE.4	C0TE.3	C0TE.2	C0TE.1	C0TE.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0RE (M4, 4h)	—	—	—	—	—	—	—	—	C0RE.7	C0RE.6	C0RE.5	C0RE.4	C0RE.3	C0RE.2	C0RE.1	C0RE.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0R (M4, 5h)	—	—	—	—	—	—	—	—	CAN0BA	INCDEC	AID	C0BPR7	C0BPR6	—	C0BIE	C0IE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0DP (M4, 6h)	C0DP.15	C0DP.14	C0DP.13	C0DP.12	C0DP.11	C0DP.10	C0DP.9	C0DP.8	C0DP.7	C0DP.6	C0DP.5	C0DP.4	C0DP.3	C0DP.2	C0DP.1	C0DP.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0DB (M4, 7h)	C0DB.15	C0DB.14	C0DB.13	C0DB.12	C0DB.11	C0DB.10	C0DB.9	C0DB.8	C0DB.7	C0DB.6	C0DB.5	C0DB.4	C0DB.3	C0DB.2	C0DB.1	C0DB.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0RMS (M4, 8h)	—	C0RMS.15	C0RMS.14	C0RMS.13	C0RMS.12	C0RMS.11	C0RMS.10	C0RMS.9	C0RMS.8	C0RMS.7	C0RMS.6	C0RMS.5	C0RMS.4	C0RMS.3	C0RMS.2	C0RMS.1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0TMA (M4, 9h)	—	C0TMA.15	C0TMA.14	C0TMA.13	C0TMA.12	C0TMA.11	C0TMA.10	C0TMA.9	C0TMA.8	C0TMA.7	C0TMA.6	C0TMA.5	C0TMA.4	C0TMA.3	C0TMA.2	C0TMA.1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M1C (M4, 11h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M2C (M4, 12h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M3C (M4, 13h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M4C (M4, 14h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M5C (M4, 15h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M6C (M4, 16h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M7C (M4, 17h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M8C (M4, 18h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M9C (M4, 19h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M10C (M4, 1Ah)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M11C (M4, 1Bh)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M12C (M4, 1Ch)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M13C (M4, 1Dh)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C0M14C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
(M4, 1Eh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M15C	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
(M4, 1Fh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VMC	—	—	—	—	—	—	—	—	—	—	VIOBI1	VIOBI0	VDBI1	VDBI0	VDBR1	VDBR0
(M5, 0h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S	S
APE	—	—	—	VIBE	VDBE	VDPE	—	—	PGG2	PGG1	PGG0	TSE	PGAE	—	DACE	ADCE
(M5, 1h)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
ACNT	ADCMX4	ADCMX3	ADCMX2	ADCMX1	ADCMX0	ADCDIF	ADCBIP	—	—	ADCDUL	—	ADCASD	ADCBY	ADCS2	ADCS1	ADCS0
(M5, 2h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DCNT	—	—	—	—	—	—	—	—	—	DACLD2	DACLD1	DACLD0	—	—	—	—
(M5, 3h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DACI	—	—	—	—	DACI.11	DACI.10	DACI.9	DACI.8	DACI.7	DACI.6	DACI.5	DACI.4	DACI.3	DACI.2	DACI.1	DACI.0
(M5, 4h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DACO	—	—	—	—	DACO.11	DACO.10	DACO.9	DACO.8	DACO.7	DACO.6	DACO.5	DACO.4	DACO.3	DACO.2	DACO.1	DACO.0
(M5, 6h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADCD	—	—	—	—	ADCD.11	ADCD.10	ADCD.9	ADCD.8	ADCD.7	ADCD.6	ADCD.5	ADCD.4	ADCD.3	ADCD.2	ADCD.1	ADCD.0
(M5, 8h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TSO	TSO.15	TSO.14	TSO.13	TSO.12	TSO.11	TSO.10	TSO.9	TSO.8	TSO.7	TSO.6	TSO.5	TSO.4	TSO.3	TSO.2	TSO.1	TSO.0
(M5, 9h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AIE	—	—	—	—	—	—	—	—	—	HFFIE	VIOBIE	DVBIE	—	AORIE	ADCIE	—
(M5, Ah)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
ASR	VIOLVL	DVLVL	—	—	XHFRY	—	—	—	—	HFFINT	VIOBI	DVBI	—	ADCOV	ADCRY	—
(M5, Bh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OSCC	—	—	—	—	HFOC1	HFOC0	HFIC1	HFIC0	ADCCD2	ADCCD1	ADCCD0	—	—	EXTHF	RCE	HFE
(M5, Ch)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits indicated by "—" are unused.

Bits indicated by "ST" reflect the input signal state.

Bits indicated by "S" are only affected by a POR and not by other forms of reset. These bits are set to 0 after a POR.

Bits indicated by "DB" have read/write access only in background or debug mode. These bits are cleared after a POR.

Bits indicated by "DW" are only written to in debug mode. These bits are cleared after a POR.

The OSCC register is cleared to 0002h after a POR and is not affected by other forms of reset.

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

Ordering Information

PART	PIN-PACKAGE	FLASH SIZE (KB)
MAXQ7665AATM+**	48 TQFN-EP*	128 (64K x 16)
MAXQ7665BATM+	48 TQFN-EP*	64 (32K x 16)
MAXQ7665CATM+**	48 TQFN-EP*	48 (24K x 16)
MAXQ7665DATM+**	48 TQFN-EP*	32 (16K x 16)

+Devices are only available in lead(Pb)-free packaging.

**EP = Exposed pad.*

***Future Product—contact factory for availability.*

Note: *All devices are specified for operation over the -40°C to +125°C automotive temperature range.*

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFN-EP	T4877MK+6	**21-0199**