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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg321f32g-a-qfp48r

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG321 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32HG321F32G-B-QFP48	32	8	25	1.98 - 3.8	-40 - 85	TQFP48
EFM32HG321F64G-B-QFP48	64	8	25	1.98 - 3.8	-40 - 85	TQFP48

Adding the suffix 'R' to the part number (e.g. EFM32HG321F32G-B-QFP48R) denotes tape and reel.

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divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32HG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32HG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32HG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Low Energy USB

The unique Low Energy USB peripheral provides a full-speed USB 2.0 compliant device controller and PHY with ultra-low current consumption. The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation, and includes a dedicated USB oscillator with clock recovery mechanism for crystal-free operation. No external components are required. The Low Energy Mode ensures the current consumption is optimized and enables USB communication on a strict power budget. The USB device includes an internal dedicated descriptor-based Scatter/Gather DMA and supports up to 3 OUT endpoints and 3 IN endpoints, in addition to endpoint 0. The on-chip PHY includes software controllable pull-up and pull-down resistors.

2.1.19 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.20 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

2.1.21 Current Digital to Analog Converter (IDAC)

The current digital to analog converter can source or sink a configurable constant current, which can be output on, or sinked from pin or ADC. The current is configurable with several ranges of various step sizes.

2.1.22 General Purpose Input/Output (GPIO)

In the EFM32HG321, there are 35 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32HG321 is a subset of the feature set described in the EFM32HG Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO,
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
USB	Full configuration	USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA and I2S	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration with I2S and IrDA	US1_TX, US1_RX, US1_CLK, US1_CS

3.4 Current Consumption

Table 3.3. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash.	24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		148	158	µA/MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		153	163	µA/MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		161	172	µA/MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		163	174	µA/MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		127	137	µA/MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		129	139	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		131	140	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		134	143	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		134	143	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		137	145	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		136	144	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		139	148	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		142	150	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		146	154	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		184	196	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		194	208	µA/MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM1}	EM1 current	24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		64	68	µA/ MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		67	71	µA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		85	91	µA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		86	92	µA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		51	55	µA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		52	56	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		53	57	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		54	58	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		56	59	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		57	61	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		58	61	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		59	63	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		64	68	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		67	71	µA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		106	114	µA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		114	126	µA/ MHz
I_{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25°C		0.9	1.35	µA

Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz

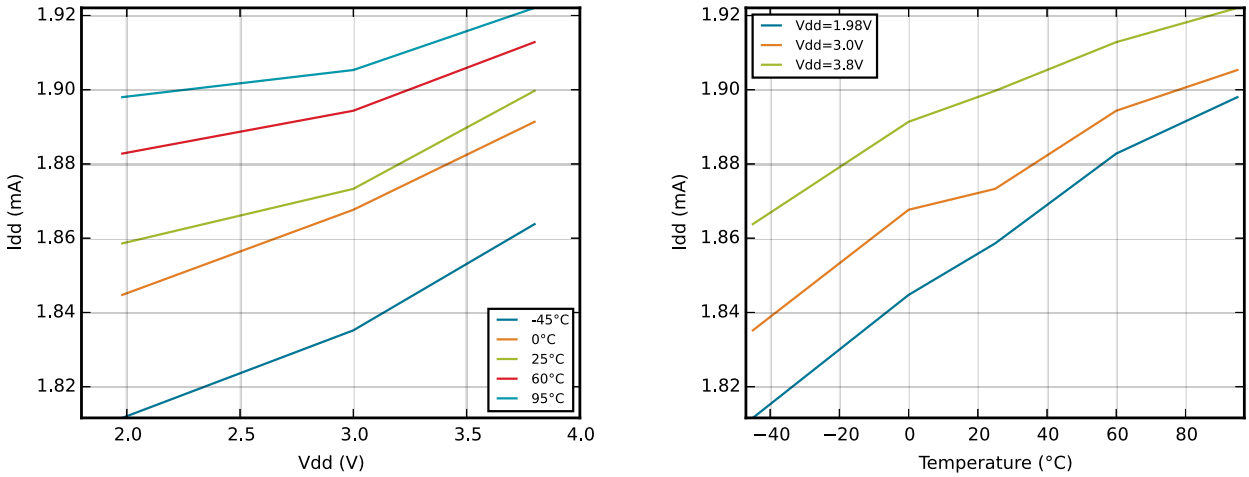


Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz

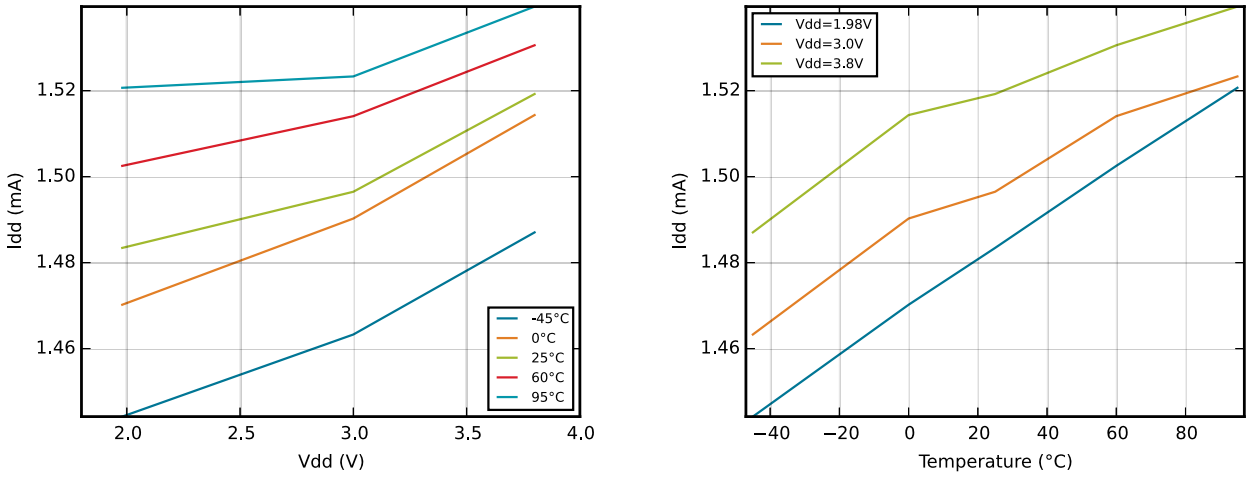
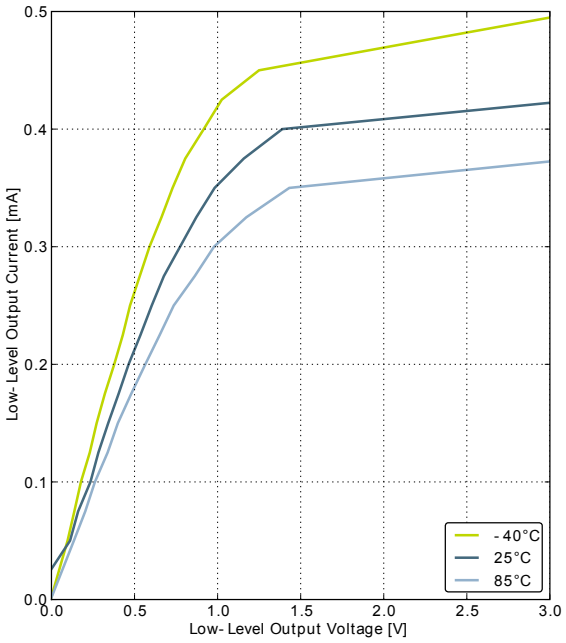
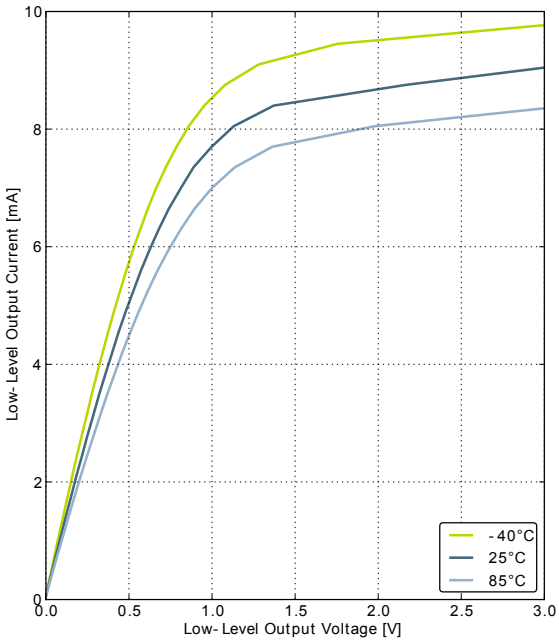


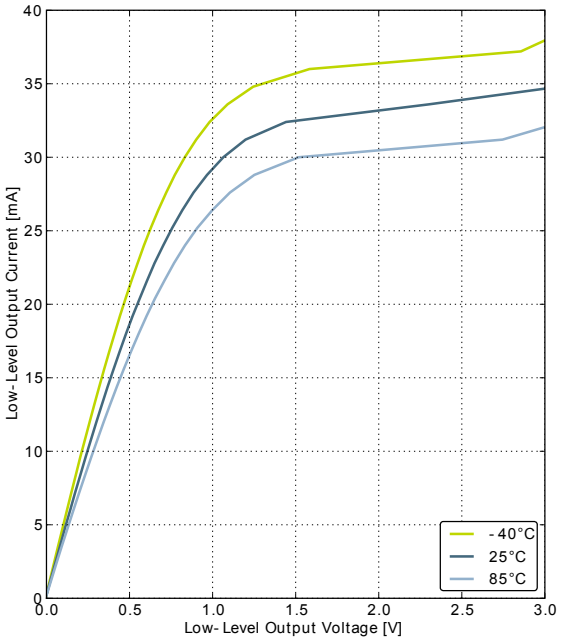
Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage



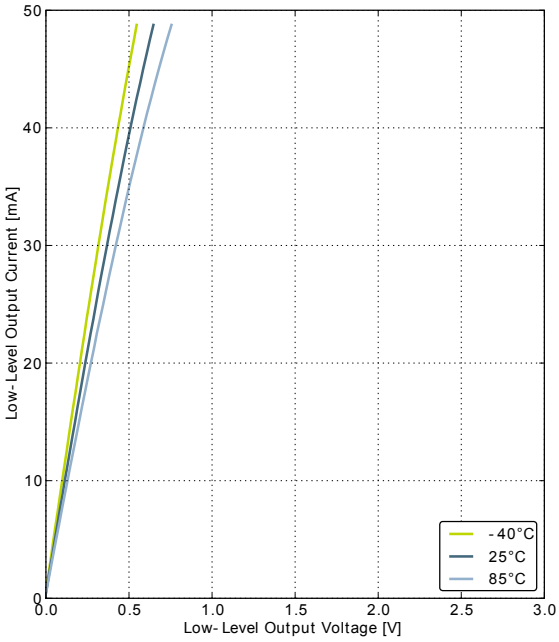
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

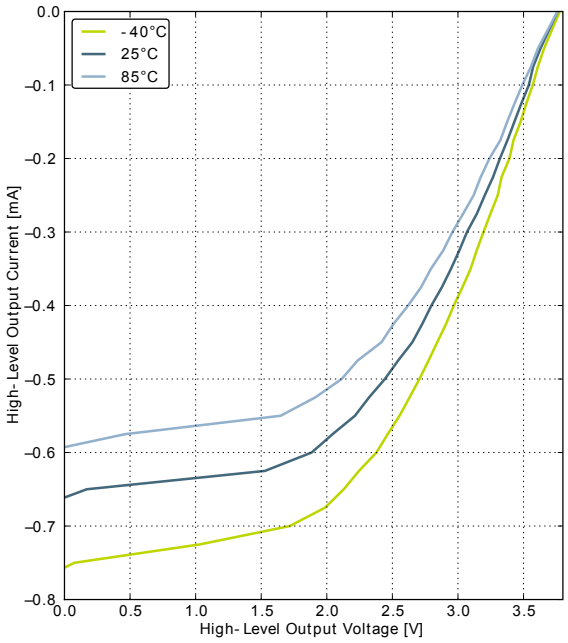


GPIO_Px_CTRL DRIVEMODE = STANDARD

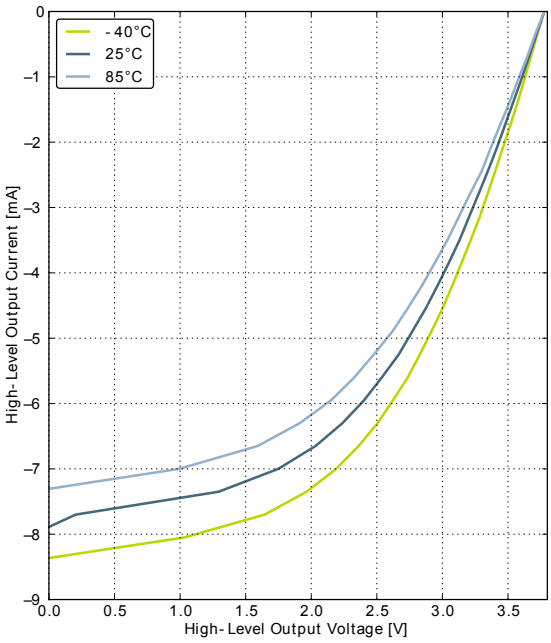


GPIO_Px_CTRL DRIVEMODE = HIGH

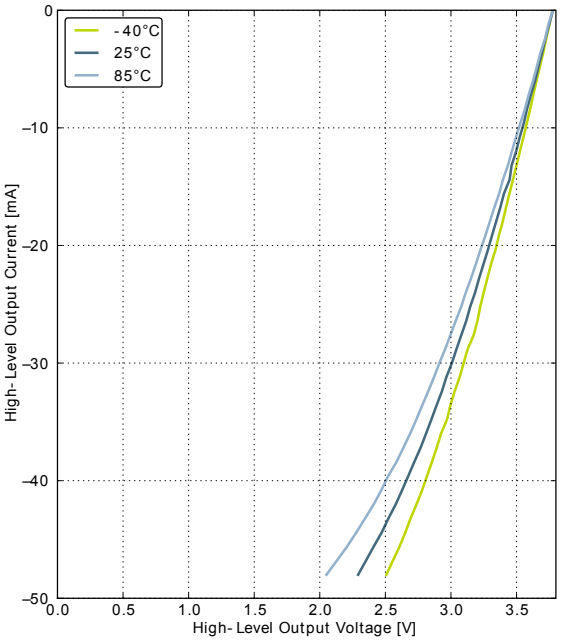
Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage



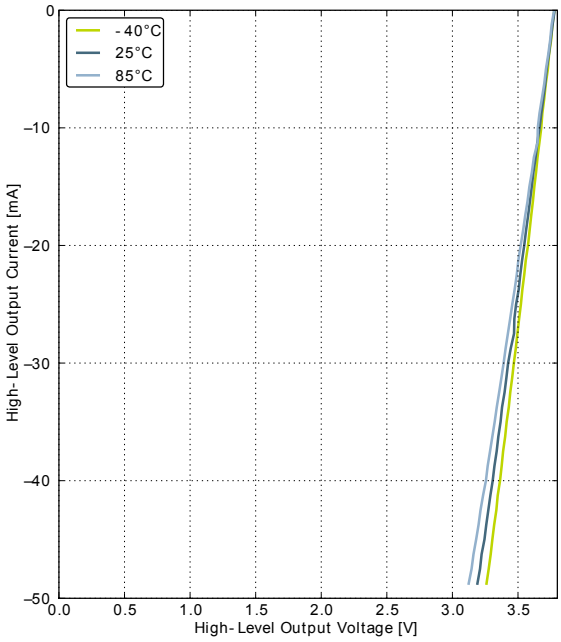
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



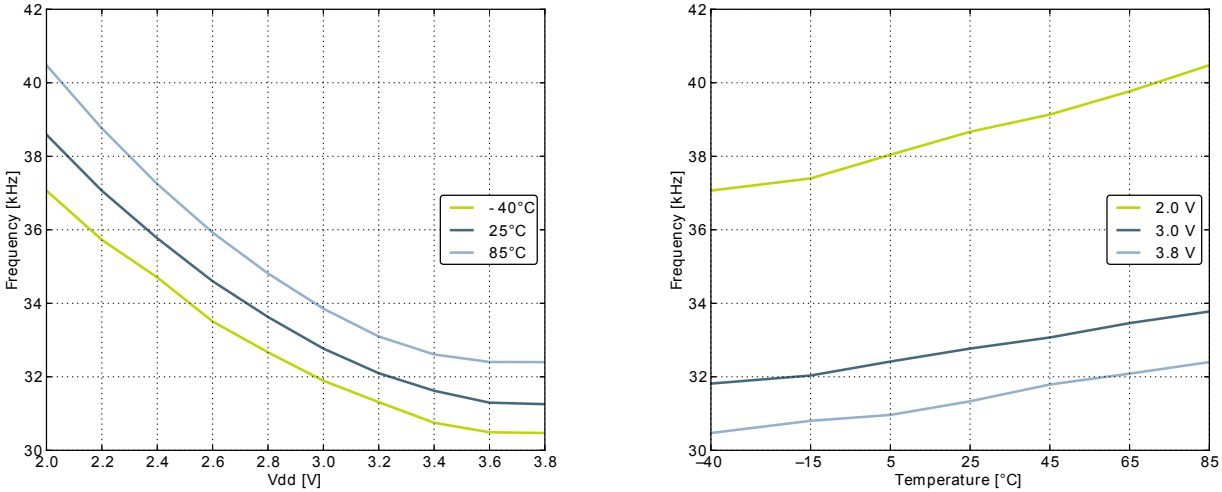
GPIO_Px_CTRL DRIVEMODE = HIGH

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25°C		31.3	32.768	34.3	kHz
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			361	492	nA
$TUNESTEP_{LFRCO}$	Frequency step for LSB change in TUNING value			202		Hz

Figure 3.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



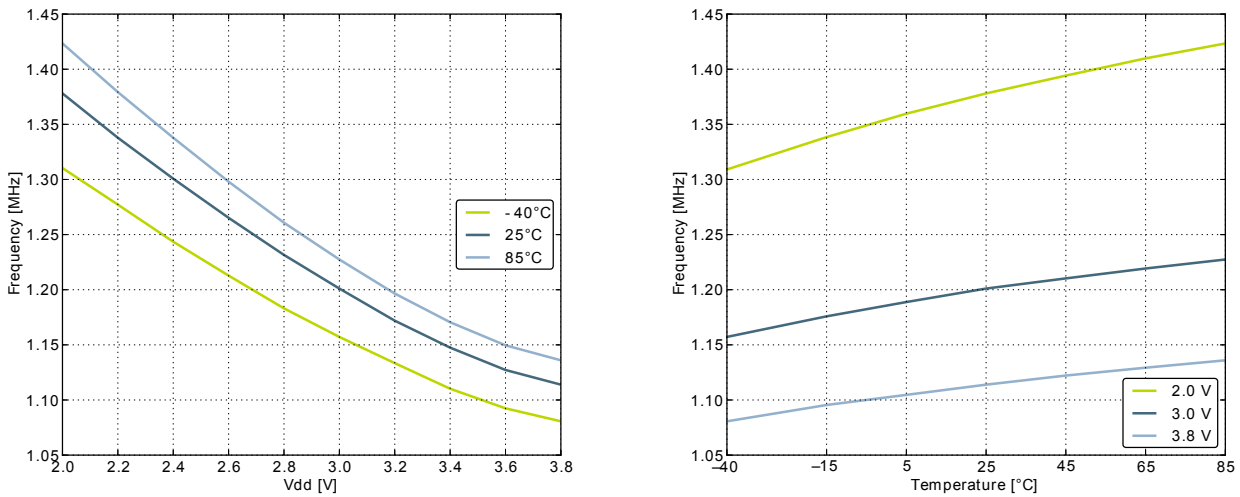
3.9.4 HFRCO

Table 3.11. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	24 MHz frequency band	23.28	24.0	24.72	MHz
		21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40	6.60	6.80	MHz
		1 MHz frequency band	1.15	1.20	1.25	MHz
$t_{HFRCO\_settling}$	Settling time after start-up	f_{HFRCO} = 14 MHz		0.6		Cycles
I_{HFRCO}	Current consumption	f_{HFRCO} = 24 MHz		158	184	µA
		f_{HFRCO} = 21 MHz		143	175	µA
		f_{HFRCO} = 14 MHz		113	140	µA
		f_{HFRCO} = 11 MHz		101	125	µA
		f_{HFRCO} = 6.6 MHz		84	105	µA
		f_{HFRCO} = 1.2 MHz		27	40	µA
$TUNESTEP_{H-FRCO}$	Frequency step for LSB change in TUNING value	24 MHz frequency band		66.8[1]		kHz
		21 MHz frequency band		52.8[1]		kHz
		14 MHz frequency band		36.9[1]		kHz
		11 MHz frequency band		30.1[1]		kHz
		7 MHz frequency band		18.0[1]		kHz
		1 MHz frequency band		3.4		kHz

[1]The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 21 MHz across operating conditions.

Figure 3.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature



3.9.6 USHFRCO

Table 3.13. USHFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{USHFRCO}$	Oscillation frequency	No Clock Recovery, Full Temperature and Supply Range, 48 MHz band	47.10	48.00	48.90	MHz
		No Clock Recovery, Full Temperature and Supply Range, 24 MHz band	23.73	24.00	24.32	MHz
		No Clock Recovery, 25°C, 3.3V, 48 MHz band	47.50	48.00	48.50	MHz
		No Clock Recovery, 25°C, 3.3V, 24 MHz band	23.86	24.00	24.16	MHz
		USB Active with Clock Recovery, Full Temperature and Supply Range	47.88	48.00	48.12	MHz
$TC_{USHFRCO}$	Temperature coefficient	3.3V		0.0175		%/°C
$VC_{USHFRCO}$	Supply voltage coefficient	25°C		0.0045		%/V
$I_{USHFRCO}$	Current consumption	$f_{USHFRCO}$ = 48 MHz	1.21	1.36	1.48	mA
		$f_{USHFRCO}$ = 24 MHz	0.81	0.92	1.02	mA

3.9.7 ULFRCO

Table 3.14. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ULFRCO}	Oscillation frequency	25°C, 3V	0.70		1.75	kHz
TC_{ULFRCO}	Temperature coefficient			0.05		%/°C
VC_{ULFRCO}	Supply voltage coefficient			-18.2		%/V

3.10 Analog Digital Converter (ADC)

Table 3.15. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	Single ended	0		V_{REF}	V
		Differential	$-V_{REF}/2$		$V_{REF}/2$	V
$V_{ADCREFIN}$	Input range of external reference voltage, single ended and differential		1.25		V_{DD}	V
$V_{ADCREFIN\_CH7}$	Input range of external negative reference voltage on channel 7	See $V_{ADCREFIN}$	0		V_{DD} - 1.1	V

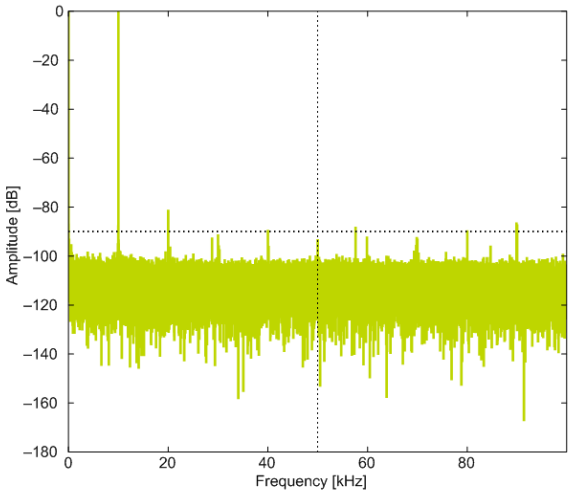
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference	68	79		dBc
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		79		dBc
$V_{ADCOFFSET}$	Offset voltage	After calibration, single ended	-4	0.3	4	mV
		After calibration, differential		0.3		mV
$TGRAD_{ADCTH}$	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/ °C
DNL_{ADC}	Differential non-linearity (DNL)	V_{DD}= 3.0 V, external 2.5V reference	-1	±0.7	4	LSB
INL_{ADC}	Integral non-linearity (INL), End point method			±1.6	±3	LSB
MC_{ADC}	No missing codes		11.999[1]	12		bits
$VREF_{ADC}$	ADC Internal Voltage Reference	Internal 1.25V, V_{DD} = 3V, 25°C	1.248	1.254	1.262	V
		Internal 1.25V, Full temperature and supply range	1.188	1.254	1.302	V
		Internal 2.5V, V_{DD} = 3V, 25°C	2.492	2.506	2.520	V
		Internal 2.5V, Full temperature and supply range	2.402	2.506	2.600	V

[1]On the average every ADC will have one missing code, most likely to appear around 2048 ± n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

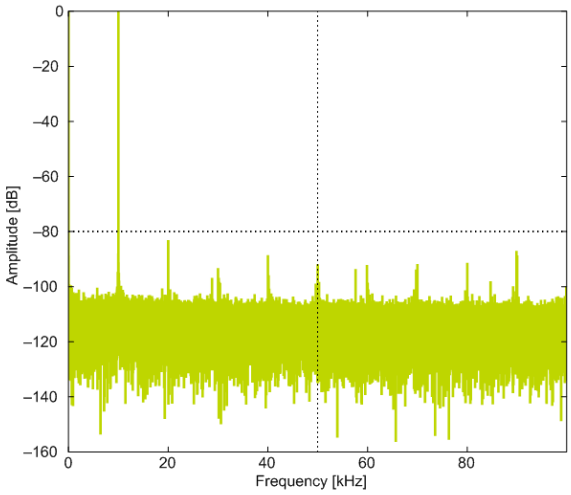
The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.26 (p. 37) and Figure 3.27 (p. 37) , respectively.

3.10.1 Typical performance

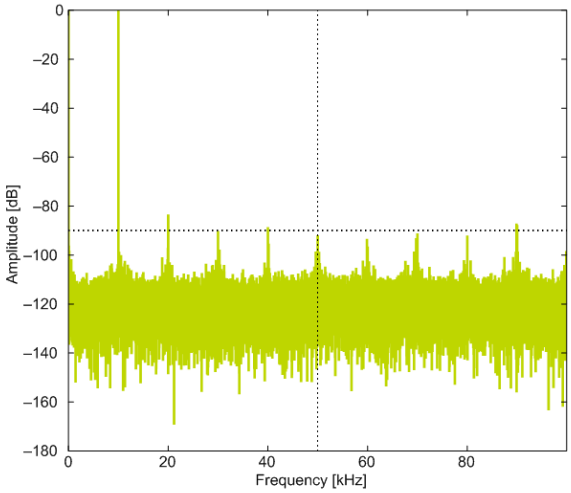
Figure 3.28. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C



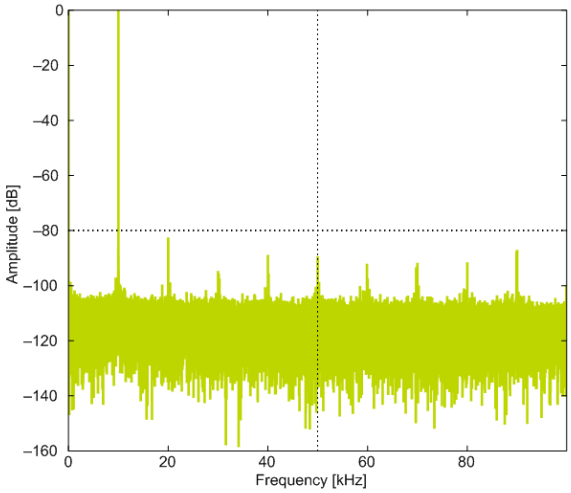
1.25V Reference



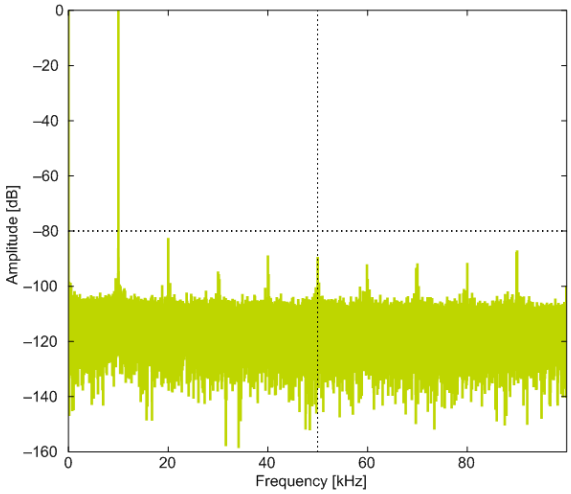
2.5V Reference



2XVDDVSS Reference



5VDIFF Reference



VDD Reference

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32HG321.

4.1 Pinout

The *EFM32HG321* pinout is shown in Figure 4.1 (p. 52) and Table 4.1 (p. 52). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32HG321 Pinout (top view, not to scale)

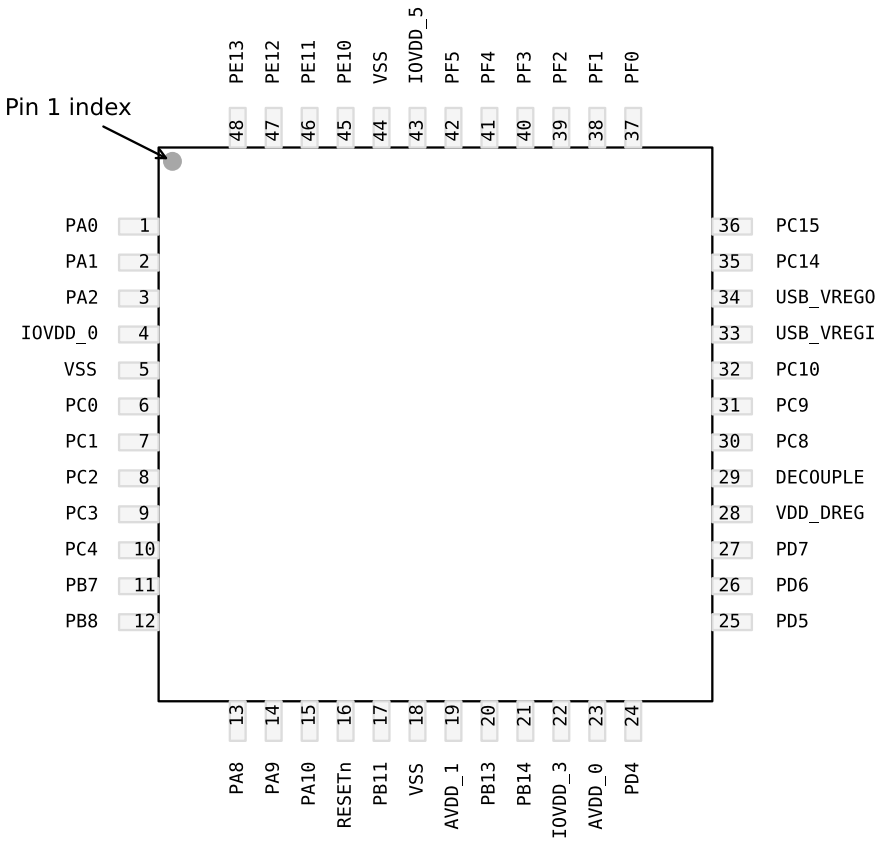


Table 4.1. Device Pinout

QFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC1 #6 TIM0_CC0 #0/1/4 PCNT0_S0IN #4	USB_DMPU #0 US1_RX #4 LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
2	PA1		TIM0_CC0 #6 TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0

QFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
34	USB_VREGO				
35	PC14		TIM0_CDTI1 #1/6 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 US1_CS #3/4 LEU0_TX #5 USB_DM	PRS_CH0 #2
36	PC15		TIM0_CDTI2 #1/6 TIM1_CC2 #0	US0_CLK #3 US1_CLK #3 LEU0_RX #5 USB_DP	PRS_CH1 #2
37	PF0		TIM0_CC0 #5	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0 BOOT_TX
38	PF1		TIM0_CC1 #5	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0 GPIO_EM4WU3 BOOT_RX
39	PF2		TIM0_CC2 #5/6 TIM2_CC0 #3	US1_TX #4 LEU0_TX #4	CMU_CLK0 #3 PRS_CH0 #3 GPIO_EM4WU4
40	PF3		TIM0_CDTI0 #5		PRS_CH0 #1
41	PF4		TIM0_CDTI1 #5		PRS_CH1 #1
42	PF5		TIM0_CDTI2 #5		PRS_CH2 #1
43	IOVDD_5	Digital IO power supply 5.			
44	VSS	Ground.			
45	PE10		TIM1_CC0 #1	US0_TX #0	PRS_CH2 #2
46	PE11		TIM1_CC1 #1	US0_RX #0	PRS_CH3 #2
47	PE12	ADC0_CH0	TIM1_CC2 #1 TIM2_CC1 #3	US0_RX #3 US0_CLK #0/6 I2C0_SDA #6	CMU_CLK1 #2 PRS_CH1 #3
48	PE13	ADC0_CH1	TIM2_CC2 #3	US0_TX #3 US0_CS #0/6 I2C0_SCL #6	ACMP0_O #0 PRS_CH2 #3 GPIO_EM4WU5

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 54). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM0_CC2	PA2	PA2			PC1	PF2	PF2	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0					PC2	PF3		Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1		PC14			PC3	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15			PC4	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0		PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8		PC8	PF2				Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9		PC9	PE12				Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10		PC10	PE13				Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12		PC9	PC15	PB13	PB13	PE12	USART0 clock input / output.
US0_CS	PE13		PC8	PC14	PB14	PB14	PE13	USART0 chip select input / output.
US0_RX	PE11		PC10	PE12	PB8	PC1	PC1	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10			PE13	PB7	PC0	PC0	USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7		PF0	PC15	PB11	PC3		USART1 clock input / output.
US1_CS	PB8		PF1	PC14	PC14	PC0		USART1 chip select input / output.
US1_RX	PC1		PD6	PD6	PA0	PC2		USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0		PD7	PD7	PF2	PC1		USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PC14							USB D- pin.
USB_DMPU	PA0							USB D- Pullup control.
USB_DP	PC15							USB D+ pin.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32HG321* is shown in Table 4.3 (p. 57) . Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

7 Revision History

7.1 Revision 1.00

December 4th, 2015

Updated all specs with results of full characterization.

Updated part number to revision B.

Added the USB electrical specifications table.

7.2 Revision 0.91

May 6th, 2015

Updated current consumption table for energy modes.

Updated GPIO max leakage current.

Updated startup time for HFXO and LFXO.

Updated current consumption for HFRCO and LFRCO.

Updated ADC current consumption.

Updated IDAC characteristics tables.

Updated ACMP internal resistance.

Updated VCMP current consumption.

7.3 Revision 0.90

March 16th, 2015

Note

This datasheet revision applies to a product under development. It's characteristics and specifications are subject to change without notice.

Corrected EM2 current consumption condition in Electrical Characteristics section.

Updated GPIO electrical characteristics.

Updated Max ESR_{HFXO} value for Crystal Frequency of 25 MHz.

Updated LFRCO plots.

Updated HFRCO table and plots.

Updated ADC table and temp sensor plot.

Added DMA current in Digital Peripherals section.

Updated block diagram.

Corrected leadframe type to matte-Sn.

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