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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg321f64g-b-qfp48

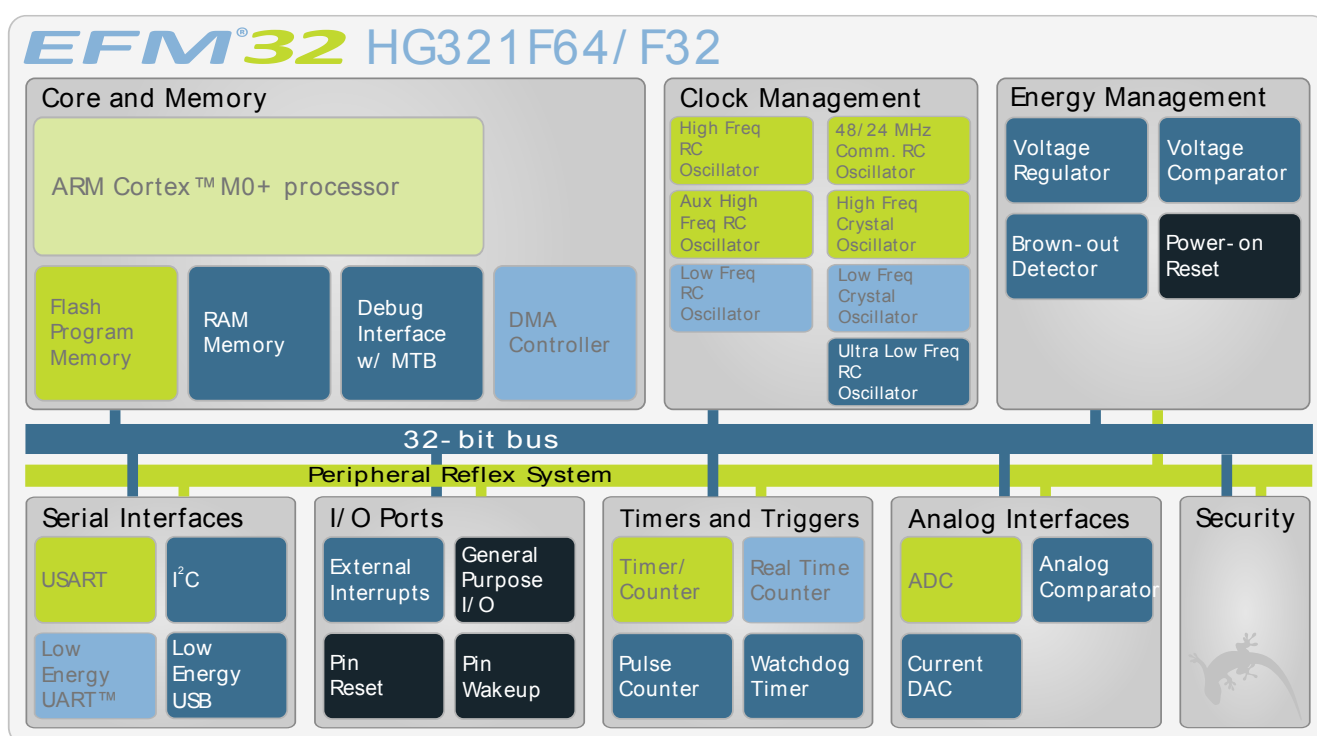
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0+, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32HG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32HG321 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32HG Reference Manual*.

A block diagram of the EFM32HG321 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and a Micro Trace Buffer (MTB) for data/instruction tracing.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32HG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is

divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32HG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32HG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32HG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Low Energy USB

The unique Low Energy USB peripheral provides a full-speed USB 2.0 compliant device controller and PHY with ultra-low current consumption. The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation, and includes a dedicated USB oscillator with clock recovery mechanism for crystal-free operation. No external components are required. The Low Energy Mode ensures the current consumption is optimized and enables USB communication on a strict power budget. The USB device includes an internal dedicated descriptor-based Scatter/Gather DMA and supports up to 3 OUT endpoints and 3 IN endpoints, in addition to endpoint 0. The on-chip PHY includes software controllable pull-up and pull-down resistors.

3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.0\text{ V}$, as defined in Table 3.2 (p. 8), unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8).

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150 ¹	$^{\circ}\text{C}$
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	$^{\circ}\text{C}$
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		$V_{DD}+0.3$	V

¹Based on programmed devices tested for 10000 hours at 150°C . Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	$^{\circ}\text{C}$
V_{DDOP}	Operating supply voltage	1.98		3.8	V
f_{APB}	Internal APB clock frequency			25	MHz
f_{AHB}	Internal AHB clock frequency			25	MHz

3.4 Current Consumption

Table 3.3. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash.	24 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		148	158	$\mu\text{A}/\text{MHz}$
		24 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		153	163	$\mu\text{A}/\text{MHz}$
		24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		161	172	$\mu\text{A}/\text{MHz}$
		24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		163	174	$\mu\text{A}/\text{MHz}$
		24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		127	137	$\mu\text{A}/\text{MHz}$
		24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		129	139	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		131	140	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		134	143	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		134	143	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		137	145	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		136	144	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		139	148	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		142	150	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		146	154	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		184	196	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		194	208	$\mu\text{A}/\text{MHz}$

Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz

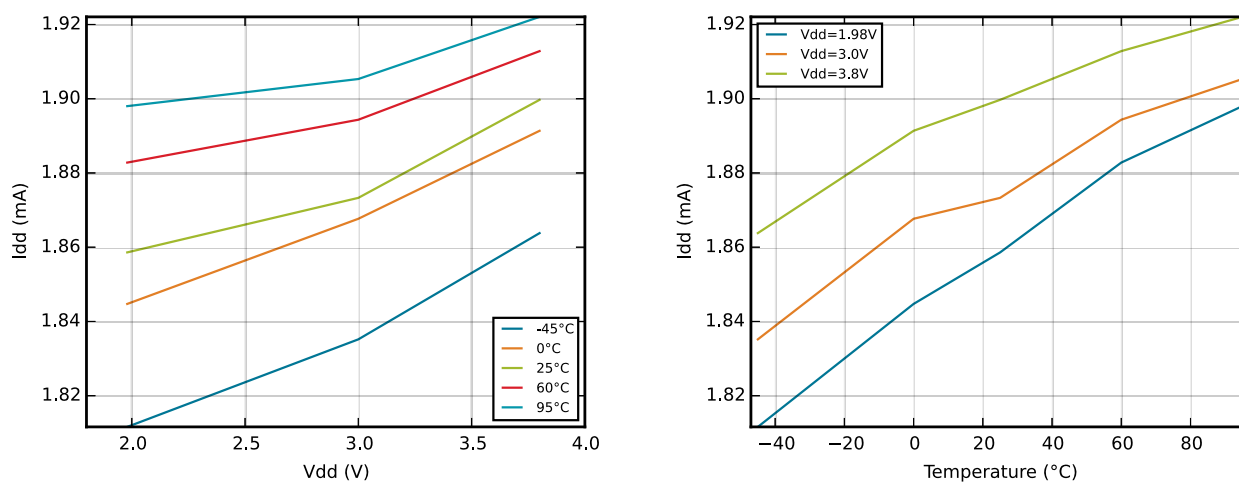


Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz

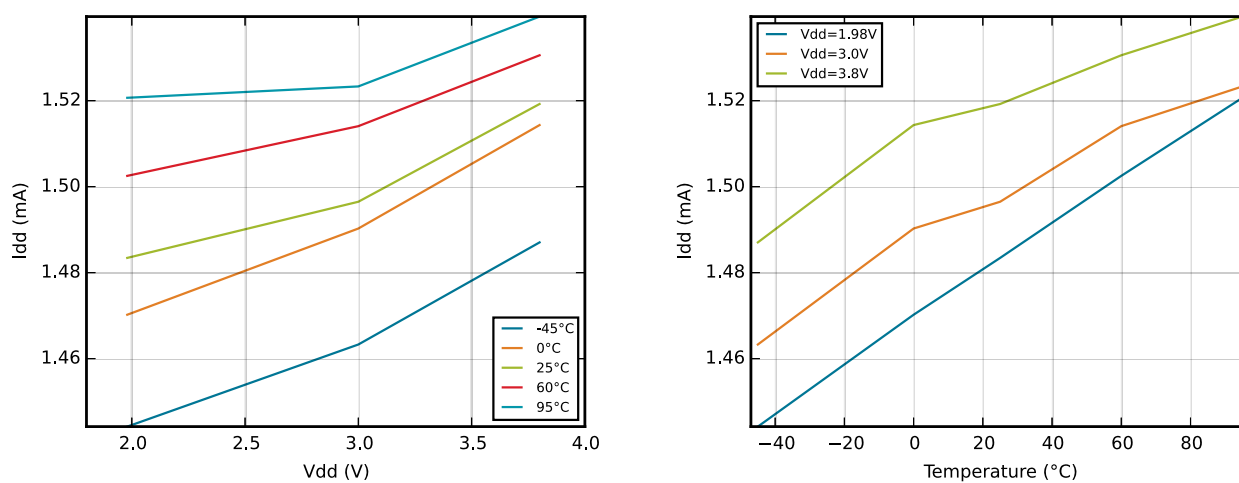
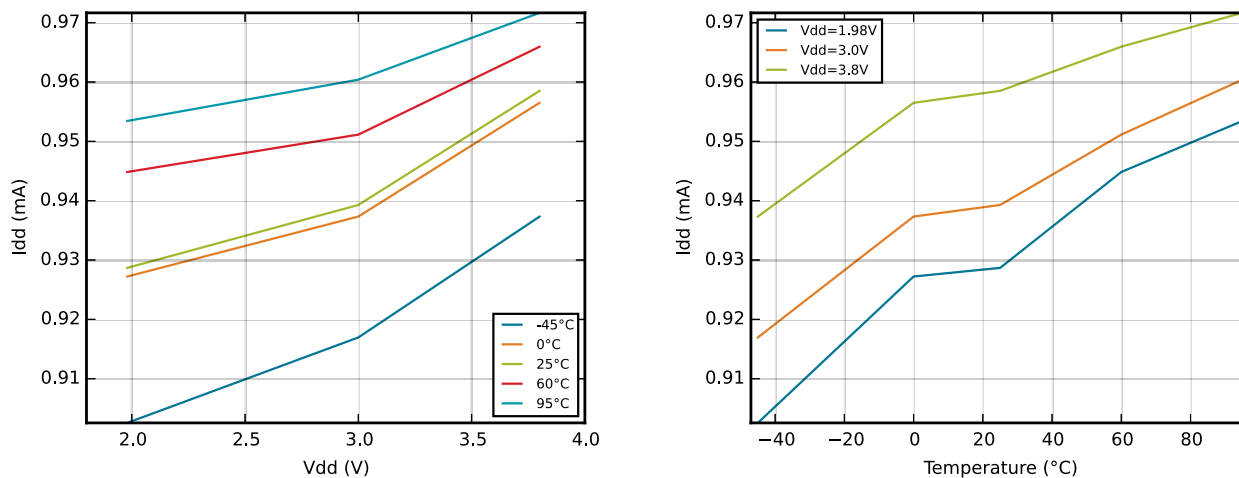


Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 6.6 MHz



3.4.2 EM1 Current Consumption

Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 24 MHz

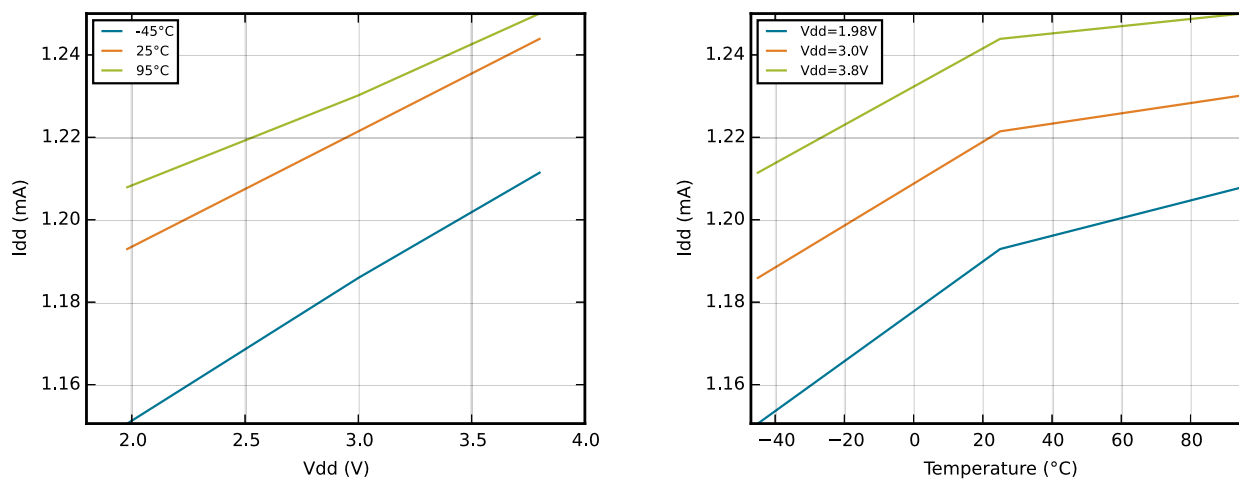


Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz

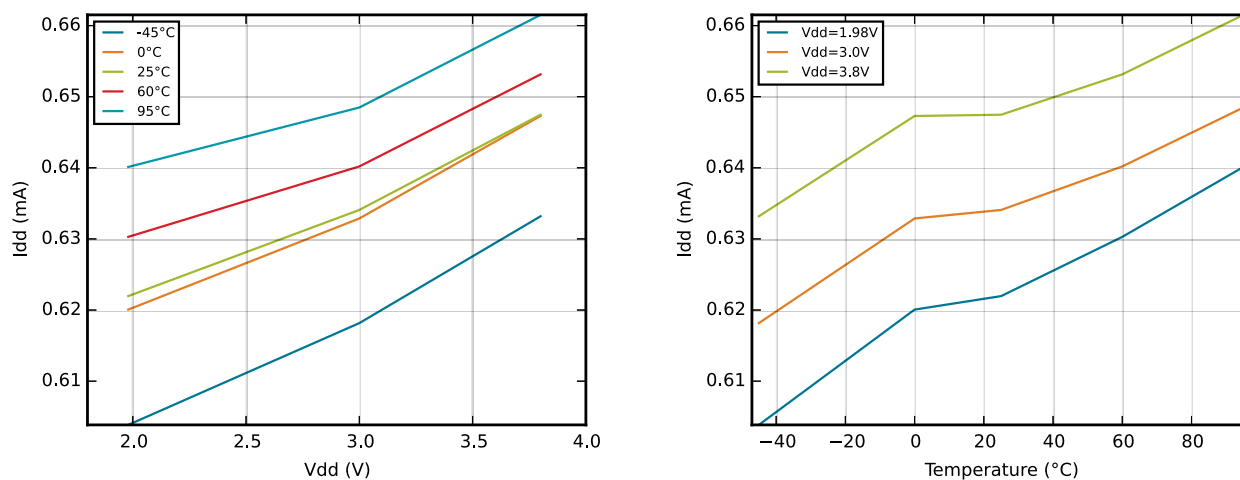
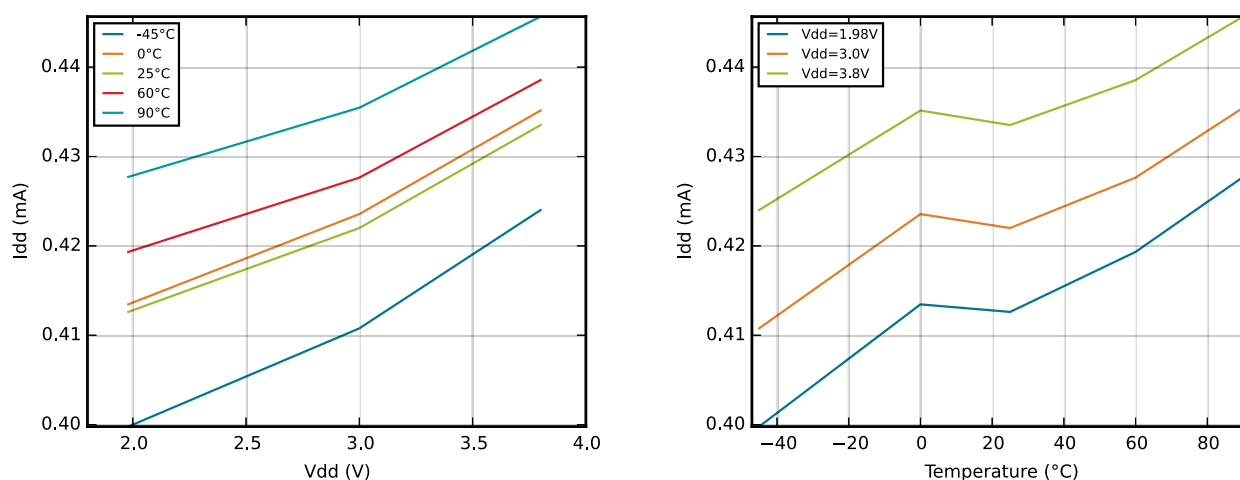
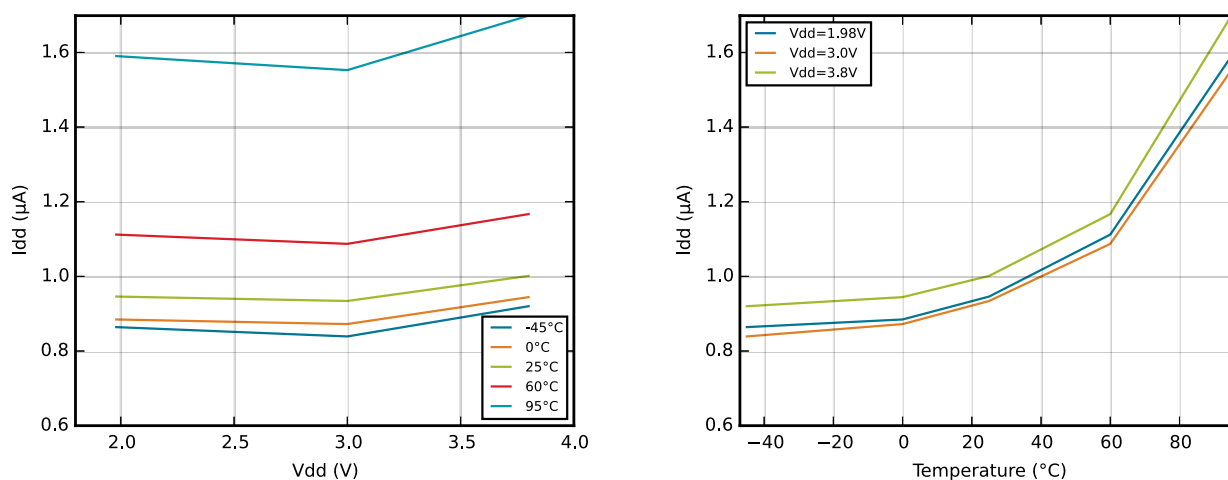


Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6 MHz



3.4.3 EM2 Current Consumption

Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.



3.4.4 EM3 Current Consumption

Figure 3.12. EM3 current consumption.

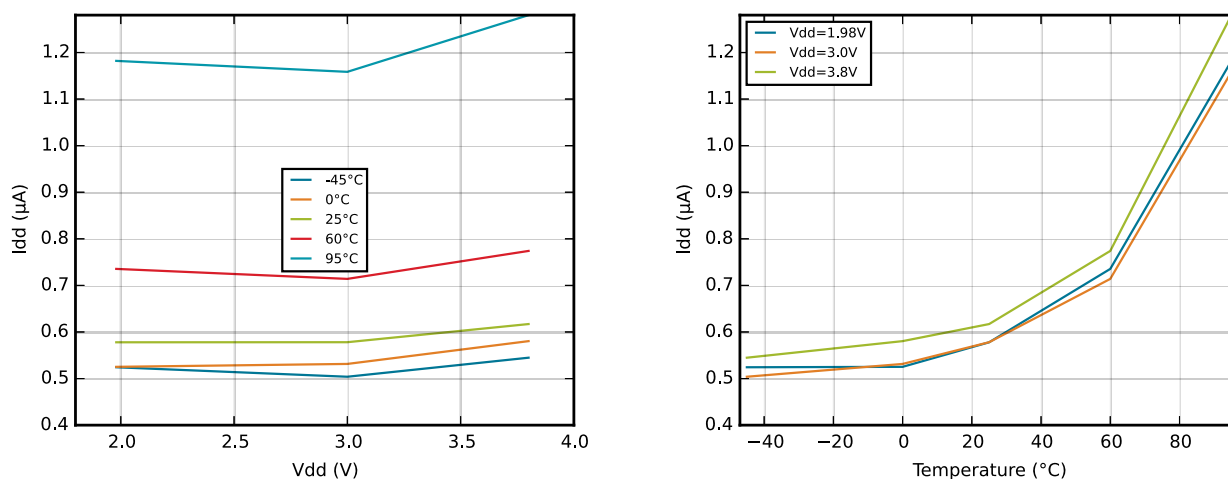


Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{BODextthr-}	BOD threshold on falling external supply voltage	EM0	1.74		1.96	V
		EM2	1.71	1.86	1.98	V
V _{BODextthr+}	BOD threshold on rising external supply voltage			1.85		V
t _{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C _{DECOUPLE}	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF
C _{USB_VREGO}	USB voltage regulator out decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND		1		μF
C _{USB_VREGI}	USB voltage regulator in decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND		4.7		μF

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
RET _{FLASH}	Flash data retention	T _{AMB} <150°C	10000			h
		T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) programming time		20			μs
t _{P_ERASE}	Page erase time		20	20.4	20.8	ms
t _{D_ERASE}	Device erase time		40	40.8	41.6	ms
I _{ERASE}	Erase current				7 ¹	mA
I _{WRITE}	Write current				7 ¹	mA
V _{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

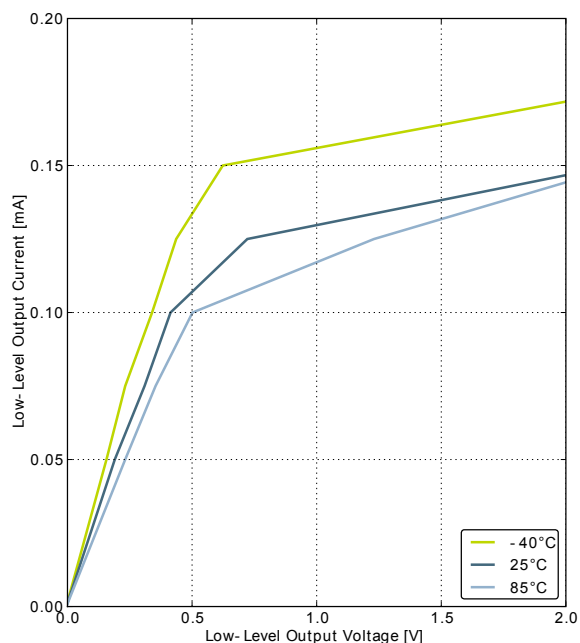
¹ Measured at 25°C

3.8 General Purpose Input Output

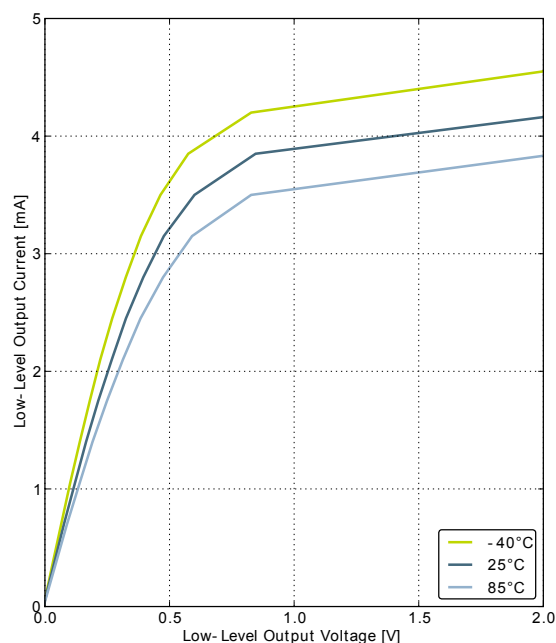
Table 3.7. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V

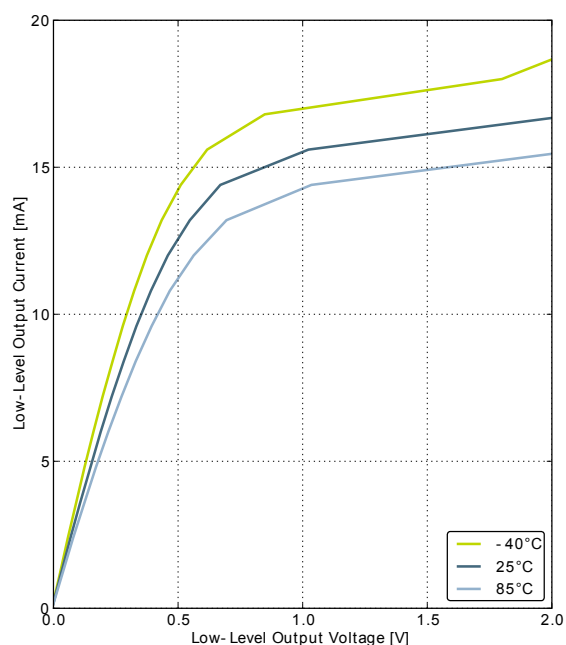
Figure 3.14. Typical Low-Level Output Current, 2V Supply Voltage



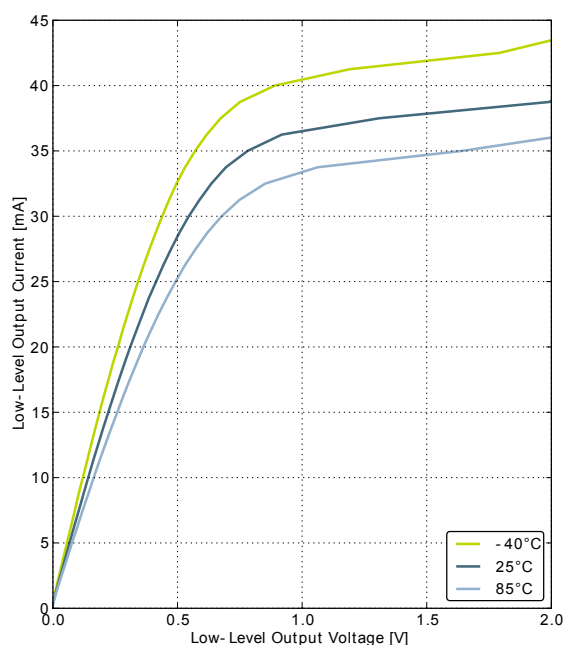
GPIO_Px_CTRL DRIVEMODE = LOWEST



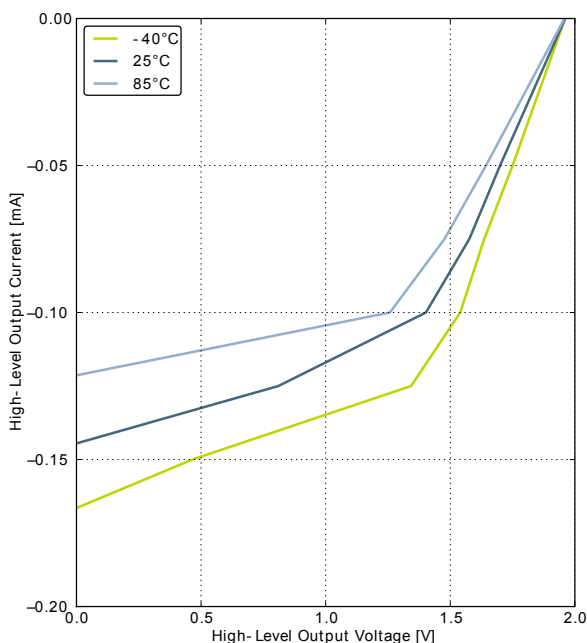
GPIO_Px_CTRL DRIVEMODE = LOW



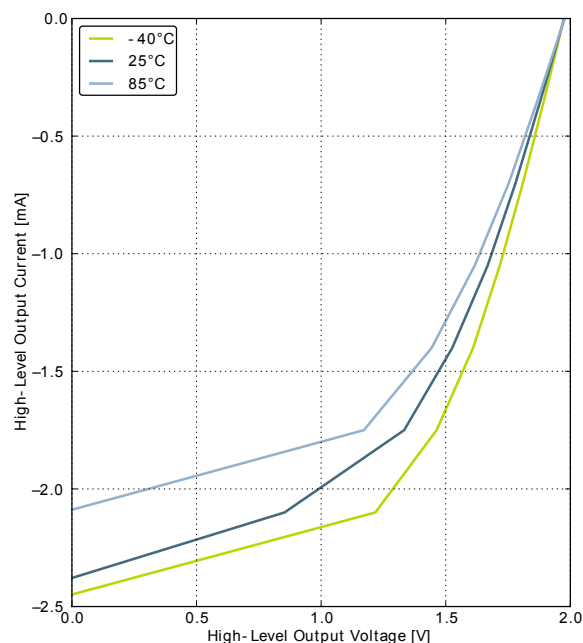
GPIO_Px_CTRL DRIVEMODE = STANDARD



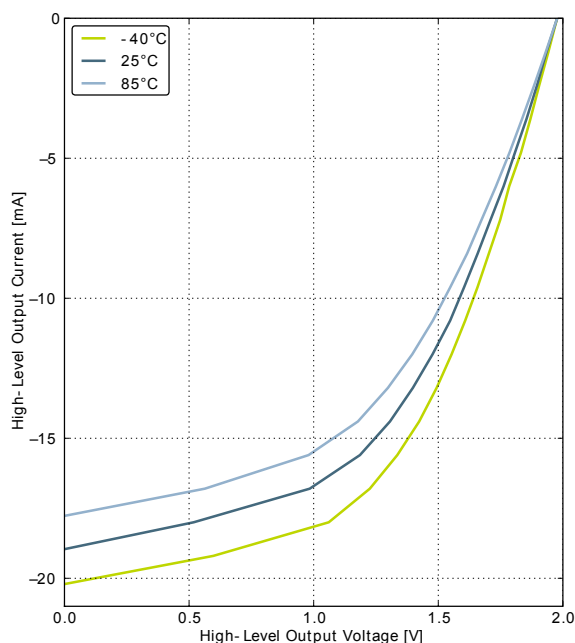
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage

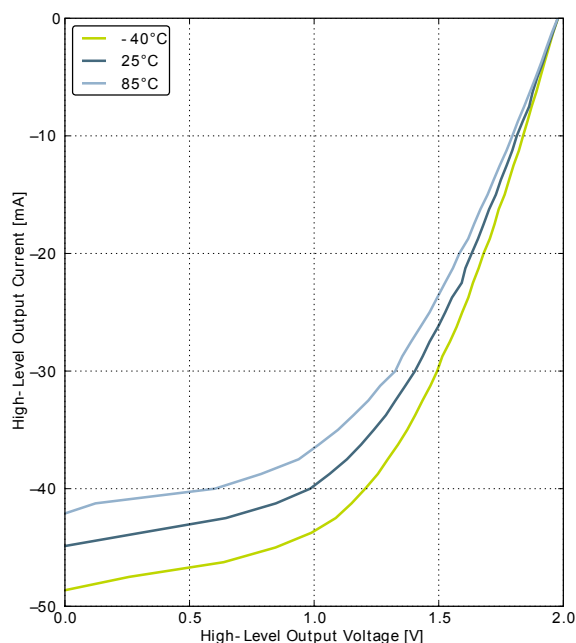
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

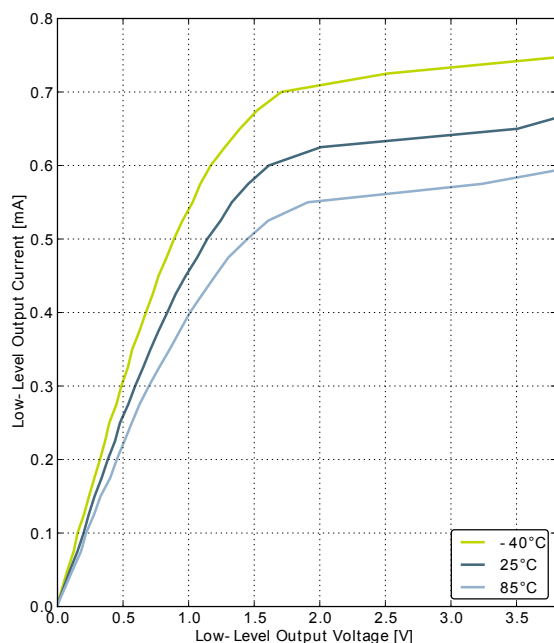


GPIO_Px_CTRL DRIVEMODE = STANDARD

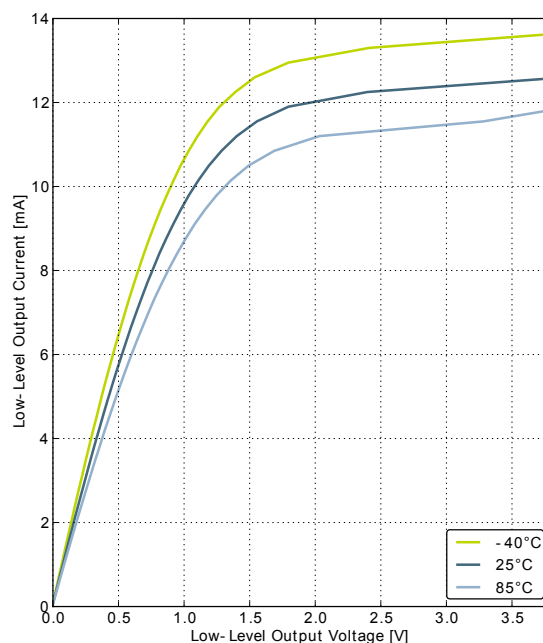


GPIO_Px_CTRL DRIVEMODE = HIGH

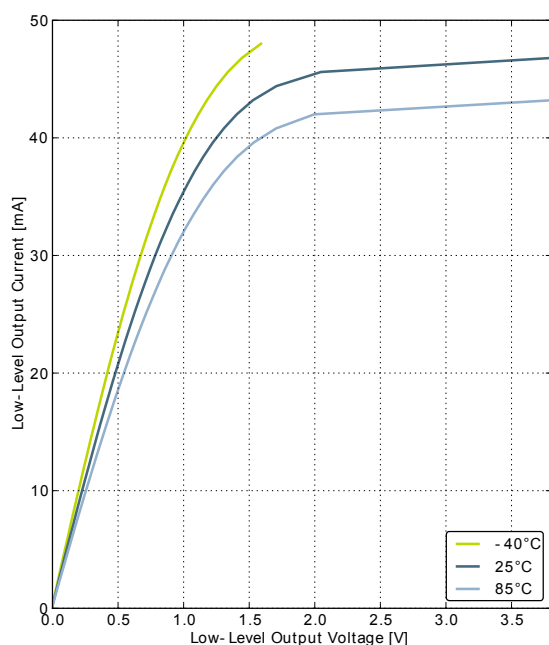
Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage



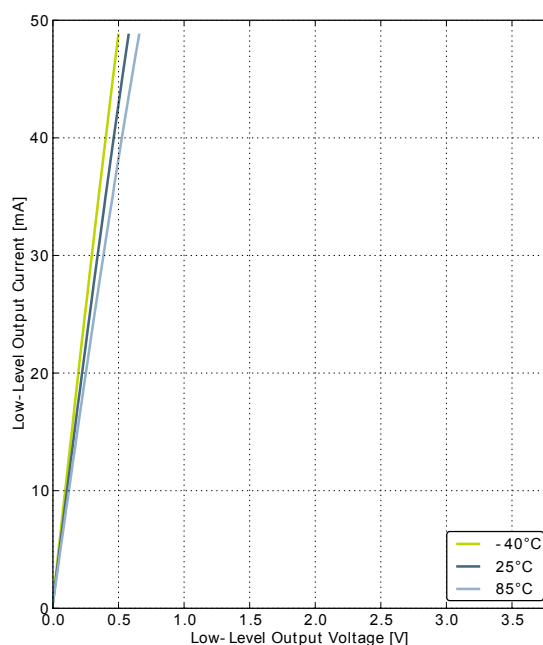
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		5		25	pF
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		1100		ms

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

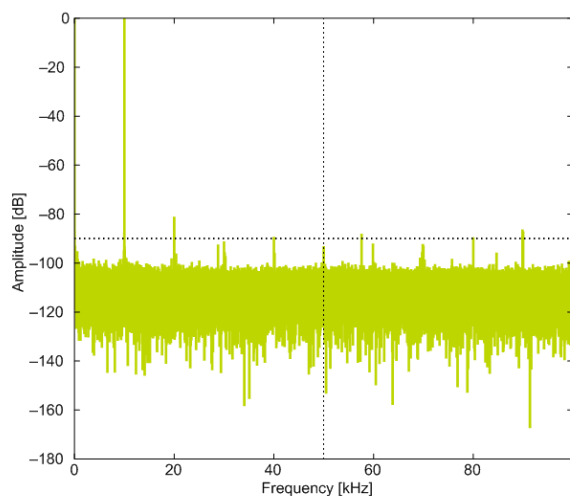
3.9.2 HFXO

Table 3.9. HFXO

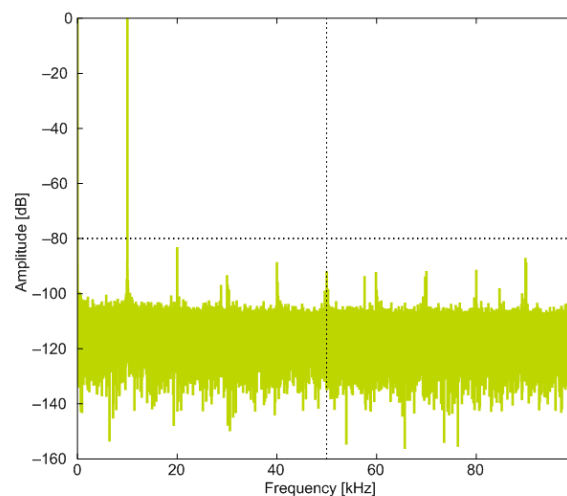
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported frequency, any mode		4		25	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 25 MHz		30	100	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μ A
		25 MHz: ESR=30 Ohm, C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μ A
t_{HFXO}	Startup time	25 MHz: ESR=30 Ohm, C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		785		μ s

3.10.1 Typical performance

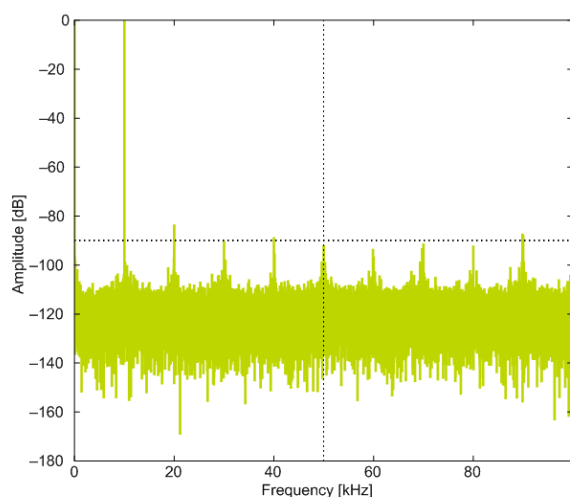
Figure 3.28. ADC Frequency Spectrum, $V_{dd} = 3V$, Temp = 25°C



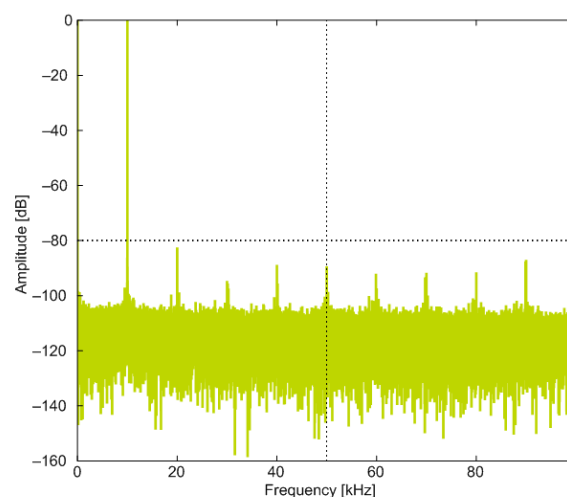
1.25V Reference



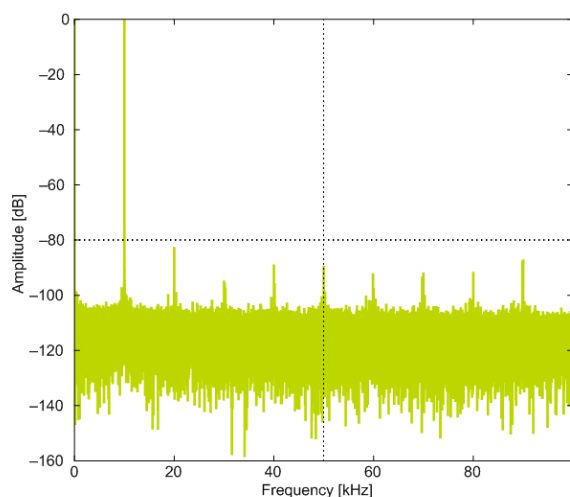
2.5V Reference



2XVDDVSS Reference



5VDIFF Reference



VDD Reference

3.12 Analog Comparator (ACMP)

Table 3.25. ACMP

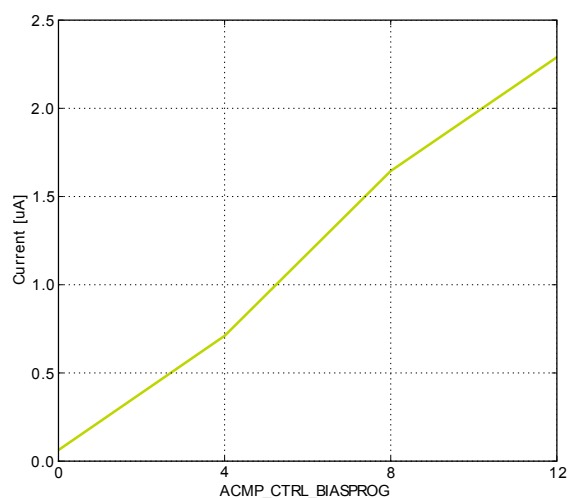
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.4	μA
		BIASPROG=0b1111, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	15	μA
		BIASPROG=0b1111, FULL-BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	μA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		μA
		Internal voltage reference		5		μA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		40		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		70		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		101		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		132		kOhm
$t_{ACMPSTART}$	Startup time				10	μs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 47) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

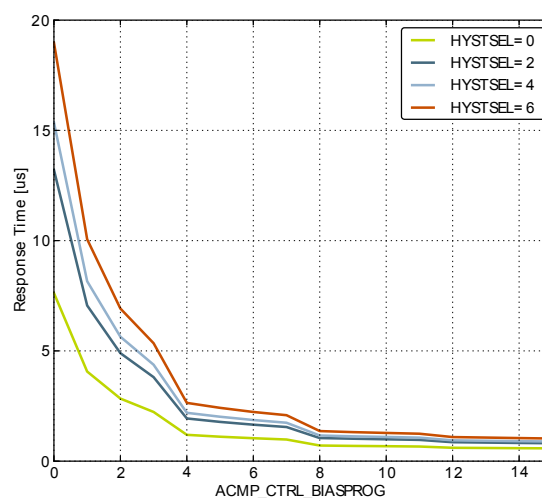
Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

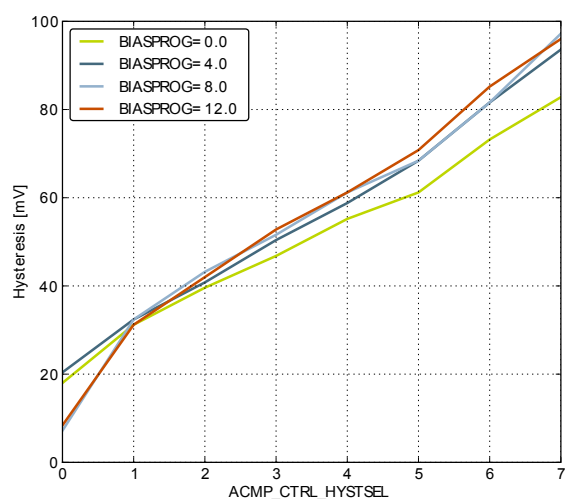
Figure 3.37. ACMP Characteristics, $V_{dd} = 3V$, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4

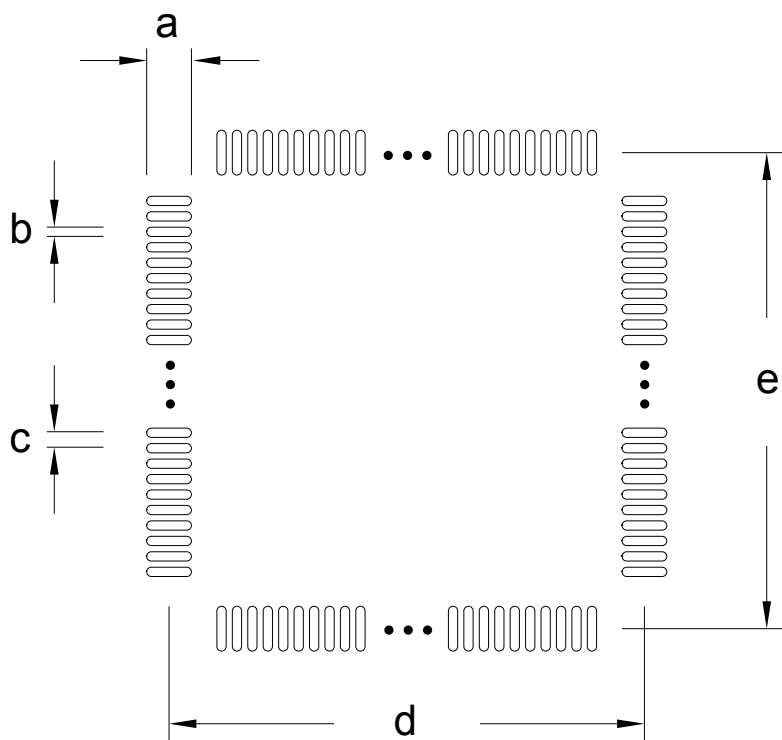


Response time , $V_{cm} = 1.25V$, CP+ to CP- = 100mV



Hysteresis

QFP48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	IOVDD_0	Digital IO power supply 0.			
5	VSS	Ground.			
6	PC0	ACMP0_CH0	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5/6 US1_TX #0 US1_CS #5 I2C0_SDA #4	PRS_CH2 #0
7	PC1	ACMP0_CH1	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5/6 US1_TX #5 US1_RX #0 I2C0_SCL #4	PRS_CH3 #0
8	PC2	ACMP0_CH2	TIM0_CDTI0 #4	US1_RX #5	
9	PC3	ACMP0_CH3	TIM0_CDTI1 #4	US1_CLK #5	
10	PC4	ACMP0_CH4	TIM0_CDTI2 #4		GPIO_EM4WU6
11	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
12	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
13	PA8		TIM2_CC0 #0		
14	PA9		TIM2_CC1 #0		
15	PA10		TIM2_CC2 #0		
16	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
17	PB11	IDAC0_OUT	TIM1_CC2 #3 PCNT0_S1IN #4	US1_CLK #4	CMU_CLK1 #3 ACMP0_O #3
18	VSS	Ground.			
19	AVDD_1	Analog power supply 1.			
20	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	
21	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
22	IOVDD_3	Digital IO power supply 3.			
23	AVDD_0	Analog power supply 0.			
24	PD4	ADC0_CH4		LEU0_TX #0	
25	PD5	ADC0_CH5		LEU0_RX #0	
26	PD6	ADC0_CH6	TIM1_CC0 #4 PCNT0_S0IN #3	US1_RX #2/3 I2C0_SDA #1	ACMP0_O #2
27	PD7	ADC0_CH7	TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2/3 I2C0_SCL #1	CMU_CLK0 #2
28	VDD_DREG	Power supply for on-chip voltage regulator.			
29	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
30	PC8		TIM2_CC0 #2	US0_CS #2	
31	PC9		TIM2_CC1 #2	US0_CLK #2	GPIO_EM4WU2
32	PC10		TIM2_CC2 #2	US0_RX #2	
33	USB_VREGI				

Figure 5.3. TQFP48 PCB Stencil Design**Table 5.3. QFP48 PCB Stencil Design Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)
a	1.50
b	0.20
c	0.50
d	8.50
e	8.50

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.2 (p. 57) .

5.2 Soldering Information

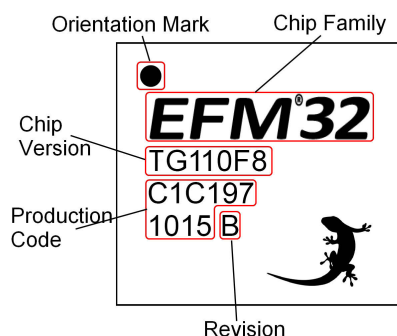
The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 62) .

6.3 Errata

Please see the errata document for EFM32HG321 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:

<http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

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