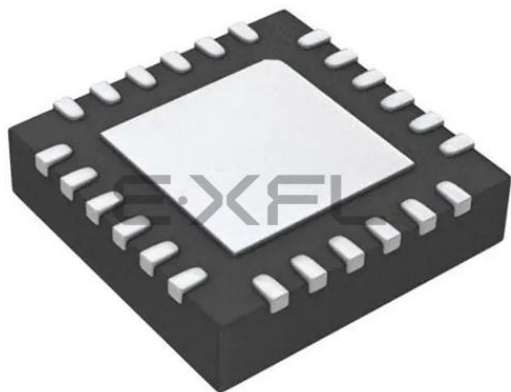




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	I ² C, SPI, UART/USART, USB
Peripherals	POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051t623-gmr

C8051T622/3 and C8051T326/7

18.1. Endpoint Addressing	116
18.2. USB Transceiver	117
18.3. USB Register Access	119
18.4. USB Clock Configuration.....	123
18.5. FIFO Management	124
18.5.1. FIFO Split Mode	125
18.5.2. FIFO Double Buffering	125
18.5.1. FIFO Access	126
18.6. Function Addressing.....	127
18.7. Function Configuration and Control.....	127
18.8. Interrupts	130
18.9. The Serial Interface Engine	136
18.10. Endpoint0	136
18.10.1. Endpoint0 SETUP Transactions	137
18.10.2. Endpoint0 IN Transactions.....	137
18.10.3. Endpoint0 OUT Transactions.....	138
18.11. Configuring Endpoints1-2	140
18.12. Controlling Endpoints1-2 IN.....	141
18.12.1. Endpoints1-2 IN Interrupt or Bulk Mode.....	141
18.12.2. Endpoints1-2 IN Isochronous Mode.....	142
18.13. Controlling Endpoints1-2 OUT.....	144
18.13.1. Endpoints1-2 OUT Interrupt or Bulk Mode.....	145
18.13.2. Endpoints1-2 OUT Isochronous Mode.....	145
19. SMBus.....	149
19.1. Supporting Documents	150
19.2. SMBus Configuration.....	150
19.3. SMBus Operation	150
19.3.1. Transmitter Vs. Receiver.....	151
19.3.2. Arbitration.....	151
19.3.3. Clock Low Extension.....	151
19.3.4. SCL Low Timeout.....	151
19.3.5. SCL High (SMBus Free) Timeout	152
19.4. Using the SMBus.....	152
19.4.1. SMBus Configuration Register.....	152
19.4.2. SMB0CN Control Register	156
19.4.2.1. Software ACK Generation	156
19.4.2.2. Hardware ACK Generation	156
19.4.3. Hardware Slave Address Recognition	158
19.4.4. Data Register	161
19.5. SMBus Transfer Modes.....	162
19.5.1. Write Sequence (Master)	162
19.5.2. Read Sequence (Master).....	163
19.5.3. Write Sequence (Slave)	164
19.5.4. Read Sequence (Slave).....	165
19.6. SMBus Status Decoding.....	165

C8051T622/3 and C8051T326/7

List of Tables

Table 2.1. Product Selection Guide	18
Table 3.1. Pin Definitions for the C8051T622/3 and C8051T326/7	19
Table 4.1. QFN-24 Package Dimensions	24
Table 4.2. QFN-24 PCB Land Pattern Dimensions	25
Table 5.1. QFN-28 Package Dimensions	26
Table 5.2. QFN-28 PCB Land Pattern Dimensions	27
Table 6.1. Absolute Maximum Ratings	28
Table 6.2. Global Electrical Characteristics	29
Table 6.3. Port I/O DC Electrical Characteristics	30
Table 6.4. Reset Electrical Characteristics	30
Table 6.5. Internal Voltage Regulator Electrical Characteristics	31
Table 6.6. EPROM Electrical Characteristics	31
Table 6.7. Internal High-Frequency Oscillator Electrical Characteristics	32
Table 6.8. Internal Low-Frequency Oscillator Electrical Characteristics	32
Table 6.9. External Oscillator Electrical Characteristics	32
Table 6.10. USB Transceiver Electrical Characteristic	33
Table 8.1. CIP-51 Instruction Set Summary	42
Table 11.1. Special Function Register (SFR) Memory Map	56
Table 11.2. Special Function Registers	57
Table 12.1. Interrupt Summary	62
Table 13.1. Security Byte Decoding	73
Table 17.1. Port I/O Assignment for Analog Functions	99
Table 17.2. Port I/O Assignment for Digital Functions	99
Table 17.3. Port I/O Assignment for External Digital Event Capture Functions	100
Table 18.1. Endpoint Addressing Scheme	117
Table 18.2. USB0 Controller Registers	122
Table 18.3. FIFO Configurations	126
Table 19.1. SMBus Clock Source Selection	153
Table 19.2. Minimum SDA Setup and Hold Times	154
Table 19.3. Sources for Hardware Changes to SMB0CN	158
Table 19.4. Hardware Address Recognition Examples (EHACK = 1)	159
Table 19.5. SMBus Status Decoding With Hardware ACK Generation Disabled (EHACK = 0)	166
Table 19.6. SMBus Status Decoding With Hardware ACK Generation Enabled (EHACK = 1)	168
Table 20.1. Timer Settings for Standard Baud Rates Using The Internal 24.5 MHz Oscillator	178
Table 20.2. Timer Settings for Standard Baud Rates Using an External 22.1184 MHz Oscillator	178
Table 21.1. Baud Rate Generator Settings for Standard Baud Rates	180
Table 22.1. SPI Slave Timing Parameters	201
Table 24.1. PCA Timebase Input Options	225

C8051T622/3 and C8051T326/7

List of Registers

SFR Definition 7.1. REG01CN: Voltage Regulator Control	39
SFR Definition 8.1. DPL: Data Pointer Low Byte	46
SFR Definition 8.2. DPH: Data Pointer High Byte	46
SFR Definition 8.3. SP: Stack Pointer	47
SFR Definition 8.4. ACC: Accumulator	47
SFR Definition 8.5. B: B Register	47
SFR Definition 8.6. PSW: Program Status Word	48
SFR Definition 9.1. PFE0CN: Prefetch Engine Control	49
SFR Definition 10.1. EMI0CN: External Memory Interface Control	53
SFR Definition 10.2. EMI0CF: External Memory Configuration	55
SFR Definition 12.1. IE: Interrupt Enable	63
SFR Definition 12.2. IP: Interrupt Priority	64
SFR Definition 12.3. EIE1: Extended Interrupt Enable 1	65
SFR Definition 12.4. EIP1: Extended Interrupt Priority 1	66
SFR Definition 12.5. EIE2: Extended Interrupt Enable 2	67
SFR Definition 12.6. EIP2: Extended Interrupt Priority 2	68
SFR Definition 12.7. IT01CF: INT0/INT1 ConfigurationO	70
SFR Definition 13.1. PSCTL: Program Store R/W Control	75
SFR Definition 13.2. MEMKEY: EPROM Memory Lock and Key	75
SFR Definition 13.3. IAPCN: In-Application Programming Control	76
SFR Definition 14.1. PCON: Power Control	79
SFR Definition 15.1. VDM0CN: VDD Monitor Control	83
SFR Definition 15.2. RSTSRC: Reset Source	85
SFR Definition 16.1. CLKSEL: Clock Select	88
SFR Definition 16.2. OSCICL: Internal H-F Oscillator Calibration	89
SFR Definition 16.3. OSCICN: Internal H-F Oscillator Control	90
SFR Definition 16.4. CLKMUL: Clock Multiplier Control	91
SFR Definition 16.5. OSCLCN: Internal L-F Oscillator Control	92
SFR Definition 16.6. OSCXCN: External Oscillator Control	96
SFR Definition 17.1. XBR0: Port I/O Crossbar Register 0	105
SFR Definition 17.2. XBR1: Port I/O Crossbar Register 1	106
SFR Definition 17.3. XBR2: Port I/O Crossbar Register 2	107
SFR Definition 17.4. P0MASK: Port 0 Mask Register	108
SFR Definition 17.5. P0MAT: Port 0 Match Register	108
SFR Definition 17.6. P1MASK: Port 1 Mask Register	109
SFR Definition 17.7. P1MAT: Port 1 Match Register	109
SFR Definition 17.8. P0: Port 0	110
SFR Definition 17.9. P0MDIN: Port 0 Input Mode	111
SFR Definition 17.10. P0MDOUT: Port 0 Output Mode	111
SFR Definition 17.11. P0SKIP: Port 0 Skip	112
SFR Definition 17.12. P1: Port 1	112
SFR Definition 17.13. P1MDIN: Port 1 Input Mode	113
SFR Definition 17.14. P1MDOUT: Port 1 Output Mode	113

C8051T622/3 and C8051T326/7

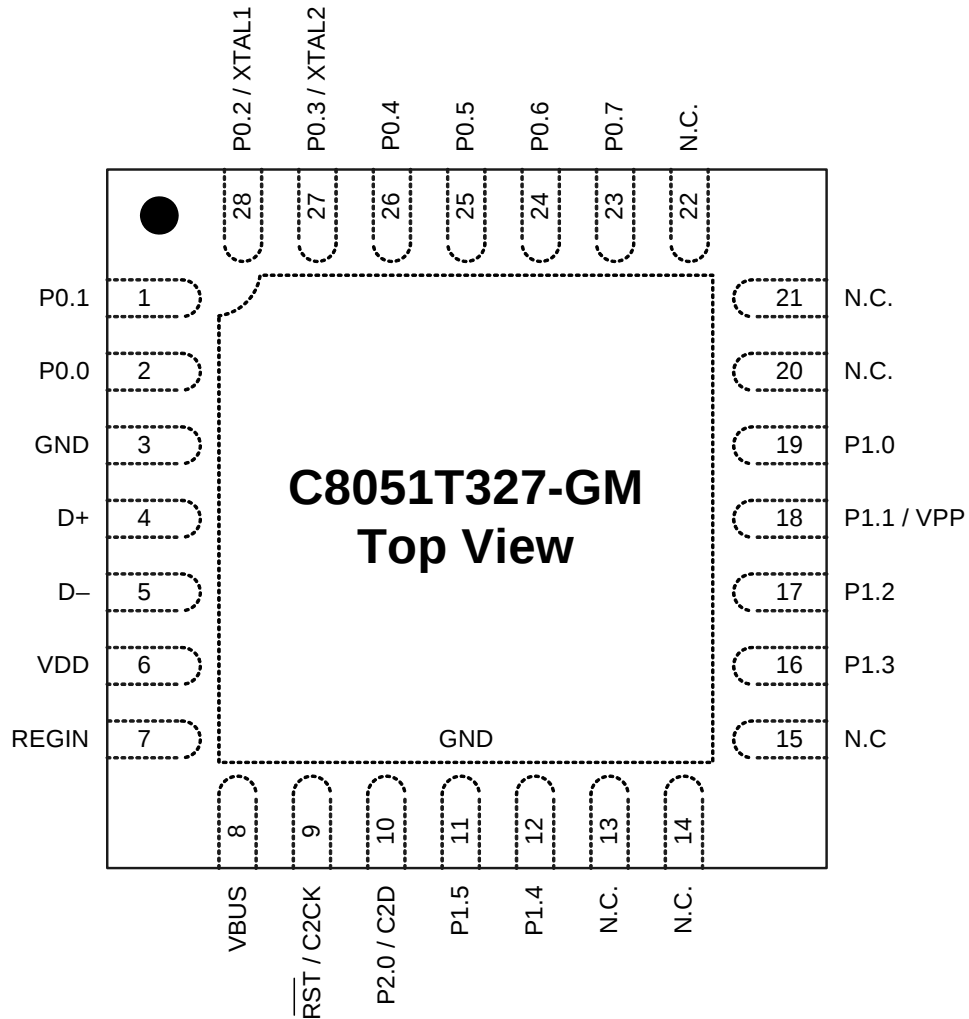


Figure 3.3. C8051T327 (QFN-28) Pinout Diagram (Top View)

C8051T622/3 and C8051T326/7

SFR Definition 8.3. SP: Stack Pointer

Bit	7	6	5	4	3	2	1	0
Name	SP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	1	1	1

SFR Address = 0x81

Bit	Name	Function
7:0	SP[7:0]	Stack Pointer. The Stack Pointer holds the location of the top of the stack. The stack pointer is incremented before every PUSH operation. The SP register defaults to 0x07 after reset.

SFR Definition 8.4. ACC: Accumulator

Bit	7	6	5	4	3	2	1	0
Name	ACC[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE0; Bit-Addressable

Bit	Name	Function
7:0	ACC[7:0]	Accumulator. This register is the accumulator for arithmetic operations.

SFR Definition 8.5. B: B Register

Bit	7	6	5	4	3	2	1	0
Name	B[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF0; Bit-Addressable

Bit	Name	Function
7:0	B[7:0]	B Register. This register serves as a second accumulator for certain arithmetic operations.

C8051T622/3 and C8051T326/7

byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 10.1 illustrates the data memory organization of the C8051T622/3 and C8051T326/7.

10.2.1.1. General Purpose Registers

The lower 32 bytes of data memory, locations 0x00 through 0x1F, may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in SFR Definition 8.6). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

10.2.1.2. Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination).

The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction:

```
MOV    C, 22.3h
```

moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

10.2.1.3. Stack

A programmer's stack can be located anywhere in the 256-byte data memory. The stack area is designated using the Stack Pointer (SP) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

10.2.2. External RAM

There are 1024 bytes of on-chip RAM mapped into the external data memory space. All of these address locations may be accessed using the external move instruction (MOVX) and the data pointer (DPTR), or using MOVX indirect addressing mode. If the MOVX instruction is used with an 8-bit address operand (such as @R1), then the high byte of the 16-bit address is provided by the External Memory Interface Control Register (EMI0CN as shown in SFR Definition 10.1).

For a 16-bit MOVX operation (@DPTR), the upper 6 bits of the 16-bit external data memory address word are "don't cares" (when USBFAE is cleared to 0). As a result, the 1024-byte RAM is mapped modulo style over the entire 64 k external data memory address range. For example, the XRAM byte at address 0x0000 is shadowed at addresses 0x0400, 0x0800, 0x0C00, 0x1000, etc. This is a useful feature when performing

C8051T622/3 and C8051T326/7

Table 12.1. Interrupt Summary

Interrupt Source	Interrupt Vector	Priority Order	Pending Flag	Bit addressable?	Cleared by HW?	Enable Flag	Priority Control
Reset	0x0000	Top	None	N/A	N/A	Always Enabled	Always Highest
External Interrupt 0 (INT0)	0x0003	0	IE0 (TCON.1)	Y	Y	EX0 (IE.0)	PX0 (IP.0)
Timer 0 Overflow	0x000B	1	TF0 (TCON.5)	Y	Y	ET0 (IE.1)	PT0 (IP.1)
External Interrupt 1 (INT1)	0x0013	2	IE1 (TCON.3)	Y	Y	EX1 (IE.2)	PX1 (IP.2)
Timer 1 Overflow	0x001B	3	TF1 (TCON.7)	Y	Y	ET1 (IE.3)	PT1 (IP.3)
UART0	0x0023	4	RI0 (SCON0.0) TI0 (SCON0.1)	Y	N	ES0 (IE.4)	PS0 (IP.4)
Timer 2 Overflow	0x002B	5	TF2H (TMR2CN.7) TF2L (TMR2CN.6)	Y	N	ET2 (IE.5)	PT2 (IP.5)
SPI0	0x0033	6	SPIF (SPI0CN.7) WCOL (SPI0CN.6) MODF (SPI0CN.5) RXOVRN (SPI0CN.4)	Y	N	ESPI0 (IE.6)	PSPI0 (IP.6)
SMB0	0x003B	7	SI (SMB0CN.0)	Y	N	ESMB0 (EIE1.0)	PSMB0 (EIP1.0)
USB0	0x0043	8	Special	N	N	EUSB0 (EIE1.0)	PUSB0 (EIP1.1)
RESERVED	0x004B	9	N/A	N/A	N/A	N/A	N/A
RESERVED	0x0053	10	N/A	N/A	N/A	N/A	N/A
Programmable Counter Array	0x005B	11	CF (PCA0CN.7) CCF _n (PCA0CN.n) COVF (PCA0PWM.6)	Y	N	EPCA0 (EIE1.4)	PPCA0 (EIP1.4)
RESERVED	0x0063	12	N/A	N/A	N/A	N/A	N/A
RESERVED	0x006B	13	N/A	N/A	N/A	N/A	N/A
Timer 3 Overflow	0x0073	14	TF3H (TMR3CN.7) TF3L (TMR3CN.6)	N	N	ET3 (EIE1.7)	PT3 (EIP1.7)
VBUS Level	0x007B	15	N/A	N/A	N/A	EVBUS (EIE2.0)	PVBUS (EIP2.0)
UART1	0x0083	16	RI1 (SCON1.0) TI1 (SCON1.1)	N	N	ES1 (EIE2.1)	PS1 (EIP2.1)
RESERVED	0x008B	17	N/A	N/A	N/A	N/A	N/A
Port Match	0x0093	18	None	N/A	N/A	EMAT (EIE2.3)	PMAT (EIP2.3)

C8051T622/3 and C8051T326/7

Port	P0							P1							P2
Pin Number	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6 ¹
Special Function Signals			XTAL1	XTAL2						VPP					
TX0															
RX0															
SCK															
MISO															
MOSI															
NSS ²															
SDA															
SCL															
SYSCLK															
CEX0															
CEX1															
CEX2															
ECI															
T0															
T1															
TX1															
RX1															
Pin Skip Settings	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	P0SKIP							P1SKIP							

Signal Unavailable to Crossbar

Pins P0.0-P1.6¹ are capable of being assigned to crossbar peripherals.

The crossbar peripherals are assigned in priority order from top to bottom, according to this diagram.

■ These boxes represent Port pins which can potentially be assigned to a peripheral.

□ Special Function Signals are not assigned by the crossbar. When these signals are enabled, the Crossbar should be manually configured to skip the corresponding port pins.

□ Pins can be “skipped” by setting the corresponding bit in PnSKIP to ‘1’.

Notes:

1. P1.6 is not available on all devices.
2. NSS is only pinned out when the SPI is in 4-wire mode.

Figure 17.3. Priority Crossbar Decoder Potential Pin Assignments

C8051T622/3 and C8051T326/7

SFR Definition 17.3. XBR2: Port I/O Crossbar Register 2

Bit	7	6	5	4	3	2	1	0
Name								URT1E
Type	R	R	R	R	R	R	R	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE3

Bit	Name	Function
7:1	Unused	Unused. Read = 0000000b; Write = Don't Care.
0	URT1E	UART1 I/O Output Enable Bit. 0: UART1 I/O unavailable at Port pins. 1: UART1 TX1, RX1 routed to Port pins.

17.5. Port Match

Port match functionality allows system events to be triggered by a logic value change on P0 or P1. A software controlled value stored in the PnMATCH registers specifies the expected or normal logic values of P0 and P1. A Port mismatch event occurs if the logic levels of the Port's input pins no longer match the software controlled value. This allows Software to be notified if a certain change or pattern occurs on P0 or P1 input pins regardless of the XBRn settings.

The PnMASK registers can be used to individually select which P0 and P1 pins should be compared against the PnMATCH registers. A Port mismatch event is generated if (P0 & P0MASK) does not equal (P0MATCH & P0MASK) or if (P1 & P1MASK) does not equal (P1MATCH & P1MASK).

A Port mismatch event may be used to generate an interrupt or wake the device from a low power mode, such as IDLE or SUSPEND. See the Interrupts and Power Options chapters for more details on interrupt and wake-up sources.

C8051T622/3 and C8051T326/7

18.10.3. Endpoint0 OUT Transactions

When a SETUP request is received that requires the host to transmit data to USB0, one or more OUT requests will be sent by the host. When an OUT packet is successfully received by USB0, hardware will set the OPRDY bit (E0CSR.0) to 1 and generate an Endpoint0 interrupt. Following this interrupt, firmware should unload the OUT packet from the Endpoint0 FIFO and set the SOPRDY bit (E0CSR.6) to 1.

If the amount of data required for the transfer exceeds the maximum packet size for Endpoint0, the data will be split into multiple packets. If the requested data is an integer multiple of the maximum packet size for Endpoint0 (as reported to the host), the host will send a zero-length data packet signaling the end of the transfer.

Upon reception of the first OUT token for a particular control transfer, Endpoint0 is said to be in Receive Mode. In this mode, only OUT tokens should be sent by the host to Endpoint0. The SUEND bit (E0CSR.4) is set to 1 if a SETUP or IN token is received while Endpoint0 is in Receive Mode.

Endpoint0 will remain in Receive mode until:

1. The SIE receives a SETUP or IN token.
2. The host sends a packet less than the maximum Endpoint0 packet size.
3. The host sends a zero-length packet.

Firmware should set the DATAEND bit (E0CSR.3) to 1 when the expected amount of data has been received. The SIE will transmit a STALL condition if the host sends an OUT packet after the DATAEND bit has been set by firmware. An interrupt will be generated with the STSTL bit (E0CSR.2) set to 1 after the STALL is transmitted.

C8051T622/3 and C8051T326/7

Hardware will automatically reset INPRDY to 0 when a packet slot is open in the endpoint FIFO. Note that if double buffering is enabled for the target endpoint, it is possible for firmware to load two packets into the IN FIFO at a time. In this case, hardware will reset INPRDY to 0 immediately after firmware loads the first packet into the FIFO and sets INPRDY to 1. An interrupt will not be generated in this case; an interrupt will only be generated when a data packet is transmitted.

When firmware writes 1 to the FCDT bit (EINCSRH.3), the data toggle for each IN packet will be toggled continuously, regardless of the handshake received from the host. This feature is typically used by Interrupt endpoints functioning as rate feedback communication for Isochronous endpoints. When FCDT = 0, the data toggle bit will only be toggled when an ACK is sent from the host in response to an IN packet.

18.12.2. Endpoints1-2 IN Isochronous Mode

When the ISO bit (EINCSRH.6) is set to 1, the target endpoint operates in Isochronous (ISO) mode. Once an endpoint has been configured for ISO IN mode, the host will send one IN token (data request) per frame; the location of data within each frame may vary. Because of this, it is recommended that double buffering be enabled for ISO IN endpoints.

Hardware will automatically reset INPRDY (EINCSRL.0) to 0 when a packet slot is open in the endpoint FIFO. Note that if double buffering is enabled for the target endpoint, it is possible for firmware to load two packets into the IN FIFO at a time. In this case, hardware will reset INPRDY to 0 immediately after firmware loads the first packet into the FIFO and sets INPRDY to 1. An interrupt will not be generated in this case; an interrupt will only be generated when a data packet is transmitted.

If there is not a data packet ready in the endpoint FIFO when USB0 receives an IN token from the host, USB0 will transmit a zero-length data packet and set the UNDRUN bit (EINCSRL.2) to 1.

The ISO Update feature (see Section 18.7) can be useful in starting a double buffered ISO IN endpoint. If the host has already set up the ISO IN pipe (has begun transmitting IN tokens) when firmware writes the first data packet to the endpoint FIFO, the next IN token may arrive and the first data packet sent before firmware has written the second (double buffered) data packet to the FIFO. The ISO Update feature ensures that any data packet written to the endpoint FIFO will not be transmitted during the current frame; the packet will only be sent after a SOF signal has been received.

C8051T622/3 and C8051T326/7

USB Register Definition 18.25. EOUTCNTH: USB0 OUT Endpoint Count High

Bit	7	6	5	4	3	2	1	0
Name							EOCH[1:0]	
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

USB Register Address = 0x17

Bit	Name	Function
7:2	Unused	Unused. Read = 000000b. Write = don't care.
1:0	EOCH[1:0]	OUT Endpoint Count High Byte. EOCH holds the upper 2-bits of the 10-bit number of data bytes in the last received packet in the current OUT endpoint FIFO. This number is only valid while OPRDY = 1.

C8051T622/3 and C8051T326/7

case, either a 1 or a 0 value are acceptable on the incoming slave address. Additionally, if the GC bit in register SMB0ADR is set to 1, hardware will recognize the General Call Address (0x00). Table 19.4 shows some example parameter settings and the slave addresses that will be recognized by hardware under those conditions.

Table 19.4. Hardware Address Recognition Examples (EHACK = 1)

Hardware Slave Address SLV[6:0]	Slave Address Mask SLVM[6:0]	GC bit	Slave Addresses Recognized by Hardware
0x34	0x7F	0	0x34
0x34	0x7F	1	0x34, 0x00 (General Call)
0x34	0x7E	0	0x34, 0x35
0x34	0x7E	1	0x34, 0x35, 0x00 (General Call)
0x70	0x73	0	0x70, 0x74, 0x78, 0x7C

SFR Definition 19.3. SMB0ADR: SMBus Slave Address

Bit	7	6	5	4	3	2	1	0
Name	SLV[6:0]							GC
Type	R/W							R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC7

Bit	Name	Function
7:1	SLV[6:0]	SMBus Hardware Slave Address. Defines the SMBus Slave Address(es) for automatic hardware acknowledgement. Only address bits which have a 1 in the corresponding bit position in SLVM[6:0] are checked against the incoming address. This allows multiple addresses to be recognized.
0	GC	General Call Address Enable. When hardware address recognition is enabled (EHACK = 1), this bit will determine whether the General Call Address (0x00) is also recognized by hardware. 0: General Call Address is ignored. 1: General Call Address is recognized.

C8051T622/3 and C8051T326/7

20.1. Enhanced Baud Rate Generation

The UART0 baud rate is generated by Timer 1 in 8-bit auto-reload mode. The TX clock is generated by TL1; the RX clock is generated by a copy of TL1 (shown as RX Timer in Figure 20.2), which is not user-accessible. Both TX and RX Timer overflows are divided by two to generate the TX and RX baud rates. The RX Timer runs when Timer 1 is enabled, and uses the same reload value (TH1). However, an RX Timer reload is forced when a START condition is detected on the RX pin. This allows a receive to begin any time a START is detected, independent of the TX Timer state.

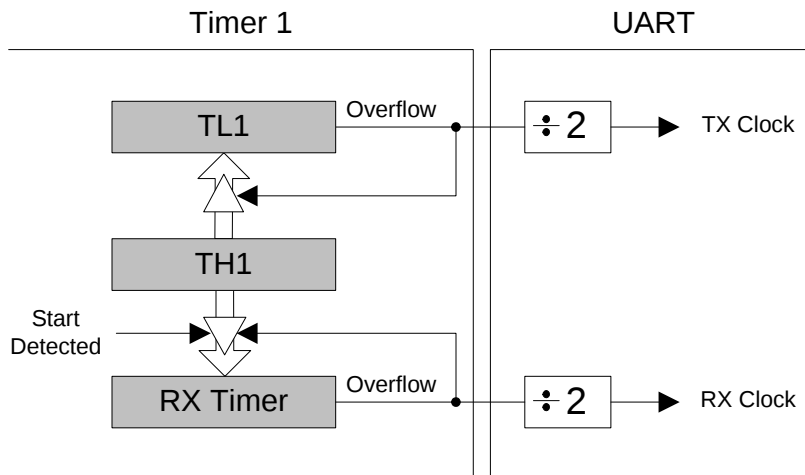


Figure 20.2. UART0 Baud Rate Logic

Timer 1 should be configured for Mode 2, 8-bit auto-reload (see Section “23.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload” on page 205). The Timer 1 reload value should be set so that overflows will occur at two times the desired UART baud rate frequency. Note that Timer 1 may be clocked by one of six sources: SYSCLK, SYSCLK/4, SYSCLK/12, SYSCLK/48, the external oscillator clock/8, or an external input T1. For any given Timer 1 clock source, the UART0 baud rate is determined by Equation 20.1-A and Equation 20.1-B.

$$A) \quad \text{UARTBaudRate} = \frac{1}{2} \times \text{T1_Overflow_Rate}$$

$$B) \quad \text{T1_Overflow_Rate} = \frac{\text{T1}_{\text{CLK}}}{256 - \text{TH1}}$$

Equation 20.1. UART0 Baud Rate

Where T1_{CLK} is the frequency of the clock supplied to Timer 1, and TH1 is the high byte of Timer 1 (reload value). Timer 1 clock frequency is selected as described in Section “23. Timers” on page 202. A quick reference for typical baud rates and system clock frequencies is given in Table 20.1 through Table 20.2. The internal oscillator may still generate the system clock when the external oscillator is driving Timer 1.

C8051T622/3 and C8051T326/7

$$\text{Baud Rate} = \frac{\text{SYSCLK}}{(65536 - (\text{SBRLH1}:\text{SBRL1}))} \times \frac{1}{2} \times \frac{1}{\text{Prescaler}}$$

Equation 21.1. UART1 Baud Rate

A quick reference for typical baud rates and system clock frequencies is given in Table 21.1.

Table 21.1. Baud Rate Generator Settings for Standard Baud Rates

	Target Baud Rate (bps)	Actual Baud Rate (bps)	Baud Rate Error	Oscillator Divide Factor	SB1PS[1:0] (Prescaler Bits)	Reload Value in SBRLH1:SBRL1
SYSCLK = 12 MHz	230400	230769	0.16%	52	11	0xFFE6
	115200	115385	0.16%	104	11	0xFFCC
	57600	57692	0.16%	208	11	0xFF98
	28800	28846	0.16%	416	11	0xFF30
	14400	14388	0.08%	834	11	0xFE5F
	9600	9600	0.0%	1250	11	0xFD8F
	2400	2400	0.0%	5000	11	0xF63C
	1200	1200	0.0%	10000	11	0xEC78
SYSCLK = 24 MHz	230400	230769	0.16%	104	11	0xFFCC
	115200	115385	0.16%	208	11	0xFF98
	57600	57692	0.16%	416	11	0xFF30
	28800	28777	0.08%	834	11	0xFE5F
	14400	14406	0.04%	1666	11	0xFCBF
	9600	9600	0.0%	2500	11	0xFB1E
	2400	2400	0.0%	10000	11	0xEC78
	1200	1200	0.0%	20000	11	0xD8F0
SYSCLK = 48 MHz	230400	230769	0.16%	208	11	0xFF98
	115200	115385	0.16%	416	11	0xFF30
	57600	57554	0.08%	834	11	0xFE5F
	28800	28812	0.04%	1666	11	0xFCBF
	14400	14397	0.02%	3334	11	0xF97D
	9600	9600	0.0%	5000	11	0xF63C
	2400	2400	0.0%	20000	11	0xD8F0
	1200	1200	0.0%	40000	11	0xB1E0

21.2. Data Format

UART1 has a number of available options for data formatting. Data transfers begin with a start bit (logic low), followed by the data bits (sent LSB-first), a parity or extra bit (if selected), and end with one or two stop bits (logic high). The data length is variable between 5 and 8 bits. A parity bit can be appended to the data, and automatically generated and detected by hardware for even, odd, mark, or space parity. The stop

C8051T622/3 and C8051T326/7

SFR Definition 21.3. SBUF1: UART1 Data Buffer

Bit	7	6	5	4	3	2	1	0
Name	SBUF1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD3

Bit	Name	Description	Write	Read
7:0	SBUF1[7:0]	Serial Data Buffer Bits. This SFR is used to both send data from the UART and to read received data from the UART1 receive FIFO.	Writing a byte to SBUF1 initiates the transmission. When data is written to SBUF1, it first goes to the Transmit Holding Register, where it is held for serial transmission. When the transmit shift register is available, data is transferred into the shift register, and SBUF1 may be written again.	Reading SBUF1 retrieves data from the receive FIFO. When read, the oldest byte in the receive FIFO is returned, and removed from the FIFO. Up to three bytes may be held in the FIFO. If there are additional bytes available in the FIFO, the RI1 bit will remain at logic 1, even after being cleared by software.

C8051T622/3 and C8051T326/7

1 at the end of the transfer. If interrupts are enabled, an interrupt request is generated when the SPIF flag is set. While the SPI0 master transfers data to a slave on the MOSI line, the addressed SPI slave device simultaneously transfers the contents of its shift register to the SPI master on the MISO line in a full-duplex operation. Therefore, the SPIF flag serves as both a transmit-complete and receive-data-ready flag. The data byte received from the slave is transferred MSB-first into the master's shift register. When a byte is fully shifted into the register, it is moved to the receive buffer where it can be read by the processor by reading SPI0DAT.

When configured as a master, SPI0 can operate in one of three different modes: multi-master mode, 3-wire single-master mode, and 4-wire single-master mode. The default, multi-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In this mode, NSS is an input to the device, and is used to disable the master SPI0 when another master is accessing the bus. When NSS is pulled low in this mode, MSTEN (SPI0CN.6) and SPIEN (SPI0CN.0) are set to 0 to disable the SPI master device, and a Mode Fault is generated (MODF, SPI0CN.5 = 1). Mode Fault will generate an interrupt if enabled. SPI0 must be manually re-enabled in software under these circumstances. In multi-master systems, devices will typically default to being slave devices while they are not acting as the system master device. In multi-master mode, slave devices can be addressed individually (if needed) using general-purpose I/O pins. Figure 22.2 shows a connection diagram between two master devices in multiple-master mode.

3-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. In this mode, NSS is not used, and is not mapped to an external port pin through the crossbar. Any slave devices that must be addressed in this mode should be selected using general-purpose I/O pins. Figure 22.3 shows a connection diagram between a master device in 3-wire master mode and a slave device.

4-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 1. In this mode, NSS is configured as an output pin, and can be used as a slave-select signal for a single SPI device. In this mode, the output value of NSS is controlled (in software) with the bit NSSMD0 (SPI0CN.2). Additional slave devices can be addressed using general-purpose I/O pins. Figure 22.4 shows a connection diagram for a master device in 4-wire master mode and two slave devices.

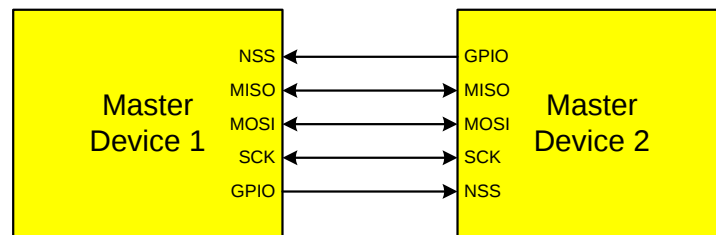


Figure 22.2. Multiple-Master Mode Connection Diagram

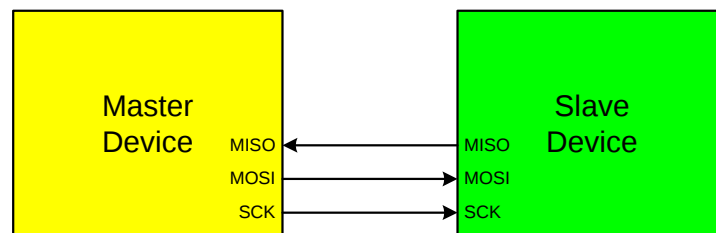


Figure 22.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram

24.1. PCA Counter/Timer

The 16-bit PCA counter/timer consists of two 8-bit SFRs: PCA0L and PCA0H. PCA0H is the high byte (MSB) of the 16-bit counter/timer and PCA0L is the low byte (LSB). Reading PCA0L automatically latches the value of PCA0H into a “snapshot” register; the following PCA0H read accesses this “snapshot” register.

Reading the PCA0L Register first guarantees an accurate reading of the entire 16-bit PCA0 counter. Reading PCA0H or PCA0L does not disturb the counter operation. The CPS2–CPS0 bits in the PCA0MD register select the timebase for the counter/timer as shown in Table 24.1.

When the counter/timer overflows from 0xFFFF to 0x0000, the Counter Overflow Flag (CF) in PCA0MD is set to logic 1 and an interrupt request is generated if CF interrupts are enabled. Setting the ECF bit in PCA0MD to logic 1 enables the CF flag to generate an interrupt request. The CF bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Clearing the CIDL bit in the PCA0MD register allows the PCA to continue normal operation while the CPU is in Idle mode.

Table 24.1. PCA Timebase Input Options

CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)
1	0	0	System clock
1	0	1	External oscillator source divided by 8*
1	1	x	Reserved.
Note: External oscillator source divided by 8 is synchronized with the system clock.			

C8051T622/3 and C8051T326/7

SFR Definition 24.4. PCA0CPMn: PCA Capture/Compare Mode

Bit	7	6	5	4	3	2	1	0
Name	PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: 0xDA (n = 0), 0xDB (n = 1), 0xDC (n = 2),

Bit	Name	Function
7	PWM16n	16-bit Pulse Width Modulation Enable. This bit enables 16-bit mode when Pulse Width Modulation mode is enabled. 0: 8 to 11-bit PWM selected. 1: 16-bit PWM selected.
6	ECOMn	Comparator Function Enable. This bit enables the comparator function for PCA module n when set to 1.
5	CAPPn	Capture Positive Function Enable. This bit enables the positive edge capture for PCA module n when set to 1.
4	CAPNn	Capture Negative Function Enable. This bit enables the negative edge capture for PCA module n when set to 1.
3	MATn	Match Function Enable. This bit enables the match function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
2	TOGn	Toggle Function Enable. This bit enables the toggle function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
1	PWMn	Pulse Width Modulation Mode Enable. This bit enables the PWM function for PCA module n when set to 1. When enabled, a pulse width modulated signal is output on the CEXn pin. 8 to 11-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0	ECCFn	Capture/Compare Flag Interrupt Enable. This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt. 0: Disable CCFn interrupts. 1: Enable a Capture/Compare Flag interrupt request when CCFn is set.
Note: When the WDTE bit is set to 1, the PCA0CPM2 register cannot be modified, and module 2 acts as the watchdog timer. To change the contents of the PCA0CPM2 register or the function of module 2, the Watchdog Timer must be disabled.		

C8051T622/3 and C8051T326/7

CONTACT INFORMATION

Silicon Laboratories Inc.

Silicon Laboratories Inc.

400 West Cesar Chavez

Austin, TX 78701

Tel: 1+(512) 416-8500

Fax: 1+(512) 416-9669

Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:

<https://www.silabs.com/support/pages/contacttechnicalsupport.aspx>

and register to submit a technical support request.

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders