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CONTENTS

Pin Identification

A1 to A21:	Address bus	P90 to P96:	Port 9
AD0 to AD15:	Address/data bus	P100 to P107:	Port 10
ADTRG:	A/D trigger input	P110 to P114:	Port 11
ANI0 to ANI11:	Analog input	P120	Port 12
ASCK0, ASCK1:	Asynchronous serial clock	$\overline{RD}$:	Read strobe
ASTB:	Address strobe	$\overline{RESET}$:	Reset
AV_{DD}:	Power supply for analog	RTP0 to RTP7:	Real-time output port
AV_{REF}:	Analog reference voltage	RTPTRG:	RTP trigger
AV_{SS}:	Ground for analog	R/$\overline{W}$:	Read/write status
BV_{DD}:	Power supply for bus interface	RXD0, RXD1:	Receive data
BV_{SS}:	Ground for bus interface	$\overline{SCK0}$ to $\overline{SCK2}$:	Serial clock
CLKOUT:	Clock output	SCL:	Serial clock
$\overline{DSTB}$:	Data strobe	SDA:	Serial data
$\overline{HLDAK}$:	Hold acknowledge	SI0 to SI2:	Serial input
$\overline{HLDRQ}$:	Hold request	SO0 to SO2:	Serial output
IC:	Internally connected	TI00, TI01, TI10,	
INTP0 to INTP6:	Interrupt request from peripherals	TI11, TI2 to TI5:	Timer input
$\overline{LBEN}$:	Lower byte enable	TO0 to TO5:	Timer output
NMI:	Non-maskable interrupt request	TXD0, TXD1:	Transmit data
P00 to P07:	Port 0	$\overline{UBEN}$:	Upper byte enable
P10 to P15:	Port 1	V_{DD}:	Power supply
P20 to P27:	Port 2	V_{PP}:	Programming power supply
P30 to P37:	Port 3	V_{SS}:	Ground
P40 to P47:	Port 4	$\overline{WAIT}$:	Wait
P50 to P57:	Port 5	$\overline{WRH}$:	Write strobe high level data
P60 to P65:	Port 6	$\overline{WRL}$:	Write strobe low level data
P70 to P77:	Port 7	X1, X2:	Crystal for main clock
P80 to P83:	Port 8	XT1, XT2:	Crystal for subclock

(2) Non-port pins

(1/2)

Pin Name	I/O	PULL	Function	Alternate Function
A1 to A4	Output	Yes	Lower address bus used for external memory expansion	P110 to P113
A5 to A12				P100/RTP0 to P107/RTP7
A13				P34/TO0
A14				P35/TO1
A15				P36/TI4/TO4
A16 to A21	Output	No	Higher address bus used for external memory expansion	P60 to P65
AD0 to AD7	I/O	No	16-bit multiplexed address/data bus used for external memory expansion	P40 to P47
AD8 to AD15				P50 to P57
ADTRG	Input	Yes	A/D converter external trigger input	P05/INTP4
ANI0 to ANI7	Input	No	Analog input to A/D converter	P70 to P77
ANI8 to ANI11	Input	No		P80 to P83
ASCK0	Input	Yes	Serial baud rate clock input for UART0 and UART1	P15/$\overline{\text{SCK1}}$
ASCK1				P25
ASTB	Output	No	External address strobe signal output	P94
AV_{DD}	—	—	Positive power supply for A/D converter	—
AV_{REF}	Input	—	Reference voltage input for A/D converter	—
AV_{SS}	—	—	Ground potential for A/D converter	—
BV_{DD}	—	—	Positive power supply for bus interface	—
BV_{SS}	—	—	Ground potential for bus interface	—
CLKOUT	Output	—	Internal system clock output	—
$\overline{\text{DSTB}}$	Output	No	External data strobe signal output	P93/$\overline{\text{RD}}$
$\overline{\text{HLDAK}}$	Output	No	Bus hold acknowledge output	P95
$\overline{\text{HLDRQ}}$	Input	No	Bus hold request input	P96
INTP0 to INTP3	Input	Yes	External interrupt request input (analog noise elimination)	P01 to P04
INTP4			External interrupt request input (digital noise elimination)	P05/ADTRG
INTP5				P06/RTPTRG
INTP6				P07
$\overline{\text{LBEN}}$	Output	No	External data bus's lower byte enable signal output	P90/$\overline{\text{WRL}}$
NMI	Input	Yes	Non-maskable interrupt request input (analog noise elimination)	P00
$\overline{\text{RD}}$	Output	No	Read strobe signal output	P93/$\overline{\text{DSTB}}$
$\overline{\text{RESET}}$	Input	–	System reset input	—
RTP0 to RTP7	Output	Yes	Real-time output port	P100/A5 to P107/A12
RTPTRG	Input	Yes	RTP external trigger input	P06/INTP5
R/$\overline{\text{W}}$	Output	No	External read/write status output	P92/$\overline{\text{WRH}}$
RXD0	Input	Yes	Serial receive data input for UART0 and UART1	P13/SI1
RXD1				P23
$\overline{\text{SCK0}}$	I/O	Yes	Serial clock I/O (3-wire type) for CSI0 to CSI2	P12/SCL[Note]

★ **Note** μPD703014AY, 703014BY, 703015AY, 703015BY, 703017AY, 70F3015BY, and 70F3017AY only

Remark PULL: On-chip pull-up resistor

2.2 Pin States

The operating states of various pins are described below with reference to their operating modes.

★ **Table 2-2. Operating States of Pins in Each Operating Mode**

Pin \ Operating State	Reset[Note 1]	HALT Mode/ Idle State	IDLE Mode/ Software STOP Mode	Bus Hold	Bus Cycle Inactive[Note 2]
AD0 to AD15	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
A1 to A15	Hi-Z	Held	Held	Held	Held[Note 3]
A16 to A21	Hi-Z	Held	Hi-Z	Hi-Z	Held[Note 3]
$\overline{\text{LBEN}}$, $\overline{\text{UBEN}}$	Hi-Z	Held	Hi-Z	Hi-Z	Held[Note 3]
R/$\overline{\text{W}}$	Hi-Z	H	Hi-Z	Hi-Z	H
$\overline{\text{DSTB}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, $\overline{\text{RD}}$	Hi-Z	H	Hi-Z	Hi-Z	H
ASTB	Hi-Z	H	Hi-Z	Hi-Z	H
$\overline{\text{HLDRQ}}$	—	Operating	—	Operating	Operating
$\overline{\text{HLDAK}}$	Hi-Z	Operating	Hi-Z	L	Operating
$\overline{\text{WAIT}}$	—	—	—	—	—
CLKOUT	Hi-Z	Operating[Note 4]	L	Operating[Note 4]	Operating[Note 4]

Notes 1. Pins (except the CLKOUT pin) are used as port pins (input mode) after reset.

2. The bus cycle inactivation timing occurs when the internal memory area is specified by the program counter (PC) in the external expansion mode.

3.
- When the external memory area has not been accessed even once after reset is released and the external expansion mode is set: Undefined
- When the bus cycle is inactivated after access to the external memory area, or when the external memory area has not been accessed even once after the external expansion mode is released and set again: The state of the external bus cycle when the external memory area accessed last is held.

4. Low level (L) when in clock output inhibit mode

Remark Hi-Z: High impedance
Held: State is held during previously set external bus cycle
L: Low-level output
H: High-level output
–: Input without sampling sampled (not acknowledged)

(9) P90 to P96 (Port 9) ··· 3-state I/O

P90 to P96 constitute a 7-bit I/O port that can be set to input or output pins in 1-bit units.

P90 to P96 can also function as control signal output pins and bus hold control signal output pins when memory is expanded externally.

During 8-bit access of port 9, the highest bit is ignored during a write operation and is read as a "0" during a read operation.

The I/O signal level uses the bus interface power supply pins BV_{DD} and BV_{SS} as a reference.

(a) Port function

P90 to P96 can be set to input or output in 1-bit units using the port 9 mode register (PM9).

(b) Alternate functions (External expansion function)

P90 to P96 can be set to operate as control signal outputs for external memory expansion using the memory expansion mode register (MM).

(i) $\overline{\text{LBEN}}$ (Lower byte enable) ··· output

This is a lower byte enable signal output pin for the external 16-bit data bus. During byte access of odd-numbered addresses, these pins are set as inactive (high level). The output changes in synchronization with the rising edge of the clock in the T1 state of the bus cycle. When the timing sets the bus cycle as inactive, the previous bus cycle's address is retained.

(ii) $\overline{\text{UBEN}}$ (Upper byte enable) ··· output

This is an upper byte enable signal output pin for the external 16-bit data bus. During byte access of even-numbered addresses, these pins are set as inactive (high level). The output changes in synchronization with the rising edge of the clock in the T1 state of the bus cycle. When the timing sets the bus cycle as inactive, the previous bus cycle's address is retained.

Access		$\overline{\text{UBEN}}$	$\overline{\text{LBEN}}$	A0
Word access		0	0	0
Halfword access		0	0	0
Byte access	Even-numbered address	1	0	0
	Odd-numbered address	0	1	1

(iii) R/$\overline{\text{W}}$ (Read/write status) ··· output

This is an output pin for the status signal pin that indicates whether the bus cycle is a read cycle or write cycle during external access. High level is set during a read cycle and low level is set during a write cycle. The output changes in synchronization with the rising edge of the clock in the T1 state of the bus cycle. High level is set when the timing sets the bus cycle as inactive.

(iv) $\overline{\text{DSTB}}$ (Data strobe) ··· output

This is an output pin for the external data bus's access strobe signal. Output becomes active (low level) during the T2 and TW states of the bus cycle. Output becomes inactive (high level) when the timing sets the bus cycle as inactive.

5.2 Non-Maskable Interrupts

Non-maskable interrupt requests are acknowledged unconditionally, even in the interrupt disabled (DI) status. NMI requests are not subject to priority control and take precedence over all the other interrupts.

The V850/SA1 includes the following two non-maskable interrupt requests.

- NMI pin input (NMI)
- Non-maskable watchdog timer interrupt request (INTWDT)

When the valid edge specified by rising edge specification register 0 (EGP0) and falling edge specification register 0 (EGN0) is detected at the NMI pin, an interrupt occurs.

INTWDT functions as the non-maskable interrupt (INTWDT) only in the state in which the WDTM4 bit of the watchdog timer mode register (WDTM) is set to 1.

While the service routine of a non-maskable interrupt is being executed (PSW.NP = 1), the acknowledgement of another non-maskable interrupt request is held pending. The pending NMI is acknowledged when PSW.NP is cleared to 0 after the original service routine of the non-maskable interrupt under execution has been terminated (by the RETI instruction). Note that if two or more NMI requests are input during the execution of the service routine for an NMI, the number of NMIs that will be acknowledged after PSW.NP goes to ‘‘0’’, is only one.

Caution Do not clear PSW.NP to 0 by the LDSR instruction during non-maskable interrupt servicing. If PSW.NP is cleared to 0, the interrupts afterwards cannot be acknowledged correctly.

5.2.3 NP flag

The NP flag is a status flag that indicates that non-maskable interrupt (NMI) servicing is under execution. This flag is set when an NMI interrupt request has been acknowledged, and masks all interrupt requests to prohibit multiple interrupts from being acknowledged.

Figure 5-4. NP Flag (NP)

After reset: 00000020H

Symbol	31	8	7	6	5	4	3	2	1	0
PSW	0		**NP**	EP	ID	SAT	CY	OV	S	Z

NP	NMI Servicing State
0	No NMI interrupt servicing
1	NMI interrupt currently being serviced

★ 5.2.4 Noise elimination of external interrupt request input pin

(1) Noise elimination of NMI and INTP0 to INTP3 pins

The noise of the NMI pin and INTP0 to INTP3 pins is eliminated by the noise eliminator using analog delay. Therefore, signals input to the NMI and INTP0 to INTP3 pins are not detected as an edge, unless they maintain their input level for a certain period. The edge is detected after a certain period has elapsed.

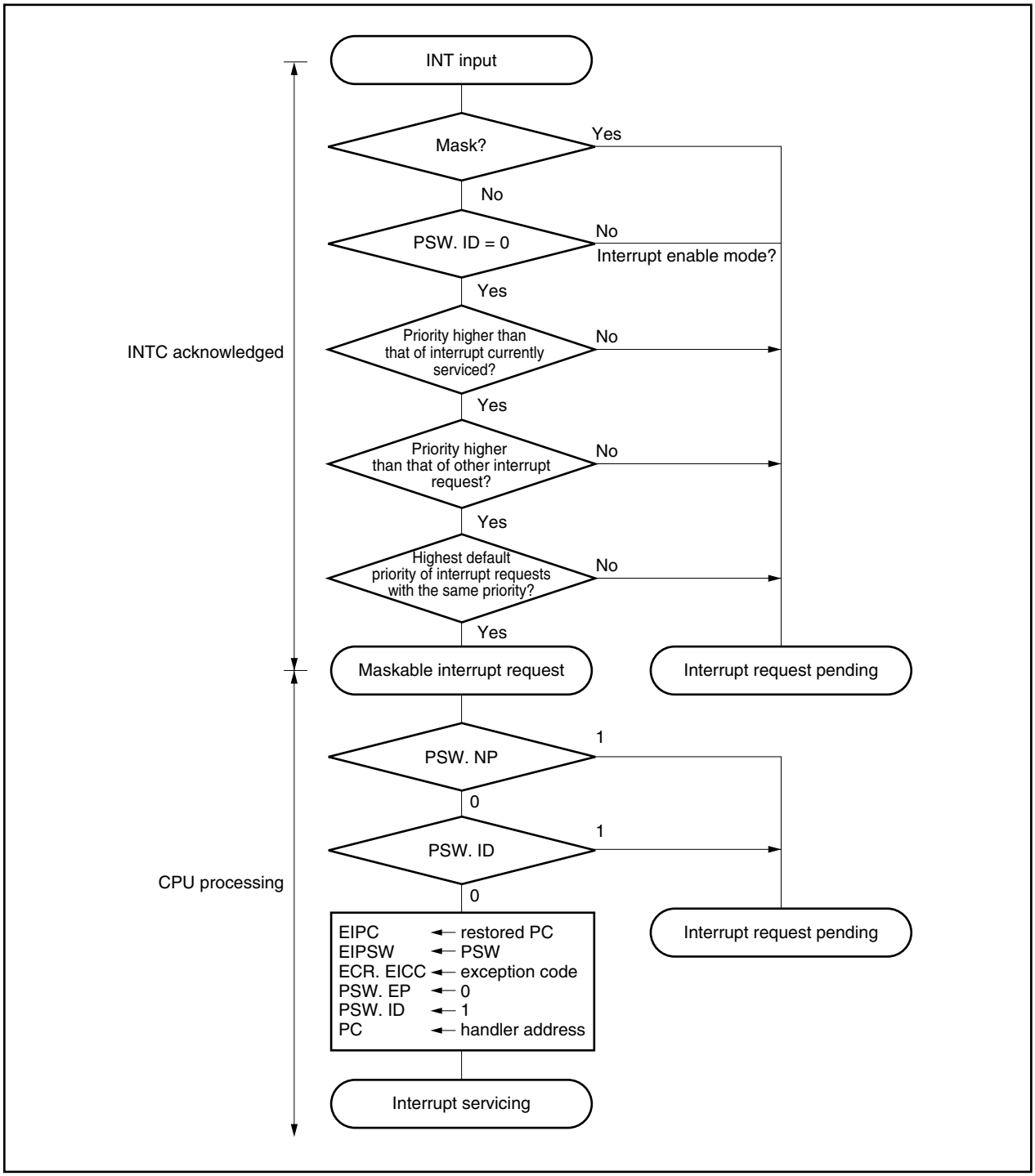
The NMI and INTP0 to INTP3 pins can be used for releasing the software STOP mode. In the software STOP mode, the system clock is not used for noise elimination because the internal system clock is stopped.

(2) Noise elimination of INTP4 to INTP6 pins

The INTP4 to INTP6 pins incorporate a digital noise eliminator. If the input level of the INTP pin is detected by the sampling clock (fxx) and the same level is not detected three successive times, the input pulse is eliminated as a noise. In the software STOP mode, the INTP4 to INTP6 pins cannot be used for releasing the software STOP mode because the internal system clock is stopped. Note the following.

- If the input pulse width is between 2 and 3 clocks, whether the input pulse is detected as a valid edge or eliminated as noise is undefined. To securely detect the level as a valid edge, the same level input of 3 clocks or more is required.
- When noise is generated in synchronization with the sampling clock, this may not be recognized as noise. In this case, eliminate the noise by adding a filter to the input pin.

Figure 5-5. Maskable Interrupt Servicing



⋆ 5.8.1 Interrupt request valid timing after EI instruction

When an interrupt request signal is generated (IF flag = 1) in the status in which the DI instruction is executed (interrupts disabled) and interrupts are not masked (MK flag = 0), seven system clocks are required from the execution of the EI instruction (interrupts enabled) to the interrupt request acknowledgement by the CPU. The CPU does not acknowledge interrupt requests if the DI instruction (interrupts disabled) is executed during the seven system clocks.

Therefore, seven system clocks worth of instruction execution clocks must be inserted after the EI instruction (interrupts enabled). However, under the following conditions, interrupt requests cannot be acknowledged even if the seven system clocks are secured, so securing under the following conditions is prohibited.

- In IDLE/software STOP mode
- An interrupt request non-sampling instruction (instruction to manipulate the PSW.ID bit) is executed
- An interrupt request control register (xxICn) is accessed

The following shows an example of program processing.

[Program processing example]

```
      DI
      :             ; (MK flag = 0)
      :             ; ← Interrupt request occurs (IF flag = 1)
      EI            ; EI instruction executed
      NOP           ; 1 system clock                              )
      NOP           ; 1 system clock                              |
      NOP           ; 1 system clock                              } Note
      NOP           ; 1 system clock                              |
      JR    LP1     ; 3 system clocks (branch to LP1 routine)     )
      :
LP1   :             ; LPI routine
      DI            ; After EI instruction execution, NOP instruction is
                      executed four times, and DI
                      instruction is executed at the eighth clock by JR instruction
```

Note Do not execute the DI instruction (PSW.ID = 1) during this period.

Remarks 1. In this example, the DI instruction is executed at the eighth clock after execution of the EI instruction, so the CPU acknowledges an interrupt request signal and performs interrupt servicing.

2. The interrupt servicing routine instructions are not executed at the eighth clock after the EI instruction execution. The interrupt servicing routine instructions are executed the four system clocks after the CPU acknowledges the interrupt request signal.

3. This example shows the case in which an interrupt request signal is generated (IF flag = 1) before the EI instruction is executed. If an interrupt request signal is generated after the EI instruction is executed, the CPU does not acknowledge the interrupt request signal if interrupts are disabled (PSW.ID = 1) for seven clocks after the IF flag is set (1).

7.2.5 Operation to output square wave

TMn can be used to output a square wave with any frequency at the interval specified by the count value set in advance to 16-bit capture/compare register n0 (CRn0).

By setting bits 0 (TOEn) and 1 (TOCn1) of 16-bit timer output control register n (TOCn) to 1, the output status of the TOn pin is reversed at the interval specified by the count value set in advance to CRn1. In this way, a square wave of any frequency can be output.

Remark n = 0, 1

Figure 7-19. Control Register Settings in Square Wave Output Mode

(a) 16-bit timer mode control registers 0, 1 (TMC0, TMC1)

					TMCn3	TMCn2	TMCn1	OVFn
TMCn	0	0	0	0	1	1	0	0

Clears and starts on match between TMn and CRn0.

(b) Capture/compare control registers 0, 1 (CRC0, CRC1)

						CRCn2	CRCn1	CRCn0
CRCn	0	0	0	0	0	0/1	0/1	1

CRn0 used as compare register

(c) 16-bit timer output control registers 0, 1 (TOC0, TOC1)

		OSPTn	OSPEn	TOCn4	LVSn	LVRn	TOCn1	TOEn
TOCn	0	0	0	0	0/1	0/1	1	1

Enables TOn output.

Reverses output on match between TMn and CRn0.

Specifies initial value of TOn output F/F.

Does not reverse output on match between TMn and CRn1.

Disables one-shot pulse output.

Remark 0/1: When these bits are reset to 0 or set to 1, other functions can be used along with the square wave output function. For details, refer to **7.1.4 (1) 16-bit timer mode control registers 0, 1 (TMC0, TMC1), 7.1.4 (2) Capture/compare control registers 0, 1 (CRC0, CRC1)**, and **7.1.4 (3) 16-bit timer output control registers 0, 1 (TOC0, TOC1)**.

7.4.3 Operation as square wave output (8-bit resolution)

A square wave with any frequency is output at the interval preset by 8-bit compare register n (CRn0).

By setting bit 0 (TOEn) of 8-bit timer mode control register n (TMCn) to 1, the output state of TOn is inverted with the count preset in CRn0 as the interval. Therefore, a square wave output with any frequency (duty factor = 50%) is possible.

Setting method

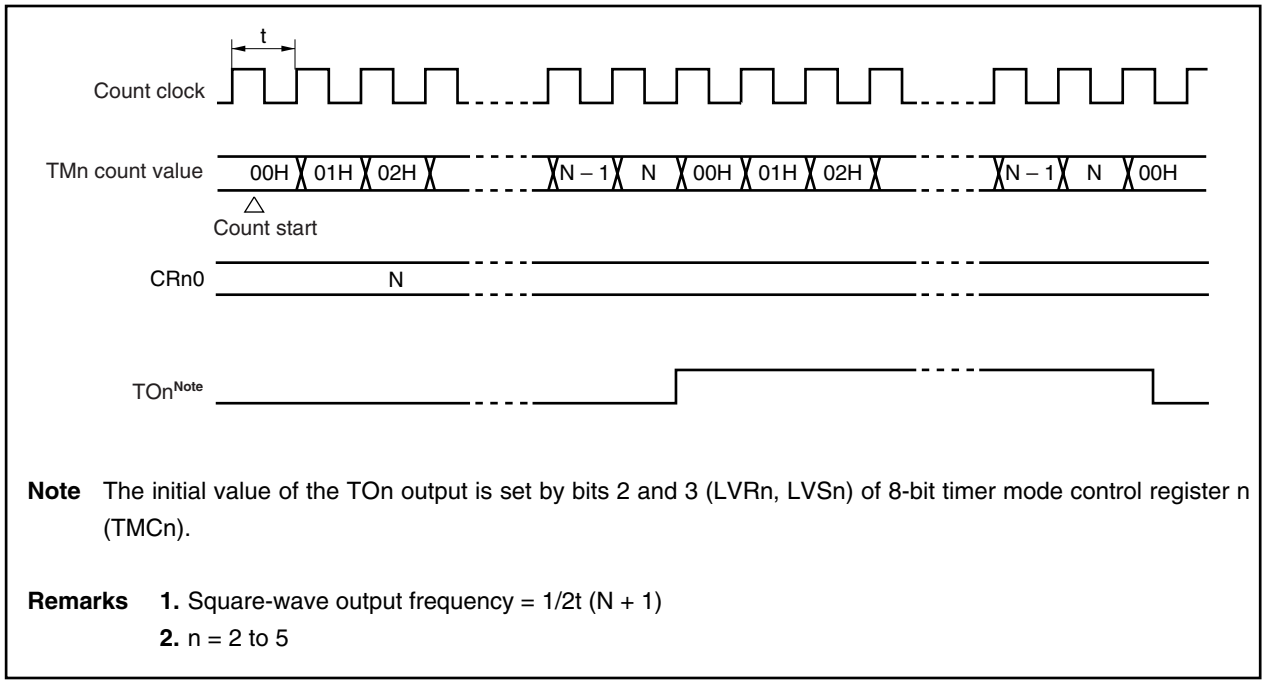
(1) Set the registers.
- Set the port latch and port mode register to 0
- TCLn, TCLn1: Select the count clock
- CRn0: Compare value
- TMCn: Clear and start mode entered when TMn and CRn0 match

LVSn	LVRn	Setting State of Timer Output Flip-flop
1	0	High-level output
0	1	Low-level output

Inversion of timer output flip-flop enabled
Timer output enabled → TOEn = 1

(2) When TCEn = 1 is set, the counter starts operating.
(3) If the values of TMn and CRn0 match, the timer output flip-flop inverts. Also, INTTMn is generated and TMn is cleared to 00H.
(4) Then, the timer output flip-flop is inverted at the same interval to output a square wave from TOn.

Figure 7-32. Timing of Square Wave Output Operation



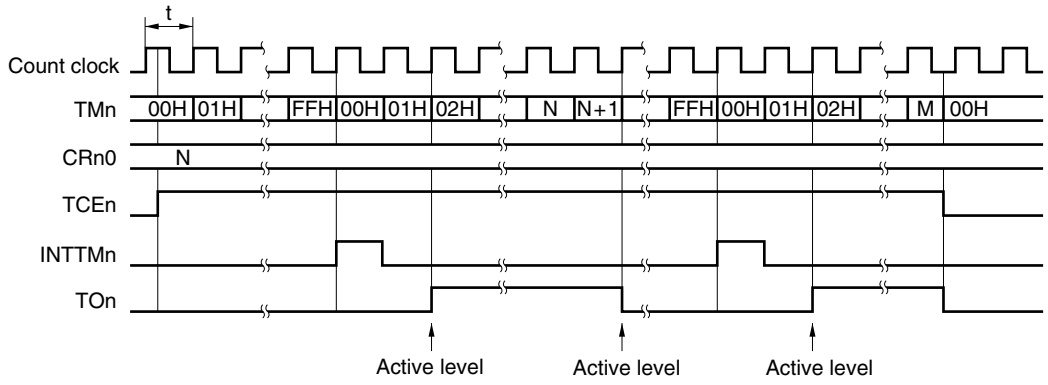
Note The initial value of the TOn output is set by bits 2 and 3 (LVRn, LVSn) of 8-bit timer mode control register n (TMCn).

Remarks **1.** Square-wave output frequency = 1/2t (N + 1)
2. n = 2 to 5

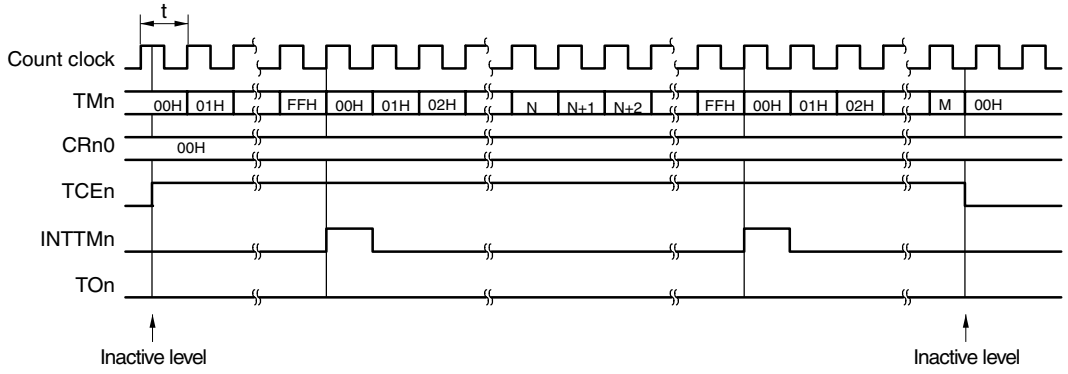
(a) Basic operation of PWM output

Figure 7-33. Timing of PWM Output

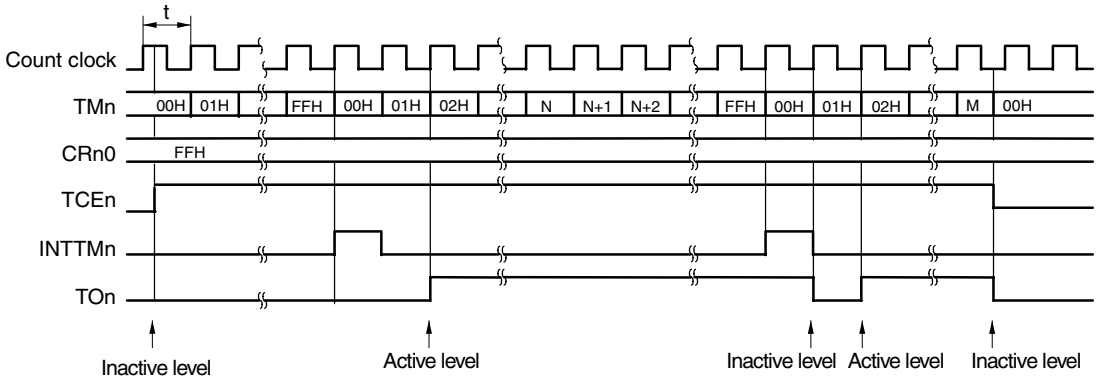
Basic operation (active level = H)



When CRn0 = 00H



When CRn0 = FFH



Remarks 1. PWM frequency = $1/2^8t$

Duty = $N/2^8$

2. n = 2 to 5

(2/3)

EXC	Detection of Extension Code Reception
0	Extension code was not received.
1	Extension code was received.

Condition for clearing (EXC = 0)	Condition for setting (EXC = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LREL = 1 • When IICE changes from 1 to 0 • When $\overline{\text{RESET}}$ is input	• When the higher four bits of the received address data are either “0000” or “1111” (set at the rising edge of the eighth clock).

COI	Detection of Matching Addresses
0	Addresses do not match.
1	Addresses match.

Condition for clearing (COI = 0)	Condition for setting (COI = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LREL = 1 • When IICE changes from 1 to 0 • When $\overline{\text{RESET}}$ is input	• When the received address matches the local address (SVA0) (set at the rising edge of the eighth clock).

TRC	Detection of Transmit/Receive Status
0	Receive status (other than transmit status). The SDA line is set to high impedance.
1	Transmit status. The value in the SO latch is enabled for output to the SDA line (valid starting at the rising edge of the first byte’s ninth clock).

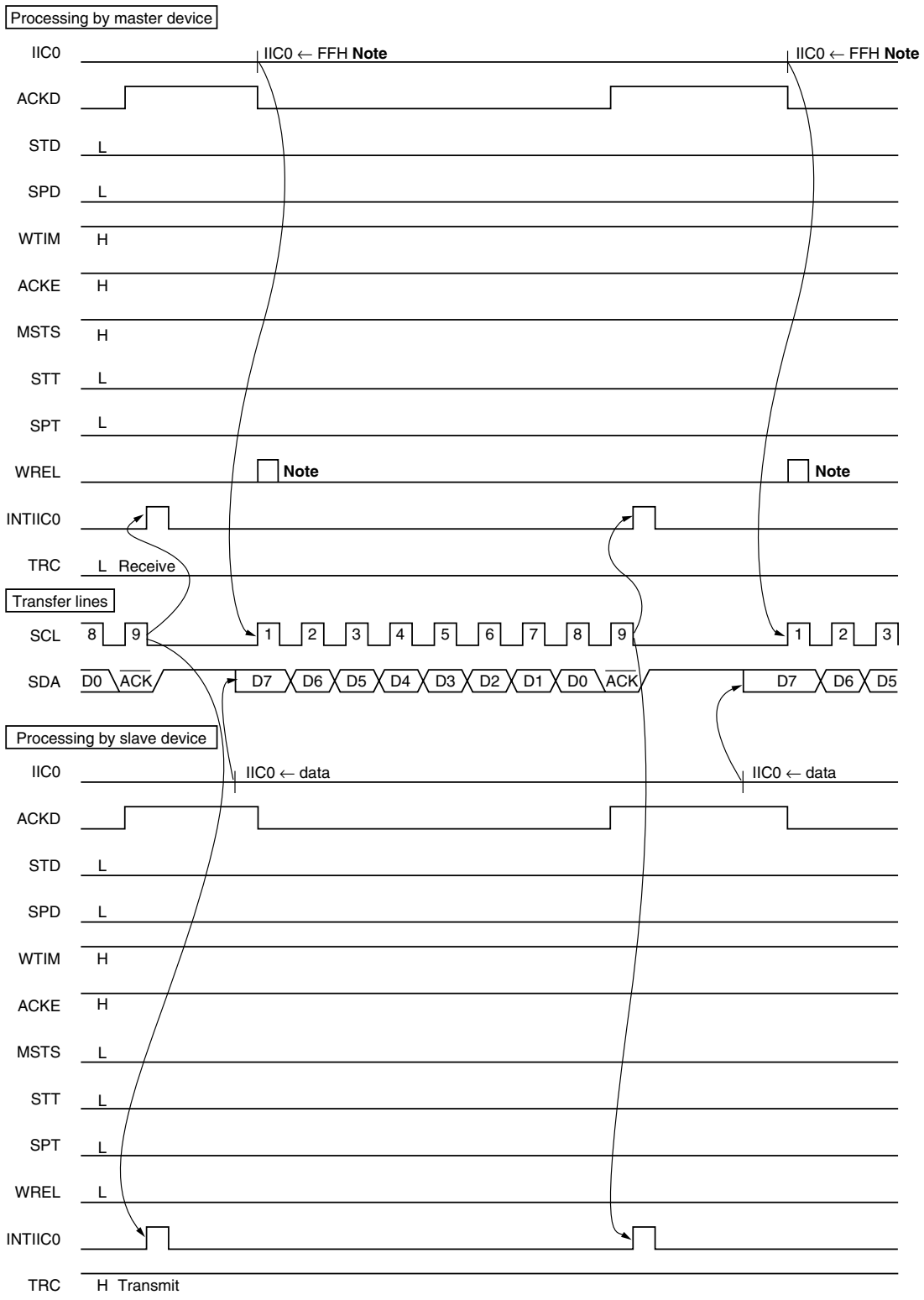
Condition for clearing (TRC = 0)	Condition for setting (TRC = 1)
• When a stop condition is detected • Cleared by LREL = 1 • When IICE changes from 1 to 0 • Cleared by WREL = 1[Note] • When $\overline{\text{ALD}}$ changes from 0 to 1 • When $\overline{\text{RESET}}$ is input Master • When “1” is output to the first byte’s LSB (transfer direction specification bit) Slave • When a start condition is detected When not used for communication	Master • When a start condition is generated Slave • When “1” is input by the first byte’s LSB (transfer direction specification bit)

Note When bit 3 (TRC) of IIC status register 0 (IICS0) is 1, if a wait is released by setting bit 5 (WREL) of IIC control register 0 (IICC0) at the 9th clock, the SDA line becomes high impedance after TRC is cleared.

Remark LREL: Bit 6 of IIC control register 0 (IICC0)
IICE: Bit 7 of IIC control register 0 (IICC0)

Figure 10-22. Example of Slave to Master Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (2/3)

(b) Data



Note To cancel master wait, write FFH to IIC0 or set WREL.

The block diagram is shown below.

Figure 11-1. Block Diagram of A/D Converter

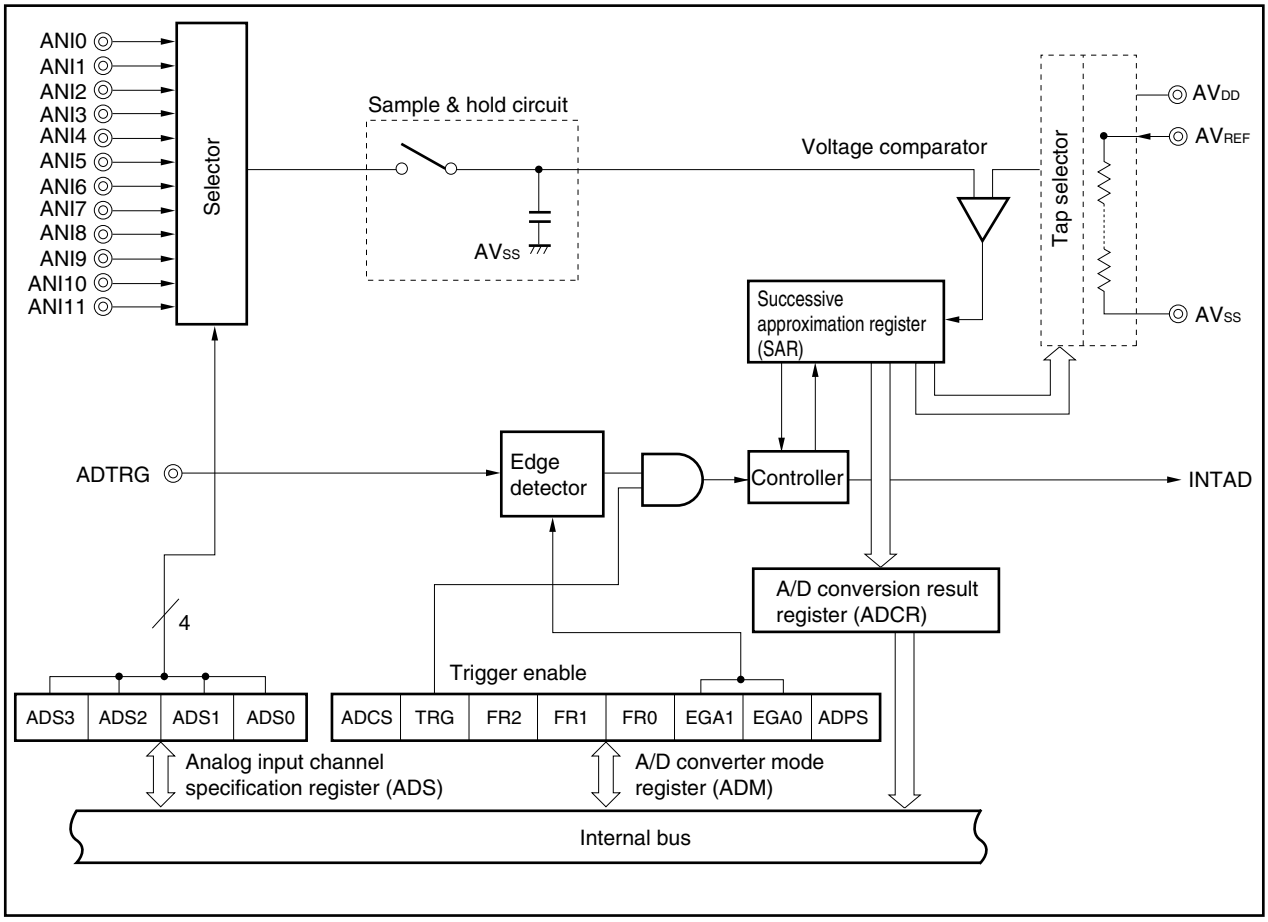
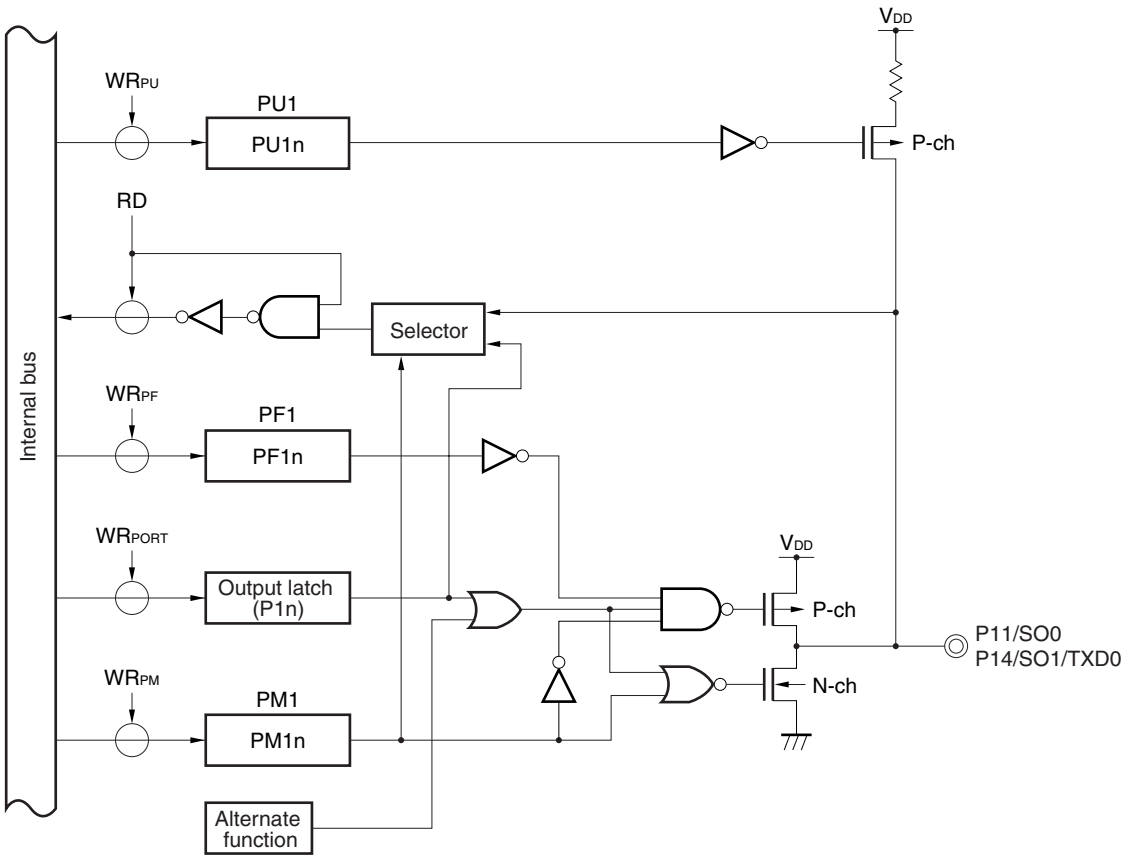


Figure 14-3. Block Diagram of P11 and P14



Remarks **1.** PU1: Pull-up resistor option register 1
PF1: Port 1 function register
PM1: Port 1 mode register
RD: Read signal of port 1
WR: Write signal of port 1

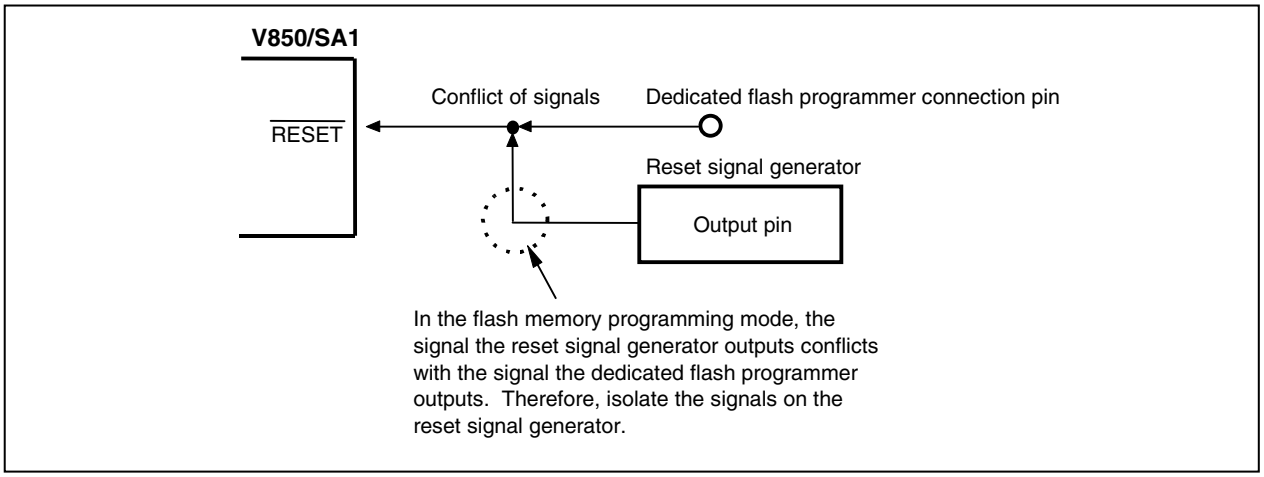
2. n = 1, 4

16.5.3 $\overline{\text{RESET}}$ pin

When connecting the reset signals of the dedicated flash programmer to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on-board, conflict of signals occurs. To avoid the conflict of signals, isolate the connection to the reset signal generator.

When a reset signal is input from the user system in the flash memory programming mode, the programming operation will not be performed correctly. Therefore, do not input signals other than the reset signals from the dedicated flash programmer.

Figure 16-10. Conflict of Signals ($\overline{\text{RESET}}$ Pin)



16.5.4 Port pin (including NMI)

When the flash memory programming mode is set, all the port pins except the pins that communicate with the dedicated flash programmer become output high-impedance status. If problems such as disabling output high-impedance status should occur to the external devices connected to the port, connect them to V_{DD} or V_{SS} via resistors.

16.5.5 Other signal pins

Connect X1, X2, XT2, and AV_{REF} to the same status as that in the normal operation mode.

16.5.6 Power supply

Supply the same power supply (V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, BV_{DD}, BV_{SS}) as when in normal operation mode.

In addition, connect V_{DD} and V_{SS} to V_{DD} and GND of the dedicated flash programmer (V_{DD} of the dedicated flash programmer has a power supply monitoring function).

(5) Internal manipulation setup parameter

If the self-programming mode is switched to the normal operation mode, the V850/SA1 must wait for 100 μs before it accesses the flash memory. In the program example in (4) above, the elapse of this wait time is ensured by setting ISETUP to "52" (@ 20 MHz operation). The total number of execution clocks in this example is 39 clocks (divh instruction (35 clocks) + add instruction (1 clock) + jne instruction (3 clocks)). Ensure that a wait time of 100 μs elapses by using the following expression.

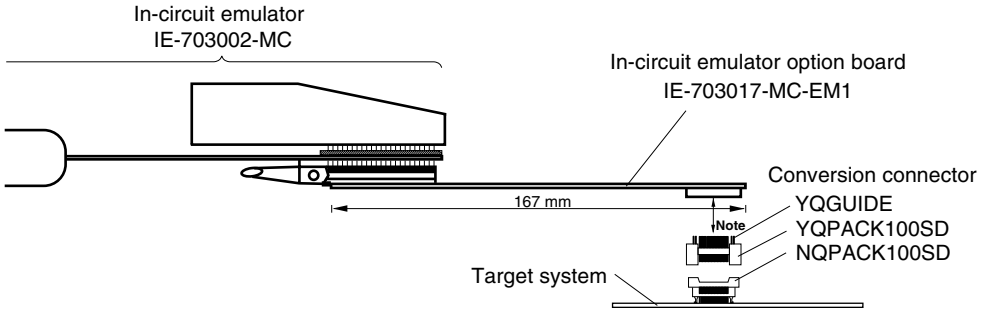
39 clocks (total number of execution clocks) $\times$ 50 ns (@ 20 MHz operation) $\times$ 52 (ISETUP) = 101.4 μs (wait time)

★ APPENDIX A NOTES ON TARGET SYSTEM DESIGN

The following shows a diagram of the connection conditions between the in-circuit emulator option board and conversion connector. Design your system making allowances for conditions such as the shape of parts mounted on the target system as shown below.

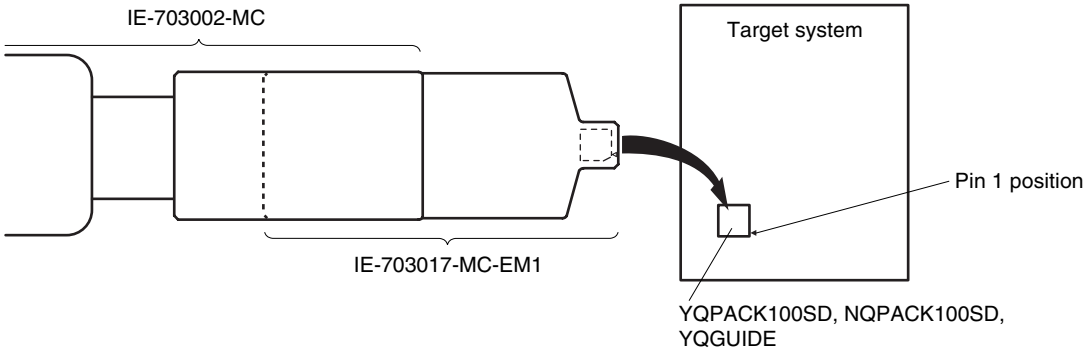
Figure A-1. 100-Pin Plastic LQFP (Fine Pitch) (14 × 14)

Side view

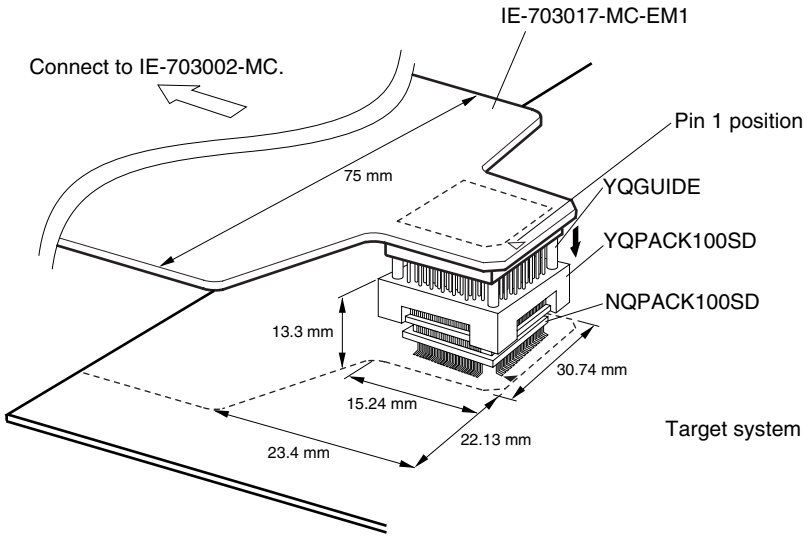


Note YQSOCKET100SDN (included with IE-703002-MC) can be inserted here to adjust the height (height: 3.2 mm).

Top view



Connection condition diagram



(5/7)

Edition	Major Revision from Previous Edition	Applied to:
3rd edition	**Figure 12-3 Correspondence Between DRAn Setup Value and Internal RAM Area** Addition	**CHAPTER 12 DMA FUNCTIONS**
	Figure 12-5 DMA Channel Control Registers 0 to 2 (DCHC0 to DCHC2) Deletion and addition of products in Note 2	
	14.2.1 (4) Block diagram (port 0) Addition	**CHAPTER 14 PORT FUNCTION**
	14.2.2 (3) Block diagrams (port 1) Addition	
	14.2.3 (3) Block diagrams (port 2) Addition	
	14.2.4 (3) Block diagrams (port 3) Addition	
	14.2.5 (1) Functions of P4 and P5 pins Modification of description	
	14.2.5 (3) Block diagram (port 4, port 5) Addition	
	14.2.6 (3) Block diagram (port 6) Addition	
	14.2.7 (2) Block diagram (port 7, port 8) Addition	
	14.2.8 (1) Function of P9 pins Modification of description	
	14.2.8 (3) Block diagrams (port 9) Addition	
	14.2.9 (3) Block diagram (port 10) Addition	
	14.2.10 (3) Block diagrams (port 11) Addition	
	14.2.11 (1) Function of P12 pin Deletion of description	
	14.2.11 (3) Block diagram (port 12) Addition	
	14.3 Setting When Port Pin Is Used for Alternate Function Addition	
	16.1.1 Erase units Addition	**CHAPTER 16 FLASH MEMORY (μPD70F3017A, 70F3017AY)**
	16.4 (3) CSI0 + HS Addition	
	Table 16-1 Signal Generation of Dedicated Flash Programmer (PG-FP3) Addition of CSI0 + HS	
	Table 16-2 Pins Used by Each Serial Interface Addition of CSI0 + HS	
	Table 16-3 List of Communication Systems Addition of CSI0 + HS	
4th edition	Addition of μPD703014B, 703014BY, 703015B, 703015BY, 70F3015B, and 70F3015BY Deletion of μPD703014AGC, 703014AYGC, 703015AGC, and 703015AYGC	Throughout
	Addition of **Table 1-1 List of V850/SA1 Products**	**INTRODUCTION**
	Addition of description to the minimum instruction execution time in **1.2 Features**	
	Deletion and addition of products in **1.4 Ordering Information**	
	Deletion and addition of products in **1.5 Pin Configuration**	
	Deletion of description in **1.6.2 (2) Bus control unit (BCU)**	
	Addition of **Table 2-1 Pin I/O Buffer Power Supplies**	**CHAPTER 2 PIN FUNCTIONS**
	Modification of description in **Table 2-2 Operating States of Pins in Each Operating Mode**	
	Modification of description in **2.3 (7) P60 to P65 (Port 6)**	
	Addition of **2.3 (13) CLKOUT (Clock Out)**	
	Addition and modification of description in **2.4 Pin I/O Circuits and Recommended Connection of Unused Pins**	
	Modification of **2.5 Pin I/O Circuits**	