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LIST OF FIGURES (2/6)

LIST OF TABLES (2/3)

(7) P60 to P65 (Port 6) ··· 3-state I/O

P60 to P65 constitute a 6-bit I/O port that can be set to input or output in 1-bit units.

★ P60 to P65 can also function as an address bus (A16 to A21) when memory is expanded externally. When the port 6 is accessed in 8-bit units, the higher 2 bits of port 6 are ignored when they are written to and 00 is read when they are read.

The I/O signal level uses the bus interface power supply pins BV_{DD} and BV_{SS} as reference.

(a) Port function

P60 to P65 can be set to input or output in 1-bit units using the port 6 mode register (PM6).

(b) Alternate functions (External expansion function)

P60 to P65 can be set as A16 to A21 using the memory expansion mode register (MM).

(i) A16 to A21 (Address 16 to 21) ··· output

These comprise an address bus that is used for external access. These pins operate as the higher 6-bit address output pins within a 22-bit address. The output changes in synchronization with the rising edge of the clock in the T1 state of the bus cycle. When the timing sets the bus cycle to inactive, the previous bus cycle's address is retained.

(8) P70 to P77 (Port 7), P80 to P83 (Port 8) ··· input

P70 to P77 constitute an 8-bit input-only port in which all the pins are fixed to input mode. P80 to P83 constitute a 4-bit input-only port in which all the pins are fixed to input.

P70 to P77 and P80 to P83 can also function as analog input pins for the A/D converter.

(a) Port function

P70 to P77 and P80 to P83 are input-only pins.

(b) Alternate functions

P70 to P77 also function as ANI0 to ANI7 and P80 to P83 also function as ANI8 to ANI11, but these alternate functions are not switchable.

(i) ANI0 to ANI11 (Analog input 0 to 11) ··· input

These are analog input pins for the A/D converter.

Connect a capacitor between these pins and AV_{SS} to prevent noise-related operation faults. Also, do not apply voltage that is outside the range for AV_{SS} and AV_{REF} to pins that are being used as inputs for the A/D converter. If it is possible for noise above the AV_{REF} range or below the AV_{SS} to enter, clamp these pins using a diode that has a small V_F value.

(b) Interrupt/exception table

The V850/SA1 increases the interrupt response speed by assigning handler addresses corresponding to interrupts/exceptions.

The collection of these handler addresses is called an interrupt/exception table, which is located in the internal ROM/on-chip flash memory area. When an interrupt/exception request is granted, execution jumps to the handler address, and the program written at that memory address is executed. The sources of interrupts/exceptions, and the corresponding addresses are shown below.

Table 3-3. Interrupt/Exception Table

Start Address of Interrupt/Exception Table	Interrupt/Exception Source
00000000H	RESET
00000010H	NMI
00000020H	INTWDT
00000040H	TRAP0n (n = 0 to F)
00000050H	TRAP1n (n = 0 to F)
00000060H	ILGOP
00000080H	INTWDTM
00000090H	INTP0
000000A0H	INTP1
000000B0H	INTP2
000000C0H	INTP3
000000D0H	INTP4
000000E0H	INTP5
000000F0H	INTP6
00000100H	INTWTI
00000110H	INTTM00
00000120H	INTTM01
00000130H	INTTM10
00000140H	INTTM11
00000150H	INTTM2
00000160H	INTTM3
00000170H	INTTM4
00000180H	INTTM5
00000190H	INTIIC0[Note]/INTCSI0
000001A0H	INTSER0
000001B0H	INTSR0/INTCSI1
000001C0H	INTST0
000001D0H	INTCSI2
000001E0H	INTSER1
000001F0H	INTSR1
00000200H	INTST1
00000210H	INTAD
00000220H	INTDMA0
00000230H	INTDMA1
00000240H	INTDMA2
00000250H	INTWT

★ **Note** Available only in the μPD703014AY, 703014BY, 703015AY, 703015BY, 703017AY, 70F3015BY, and 70F3017AY.

5.2 Non-Maskable Interrupts

Non-maskable interrupt requests are acknowledged unconditionally, even in the interrupt disabled (DI) status. NMI requests are not subject to priority control and take precedence over all the other interrupts.

The V850/SA1 includes the following two non-maskable interrupt requests.

- NMI pin input (NMI)
- Non-maskable watchdog timer interrupt request (INTWDT)

When the valid edge specified by rising edge specification register 0 (EGP0) and falling edge specification register 0 (EGN0) is detected at the NMI pin, an interrupt occurs.

INTWDT functions as the non-maskable interrupt (INTWDT) only in the state in which the WDTM4 bit of the watchdog timer mode register (WDTM) is set to 1.

While the service routine of a non-maskable interrupt is being executed (PSW.NP = 1), the acknowledgement of another non-maskable interrupt request is held pending. The pending NMI is acknowledged when PSW.NP is cleared to 0 after the original service routine of the non-maskable interrupt under execution has been terminated (by the RETI instruction). Note that if two or more NMI requests are input during the execution of the service routine for an NMI, the number of NMIs that will be acknowledged after PSW.NP goes to ‘‘0’’, is only one.

Caution Do not clear PSW.NP to 0 by the LDSR instruction during non-maskable interrupt servicing. If PSW.NP is cleared to 0, the interrupts afterwards cannot be acknowledged correctly.

5.2.1 Operation

If a non-maskable interrupt request is generated, the CPU performs the following processing, and transfers control to the handler routine.

<1> Saves the restored PC to FEPC.
<2> Saves the current PSW to FEPSW.
<3> Writes exception codes (0010H, 0020H) to the higher halfword (FECC) of ECR.
<4> Sets the NP and ID bits of the PSW and clears the EP bit.
<5> Loads the handler address (00000010H, 00000020H) of the non-maskable interrupt routine to the PC, and transfers control.

Figure 5-1. Non-Maskable Interrupt Servicing

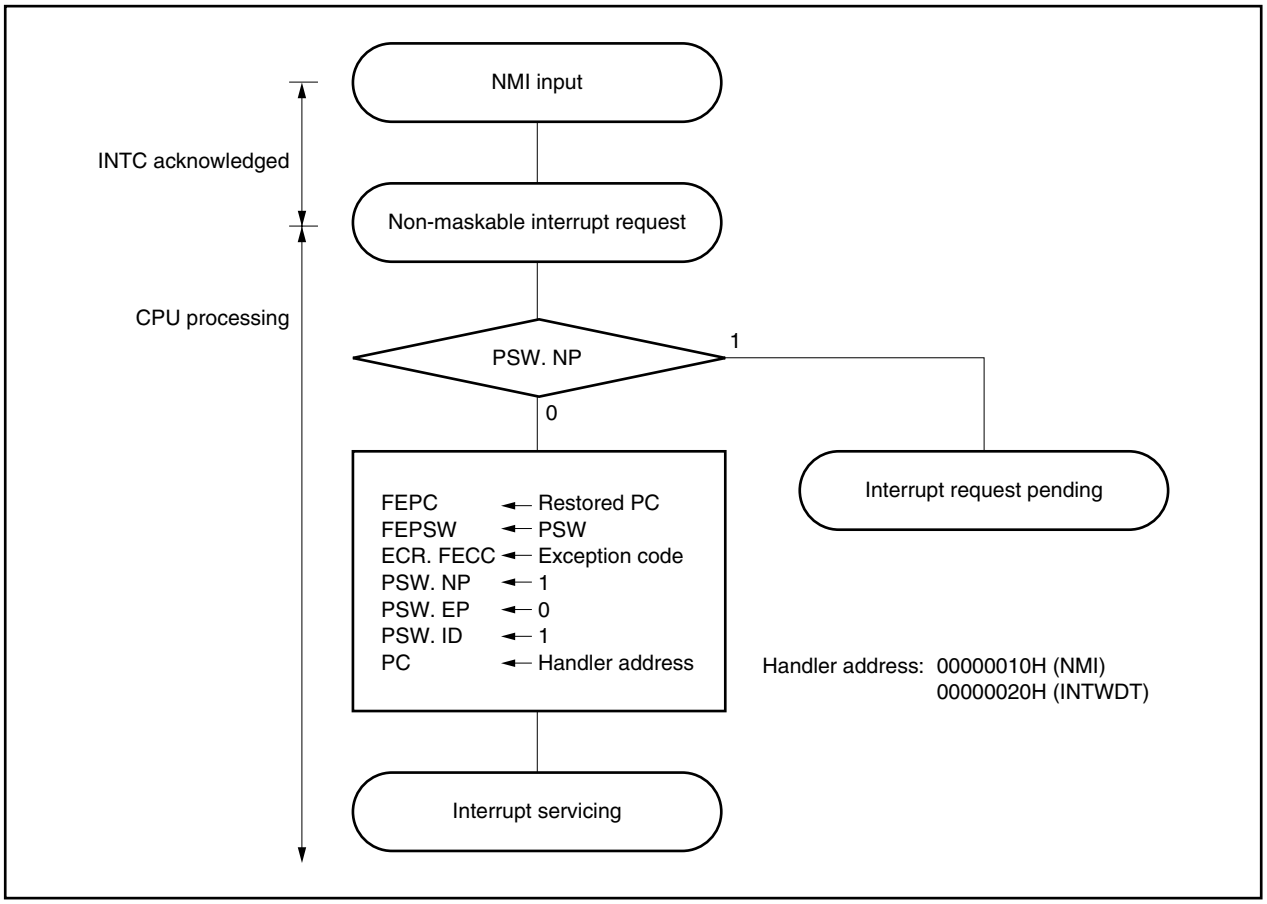
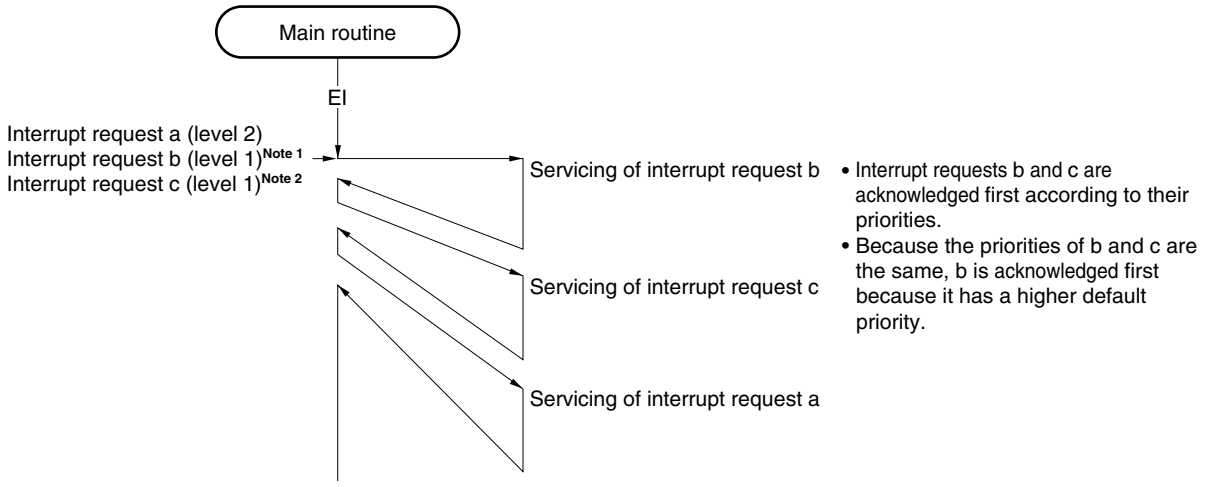


Figure 5-8. Example of Servicing Interrupt Requests Generated Simultaneously



Notes 1. Higher default priority

2. Lower default priority

Remarks 1. a, b, and c in the above figure are the names of interrupt requests shown for the sake of explanation.

2. The default priority in the above figure indicates the relative priority between two interrupt requests.

6.5 Oscillation Stabilization Time

The following shows the methods for specifying the length of the oscillation stabilization time required to stabilize the oscillator following release of software STOP mode.

(1) Release non-maskable interrupt or by unmasked interrupt request

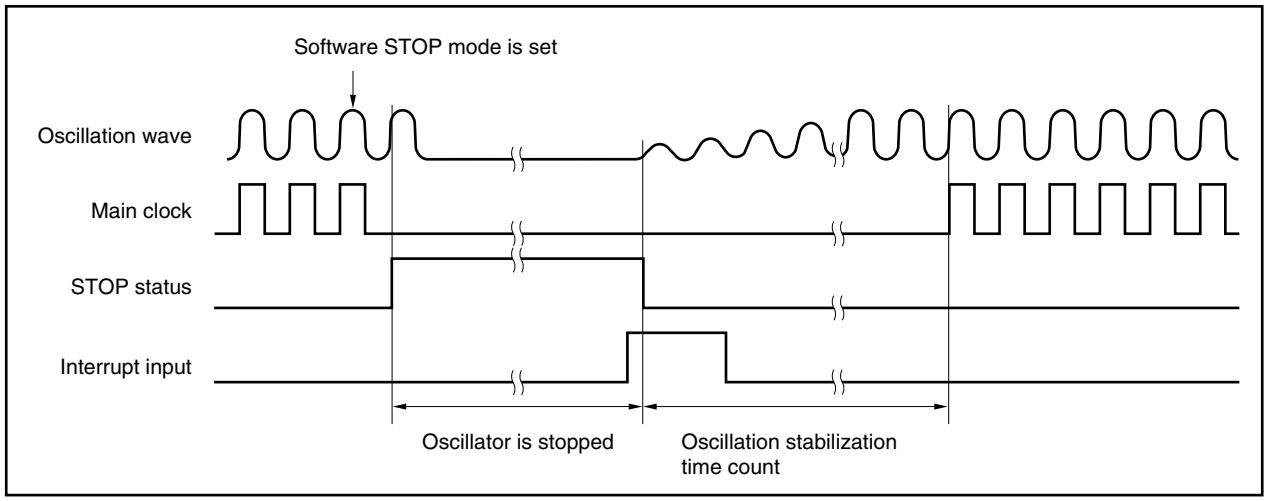
Software STOP mode is released by a non-maskable interrupt or an unmasked interrupt request. When an interrupt is input to this pin, the counter (watchdog timer) starts counting and the count time is the length of time that must elapse for stabilization of the oscillator's clock output.

The oscillation stabilization time is set by the oscillation stabilization time select register (OSTS).

Oscillation stabilization time ≒ WDT count time

After the specified amount of time has elapsed, system clock output starts and processing branches to the interrupt handler address.

Figure 6-2. Oscillation Stabilization Time



(2) Use of $\overline{\text{RESET}}$ pin to secure time ($\overline{\text{RESET}}$ pin input)

For securing time with the $\overline{\text{RESET}}$ pin, refer to **CHAPTER 15 RESET FUNCTION**.

The oscillation stabilization time is 2^{19}/fxx according to the value of the OSTS register after reset.

(2) 8-bit timer mode control registers 2 to 5 (TMC2 to TMC5)

The TMCn register makes the following six settings.

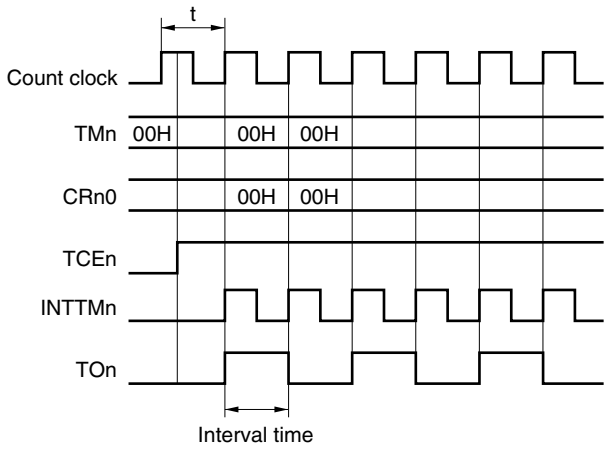
(1) Controls counting by 8-bit counter n (TMn)
(2) Selects the operating mode of 8-bit counter n (TMn)
(3) Selects the individual mode or cascade connection mode
(4) Sets the state of the timer output flip-flop
(5) Controls the timer flip-flop or selects the active level in the PWM (free-running) mode
(6) Controls timer output

TMCn is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets these registers to 04H (the hardware status is initialized to 04H, but 00H is read when read).

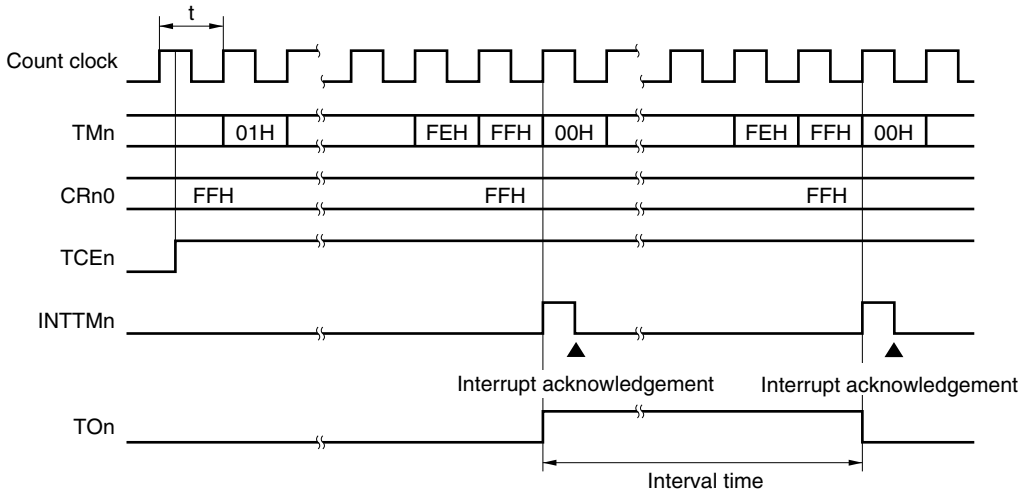
Figure 7-30. Timing of Interval Timer Operation (2/3)

When CRn0 = 00H



Remark n = 2 to 5

When CRn0 = FFH



Remark n = 2 to 5

10.2.3 Operations

CSIn has the following two operation modes.

- Operation stop mode
- 3-wire serial I/O mode

(1) Operation stop mode

Serial transfers are not performed in this mode, enabling a reduction in power consumption.

In operation stop mode, if the SIn, SOn, and $\overline{\text{SCKn}}$ pins are also used as I/O ports, they can be used as normal I/O ports as well.

(a) Register settings

Operation stop mode is set via the CSIEn bit of serial operation mode register n (CSIMn).

Figure 10-2. Settings of CSIMn (Operation Stop Mode)

After reset : 00H R/W Address: CSIM0 FFFFF2A2H
CSIM1 FFFFF2B2H
CSIM2 FFFFF2C2H

	7	6	5	4	3	2	1	0
CSIMn	CSIEn	0	0	0	0	MODEn	SCLn1	SCLn0

(n = 0 to 2)

CSIEn	SIOn Operation Enable/Disable Specification		
	Shift Register Operation	Serial Counter	Port
0	Operation disable	Clear	Port function

(3/3)

ACKD	Detection of $\overline{ACK}$
0	$\overline{ACK}$ was not detected.
1	$\overline{ACK}$ was detected.

Condition for clearing (ACKD = 0)	Condition for setting (ACKD = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock • Cleared by LREL = 1 • When IICE changes from 1 to 0 • When $\overline{RESET}$ is input	• After the SDA line is set to low level at the rising edge of the SCL's ninth clock

STD	Detection of Start Condition
0	Start condition was not detected.
1	Start condition was detected. This indicates that the address transfer period is in effect.

Condition for clearing (STD = 0)	Condition for setting (STD = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock following address transfer • Cleared by LREL = 1 • When IICE changes from 1 to 0 • When $\overline{RESET}$ is input	• When a start condition is detected

SPD	Detection of Stop Condition
0	Stop condition was not detected.
1	Stop condition was detected. The master device's communication is terminated and the bus is released.

Condition for clearing (SPD = 0)	Condition for setting (SPD = 1)
• At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition • When IICE changes from 1 to 0 • When $\overline{RESET}$ is input	• When a stop condition is detected

Remark LREL: Bit 6 of IIC control register 0 (IICC0)

IICE: Bit 7 of IIC control register 0 (IICC0)

10.3.3 I^2C bus mode functions

(1) Pin configuration

The serial clock pin (SCL) and serial data bus pin (SDA) are configured as follows.

SCL ..... This pin is used for serial clock input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.
SDA ..... This pin is used for serial data input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

Since outputs from the serial clock line and the serial data bus line are N-ch open-drain outputs, an external pull-up resistor is required.

Figure 10-7. Pin Configuration Diagram

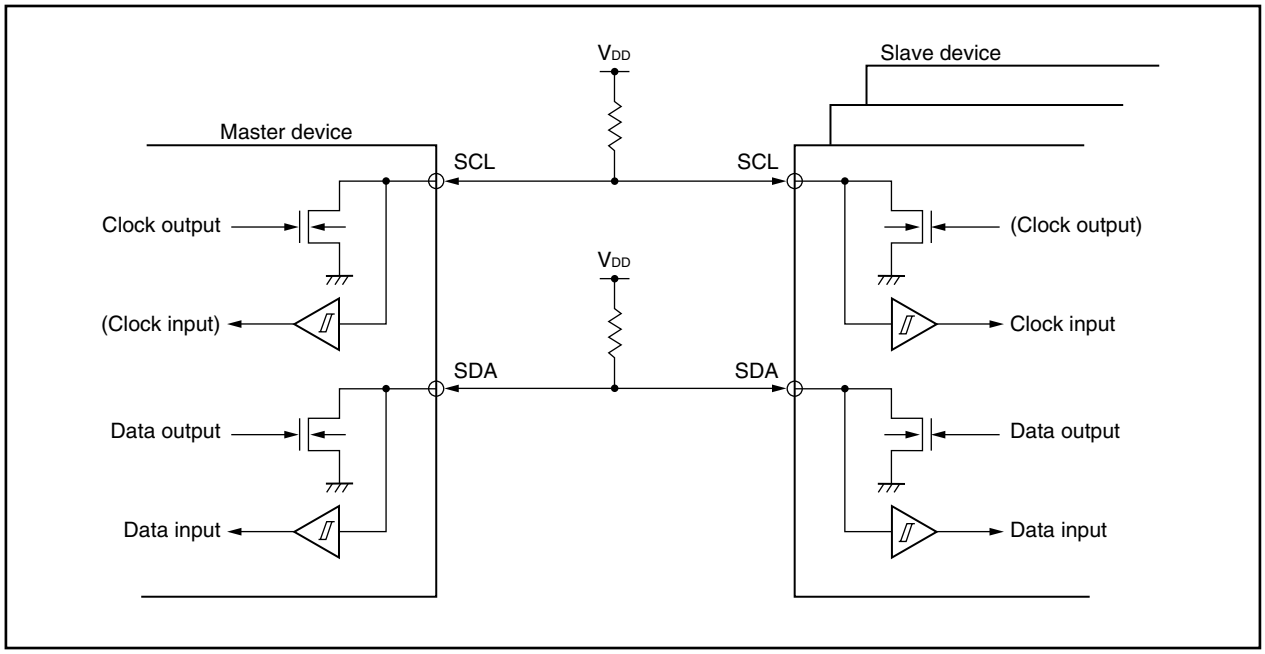
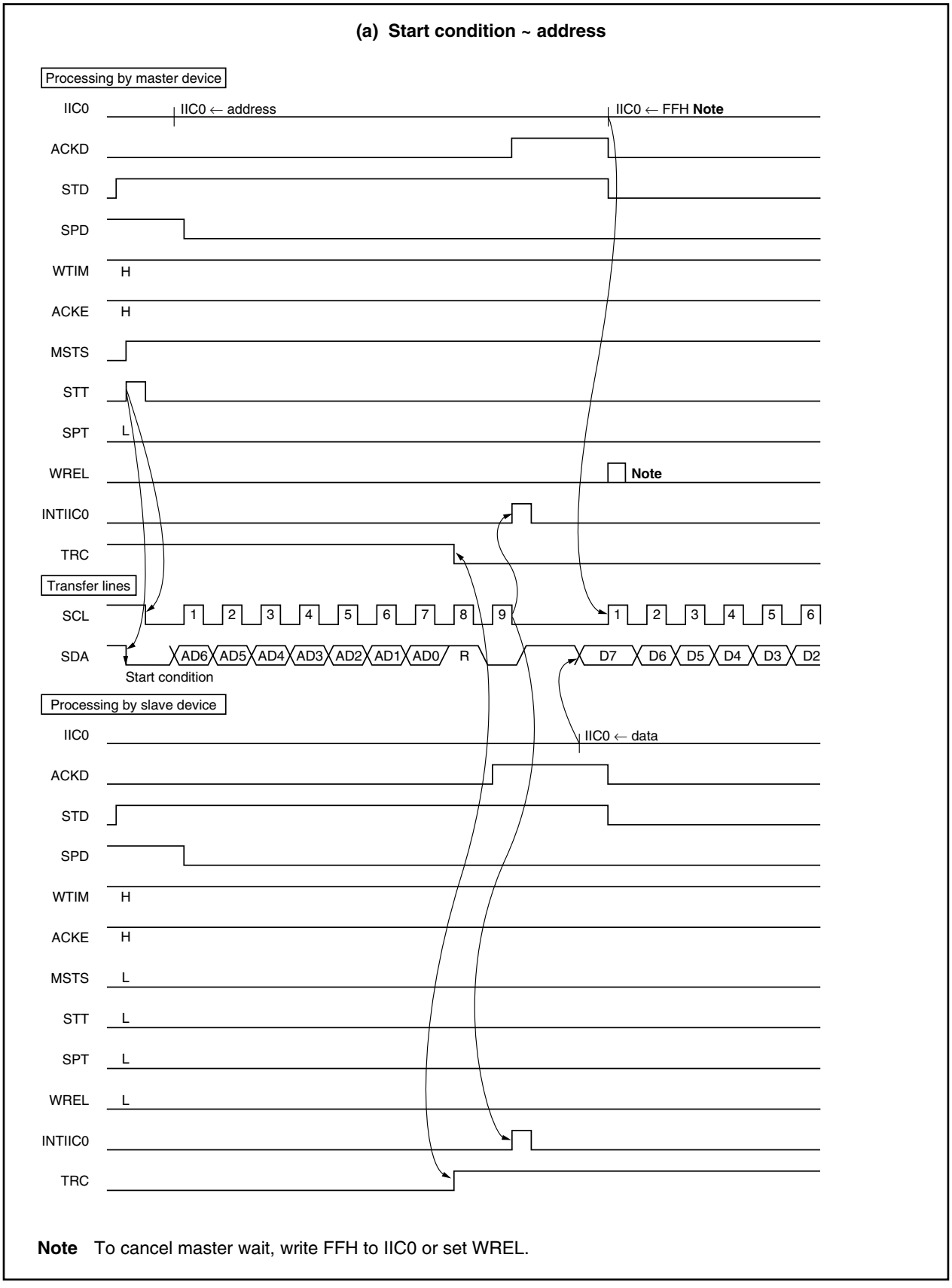


Figure 10-22. Example of Slave to Master Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)



Note To cancel master wait, write FFH to IIC0 or set WREL.

CHAPTER 11 A/D CONVERTER

11.1 Function

The A/D converter converts analog input signals into digital values with a resolution of 10 bits, and can handle 12 channels of analog input signals (ANI0 to ANI11).

(1) Hardware start

Conversion is started by trigger input (ADTRG) (rising edge, falling edge, or both rising and falling edges can be specified).

(2) Software start

Conversion is started by setting the A/D converter mode register (ADM).

One analog input channel is selected from ANI0 to ANI11, and A/D conversion is performed. If A/D conversion has been started by means of hardware start, conversion stops once it has been completed, and an interrupt request (INTAD) is generated. If conversion has been started by means of software start, conversion is performed repeatedly. Each time conversion has been completed, INTAD is generated.

Operation of the A/D converter continues in HALT mode.

14.2.9 Port 10

Port 10 is an 8-bit I/O port for which I/O settings can be controlled in 1-bit units. A pull-up resistor can be connected in 1-bit units (software pull-up function).

The pins in this port are selectable as normal outputs or N-ch open-drain outputs.

After reset: 00H R/W Address: FFFFF014H

	7	6	5	4	3	2	1	0
P10	P107	P106	P105	P104	P103	P102	P101	P100

P10n	Control of Output Data (in Output Mode) (n = 0 to 7)
0	Output 0
1	Output 1

Remark In input mode: When port 10 (P10) is read, the pin levels at that time are read. Writing to P10 writes the values to that register. This does not affect the input pins.

In output mode: When port 10 (P10) is read, the P10 values are read. Writing to P10 writes the values to that register, and those values are immediately output.

Port 10 includes the following alternate functions.

Table 14-10. Alternate Functions of Port 10

Pin Name		Alternate Function	I/O	PULL [Note]	Remark
Port 10	P100	RTP0/A5	I/O	Yes	Selectable as N-ch open-drain outputs
	P101	RTP1/A6			
	P102	RTP2/A7			
	P103	RTP3/A8			
	P104	RTP4/A9			
	P105	RTP5/A10			
	P106	RTP6/A11			
	P107	RTP7/A12			

Note Software pull-up function

(2) Control registers

(a) Port 12 mode register (PM12)

PM12 can be read/written in 1-bit or 8-bit units.

After reset: 01H R/W Address: FFFFF038H

	7	6	5	4	3	2	1	0
PM12	0	0	0	0	0	0	0	PM120

P120	Control of Input Mode
0	Output mode
1	Input mode

(b) Port 12 mode control register (PMC12)

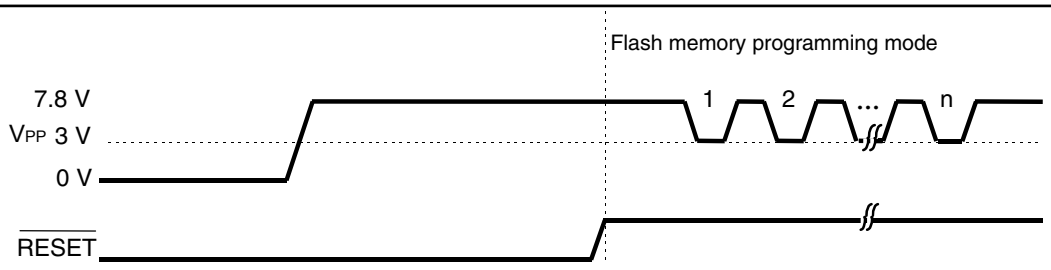
PMC12 can be read/written in 1-bit or 8-bit units.

After reset: 00H R/W Address: FFFFF058H

	7	6	5	4	3	2	1	0
PMC12	0	0	0	0	0	0	0	PMC120

PMC120	Switching of Alternate Function
0	Use as port mode
1	$\overline{\text{Use as WAIT pin}}$

Figure 16-12. Flash Memory Programming Mode



VPP	Operation Mode
0 V	Normal operation mode
7.8 V	Flash memory programming mode

16.6.3 Selection of communication mode

In the V850/SA1, the communication mode is selected by inputting a pulse (16 pulses max.) to VPP pin after switching to the flash memory programming mode. The VPP pulse is generated by the dedicated flash programmer.

The following shows the relationship between the number of pulses and the communication mode.

Table 16-5. List of Communication Modes

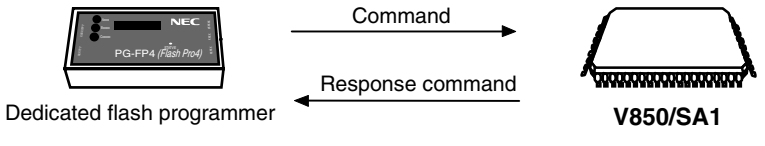
VPP Pulse	Communication Mode	Remarks
0	CSI0	V850/SA1 performs slave operation, MSB first
3	CSI0 + HS	V850/SA1 performs slave operation, MSB first
8	UART0	Communication rate: 9600 bps (at reset), LSB first
Other	RFU	Setting prohibited

Caution When UART0 is selected, the receive clock is calculated based on the reset command sent from the dedicated flash programmer after receiving the VPP pulse.

16.6.4 Communication command

The V850/SA1 communicates with the dedicated flash programmer by means of commands. The command sent from the dedicated flash programmer to the V850/SA1 is called a “command”. The response signal sent from the V850/SA1 to the dedicated flash programmer is called a “response command”.

Figure 16-13. Communication Command



(5) Internal manipulation setup parameter

If the self-programming mode is switched to the normal operation mode, the V850/SA1 must wait for 100 μs before it accesses the flash memory. In the program example in (4) above, the elapse of this wait time is ensured by setting ISETUP to "52" (@ 20 MHz operation). The total number of execution clocks in this example is 39 clocks (divh instruction (35 clocks) + add instruction (1 clock) + jne instruction (3 clocks)). Ensure that a wait time of 100 μs elapses by using the following expression.

39 clocks (total number of execution clocks) $\times$ 50 ns (@ 20 MHz operation) $\times$ 52 (ISETUP) = 101.4 μs (wait time)

(5/7)

Edition	Major Revision from Previous Edition	Applied to:
3rd edition	**Figure 12-3 Correspondence Between DRAn Setup Value and Internal RAM Area** Addition	**CHAPTER 12 DMA FUNCTIONS**
	Figure 12-5 DMA Channel Control Registers 0 to 2 (DCHC0 to DCHC2) Deletion and addition of products in Note 2	
	14.2.1 (4) Block diagram (port 0) Addition	**CHAPTER 14 PORT FUNCTION**
	14.2.2 (3) Block diagrams (port 1) Addition	
	14.2.3 (3) Block diagrams (port 2) Addition	
	14.2.4 (3) Block diagrams (port 3) Addition	
	14.2.5 (1) Functions of P4 and P5 pins Modification of description	
	14.2.5 (3) Block diagram (port 4, port 5) Addition	
	14.2.6 (3) Block diagram (port 6) Addition	
	14.2.7 (2) Block diagram (port 7, port 8) Addition	
	14.2.8 (1) Function of P9 pins Modification of description	
	14.2.8 (3) Block diagrams (port 9) Addition	
	14.2.9 (3) Block diagram (port 10) Addition	
	14.2.10 (3) Block diagrams (port 11) Addition	
	14.2.11 (1) Function of P12 pin Deletion of description	
	14.2.11 (3) Block diagram (port 12) Addition	
	14.3 Setting When Port Pin Is Used for Alternate Function Addition	
	16.1.1 Erase units Addition	**CHAPTER 16 FLASH MEMORY (μPD70F3017A, 70F3017AY)**
	16.4 (3) CSI0 + HS Addition	
	Table 16-1 Signal Generation of Dedicated Flash Programmer (PG-FP3) Addition of CSI0 + HS	
	Table 16-2 Pins Used by Each Serial Interface Addition of CSI0 + HS	
	Table 16-3 List of Communication Systems Addition of CSI0 + HS	
4th edition	Addition of μPD703014B, 703014BY, 703015B, 703015BY, 70F3015B, and 70F3015BY Deletion of μPD703014AGC, 703014AYGC, 703015AGC, and 703015AYGC	Throughout
	Addition of **Table 1-1 List of V850/SA1 Products**	**INTRODUCTION**
	Addition of description to the minimum instruction execution time in **1.2 Features**	
	Deletion and addition of products in **1.4 Ordering Information**	
	Deletion and addition of products in **1.5 Pin Configuration**	
	Deletion of description in **1.6.2 (2) Bus control unit (BCU)**	
	Addition of **Table 2-1 Pin I/O Buffer Power Supplies**	**CHAPTER 2 PIN FUNCTIONS**
	Modification of description in **Table 2-2 Operating States of Pins in Each Operating Mode**	
	Modification of description in **2.3 (7) P60 to P65 (Port 6)**	
	Addition of **2.3 (13) CLKOUT (Clock Out)**	
	Addition and modification of description in **2.4 Pin I/O Circuits and Recommended Connection of Unused Pins**	
	Modification of **2.5 Pin I/O Circuits**	