What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1512t-i-ss

FIGURE 2-1: CORE BLOCK DIAGRAM

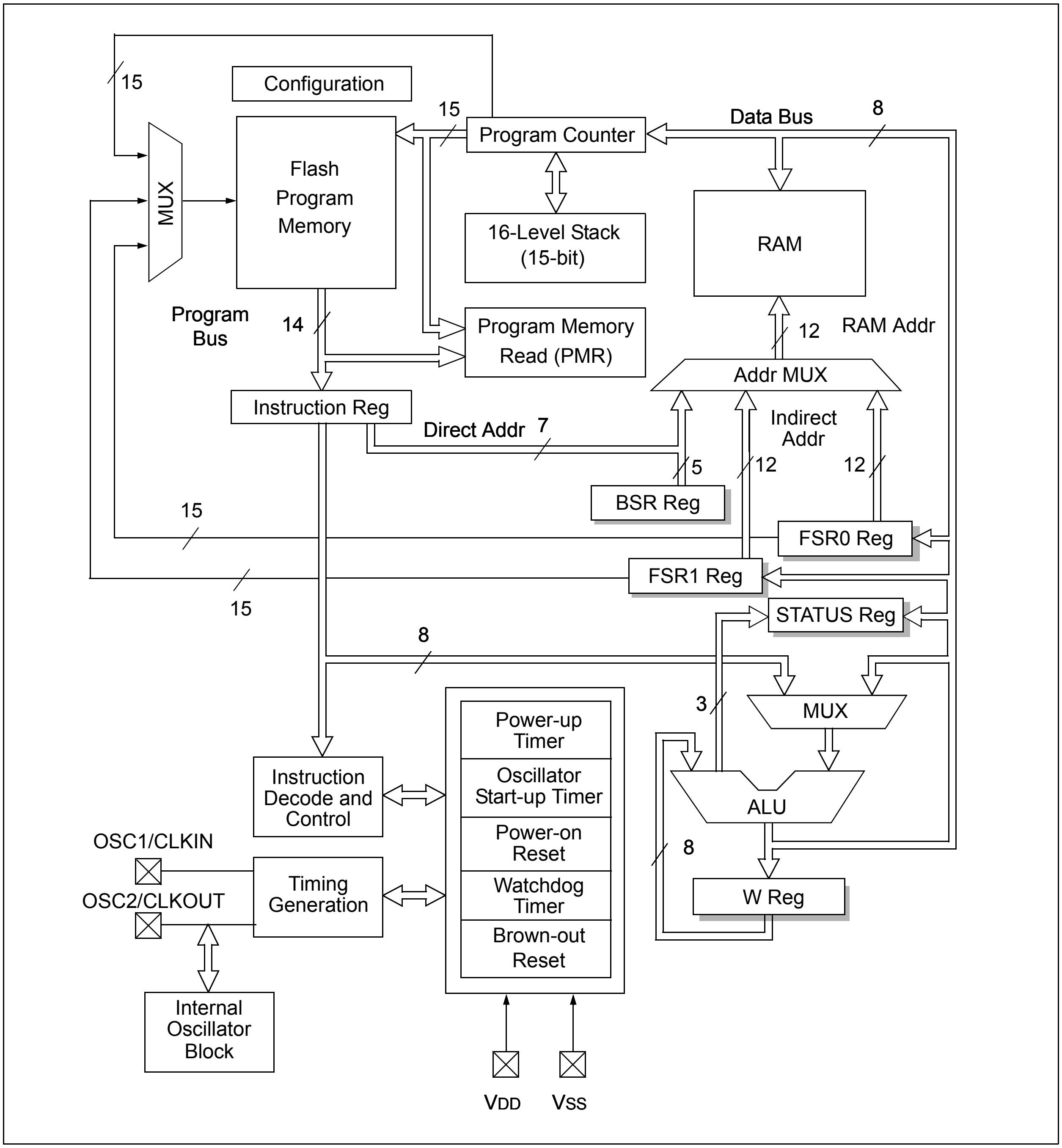


TABLE 3-5: PIC16(L)F1512/3 MEMORY MAP (BANKS 8-30)

	BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15
400h	Core Registers (Table 3-2)	480h	Core Registers (Table 3-2)	500h	Core Registers (Table 3-2)	580h	Core Registers (Table 3-2)	600h	Core Registers (Table 3-2)	680h	Core Registers (Table 3-2)	700h	Core Registers (Table 3-2)	780h	Core Registers (Table 3-2)
40Bh		48Bh		50Bh		58Bh		60Bh		68Bh		70Bh		78Bh	
40Ch	Unimplemented Read as ‘0’	48Ch	Unimplemented Read as ‘0’	50Ch	Unimplemented Read as ‘0’	58Ch	Unimplemented Read as ‘0’	60Ch	Unimplemented Read as ‘0’	68Ch	Unimplemented Read as ‘0’	70Ch	See Table 3-6	78Ch	Unimplemented Read as ‘0’
46Fh		4EFh		56Fh		5EFh		66Fh		6EFh		76Fh		7EFh	
470h	Common RAM (Accesses 70h – 7Fh)	4F0h	Common RAM (Accesses 70h – 7Fh)	570h	Common RAM (Accesses 70h – 7Fh)	5F0h	Common RAM (Accesses 70h – 7Fh)	670h	Common RAM (Accesses 70h – 7Fh)	6F0h	Common RAM (Accesses 70h – 7Fh)	770h	Common RAM (Accesses 70h – 7Fh)	7F0h	Common RAM (Accesses 70h – 7Fh)
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

	BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23
800h	Core Registers (Table 3-2)	880h	Core Registers (Table 3-2)	900h	Core Registers (Table 3-2)	980h	Core Registers (Table 3-2)	A00h	Core Registers (Table 3-2)	A80h	Core Registers (Table 3-2)	B00h	Core Registers (Table 3-2)	B80h	Core Registers (Table 3-2)
80Bh		88Bh		90Bh		98Bh		A0Bh		A8Bh		B0Bh		B8Bh	
80Ch	Unimplemented Read as ‘0’	88Ch	Unimplemented Read as ‘0’	90Ch	Unimplemented Read as ‘0’	98Ch	Unimplemented Read as ‘0’	A0Ch	Unimplemented Read as ‘0’	A8Ch	Unimplemented Read as ‘0’	B0Ch	Unimplemented Read as ‘0’	B8Ch	Unimplemented Read as ‘0’
86Fh		8EFh		96Fh		9EFh		A6Fh		AEFh		B6Fh		BEFh	
870h	Common RAM (Accesses 70h – 7Fh)	8F0h	Common RAM (Accesses 70h – 7Fh)	970h	Common RAM (Accesses 70h – 7Fh)	9F0h	Common RAM (Accesses 70h – 7Fh)	A70h	Common RAM (Accesses 70h – 7Fh)	AF0h	Common RAM (Accesses 70h – 7Fh)	B70h	Common RAM (Accesses 70h – 7Fh)	BF0h	Common RAM (Accesses 70h – 7Fh)
87Fh		8FFh		97Fh		9FFh		A7Fh		AFFh		B7Fh		BFFh	

	BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31
C00h	Core Registers (Table 3-2)	C80h	Core Registers (Table 3-2)	D00h	Core Registers (Table 3-2)	D80h	Core Registers (Table 3-2)	E00h	Core Registers (Table 3-2)	E80h	Core Registers (Table 3-2)	F00h	Core Registers (Table 3-2)	F80h	Core Registers (Table 3-2)
C0Bh		C8Bh		D0Bh		D8Bh		E0Bh		E8Bh		F0Bh		F8Bh	
C0Ch	Unimplemented Read as ‘0’	C8Ch	Unimplemented Read as ‘0’	D0Ch	Unimplemented Read as ‘0’	D8Ch	Unimplemented Read as ‘0’	E0Ch	Unimplemented Read as ‘0’	E8Ch	Unimplemented Read as ‘0’	F0Ch	Unimplemented Read as ‘0’	F8Ch	See (Table 3-7)
C6Fh		CEFh		D6Fh		DEFh		E6Fh		EEFh		F6Fh		FEFh	
C70h	Common RAM (Accesses 70h – 7Fh)	CF0h	Common RAM (Accesses 70h – 7Fh)	D70h	Common RAM (Accesses 70h – 7Fh)	DF0h	Common RAM (Accesses 70h – 7Fh)	E70h	Common RAM (Accesses 70h – 7Fh)	EF0h	Common RAM (Accesses 70h – 7Fh)	F70h	Common RAM (Accesses 70h – 7Fh)	FE0h	Common RAM (Accesses 70h – 7Fh)
C7Fh		CFFh		D7Fh		DFFh		E7Fh		EFFh		F7Fh		FEFh	

Legend: = Unimplemented data memory locations, read as ‘0’.

5.2 Clock Source Types

Clock sources can be classified as external or internal.

External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.

Internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators that are used to generate the internal system clock sources: the 16 MHz High-Frequency Internal Oscillator and the 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Select (SCS) bits in the OSCCON register. See **Section 5.3 “Clock Switching”** for additional information.

5.2.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the FOSC<2:0> bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset.
- Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to:
  - Secondary oscillator during run-time, or
  - An external clock source determined by the value of the FOSC bits.

See **Section 5.3 “Clock Switching”**for more information.

5.2.1.1 EC Mode

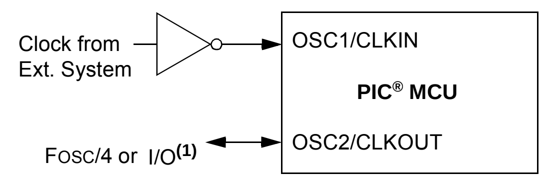
The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. Figure 5-2 shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:

- High power, 4-20 MHz (FOSC = `111`)
- Medium power, 0.5-4 MHz (FOSC = `110`)
- Low power, 0-0.5 MHz (FOSC = `101`)

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 5-2: EXTERNAL CLOCK (EC) MODE OPERATION



Note 1: Output depends upon the $\overline{\text{CLKOUTEN}}$ bit of the Configuration Words.

5.2.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 5-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

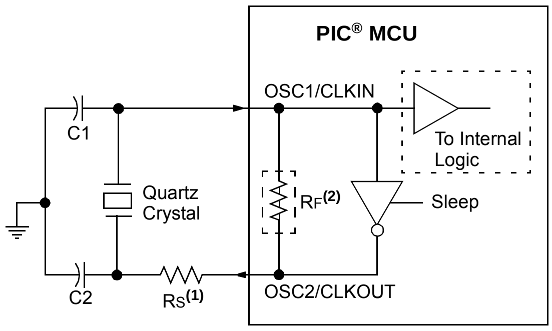
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 5-3 and Figure 5-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 5-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: A series resistor (RS) may be required for quartz crystals with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

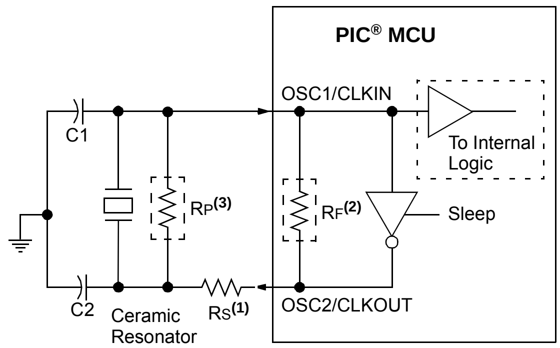
Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Applications Notes:

- *AN826, Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices* (DS00826)
- *AN849, Basic PIC® Oscillator Design* (DS00849)
- A*N943, Practical PIC® Oscillator Analysis and Design* (DS00943)
- *AN949, Making Your Oscillator Work* (DS00949)

FIGURE 5-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (RS) may be required for ceramic resonators with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

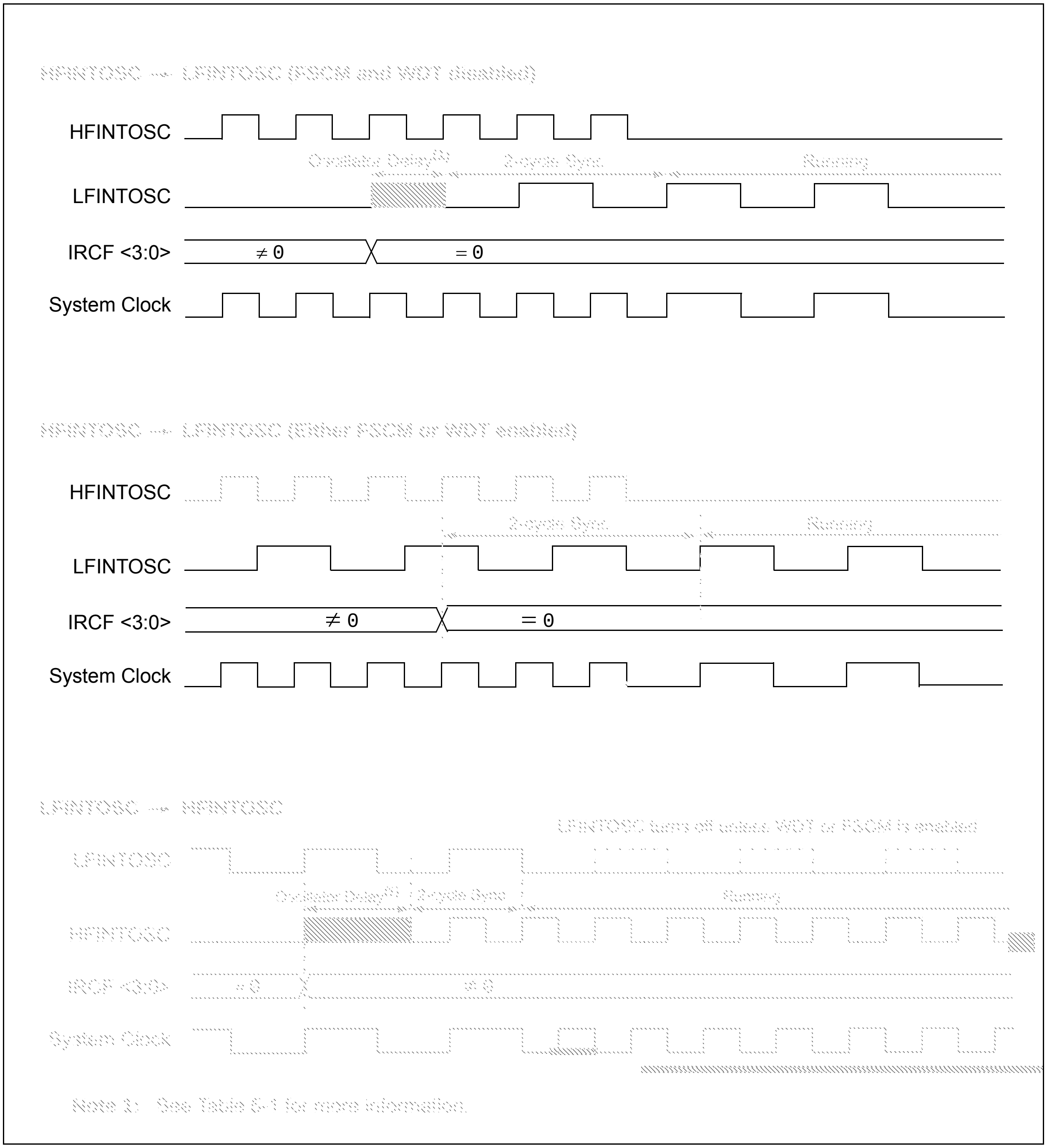
3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

5.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended unless either FSCM or Two-Speed Start-up are enabled, in which case code will continue to execute while the OST is counting. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see **Section 5.4 "Two-Speed Clock Start-up Mode"**).

FIGURE 5-7: INTERNAL OSCILLATOR SWITCH TIMING



EXAMPLE 11-2: ERASING ONE ROW OF PROGRAM MEMORY

```
; This row erase routine assumes the following:
; 1. A valid address within the erase row is loaded in ADDRH:ADDRL
; 2. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)


        BCF       INTCON,GIE     ; Disable ints so required sequences will execute properly
        BANKSEL   PMADRL
        MOVF      ADDRL,W        ; Load lower 8 bits of erase address boundary
        MOVWF     PMADRL
        MOVF      ADDRH,W        ; Load upper 6 bits of erase address boundary
        MOVWF     PMADRH
        BCF       PMCON1,CFGS    ; Not configuration space
        BSF       PMCON1,FREE    ; Specify an erase operation
        BSF       PMCON1,WREN    ; Enable writes

Required
Sequence
        MOVLW     55h            ; Start of required sequence to initiate erase
        MOVWF     PMCON2         ; Write 55h
        MOVLW     0AAh           ;
        MOVWF     PMCON2         ; Write AAh
        BSF       PMCON1,WR      ; Set WR bit to begin erase
        NOP                      ; NOP instructions are forced as processor starts
        NOP                      ; row erase of program memory.
                                 ;
                                 ; The processor stalls until the erase process is complete
                                 ; after erase processor continues with 3rd instruction

        BCF       PMCON1,WREN    ; Disable writes
        BSF       INTCON,GIE     ; Enable interrupts
```

REGISTER 12-17: WPUE: WEAK PULL-UP PORTE REGISTER(1,2)

U-0	U-0	U-0	U-0	R/W-1/1	U-0	U-0	U-0
—	—	—	—	WPUE3	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **WPUE:** Weak Pull-up Register bit
1 = Pull-up enabled
0 = Pull-up disabled

bit 2-0 **Unimplemented:** Read as '0'

Note 1: Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

TABLE 12-9: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
A(A)DCON0	—	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON	130, 147
CCPxCON	—	—	DCxB<1:0>		CCPxM<3:0>				236
PORTE	—	—	—	—	RE3	—	—	—	113
TRISE	—	—	—	—	—(1)	—	—	—	113
WPUE	—	—	—	—	WPUE3	—	—	—	114

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTE.
Note 1: Unimplemented, read as '1'.

TABLE 12-10: SUMMARY OF CONFIGURATION WORD WITH PORTE

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—		FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—	37
	7:0	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by PORTE.

16.2 ADC Operation

16.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/$\overline{\text{DONE}}$ bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

Note:	The GO/$\overline{\text{DONE}}$ bit should not be set in the same instruction that turns on the ADC. Refer to **Section 16.2.6 "A/D Conversion Procedure"**.

16.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/$\overline{\text{DONE}}$ bit
- Set the ADIF Interrupt Flag bit
- Update the ADRESH and ADRESL registers with new conversion result

16.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/$\overline{\text{DONE}}$ bit can be cleared in software. The ADRESH and ADRESL registers will be updated with the partially complete Analog-to-Digital conversion sample. Incomplete bits will match the last bit converted.

Note:	A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

16.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

16.2.5 SPECIAL EVENT TRIGGER

The Special Event Trigger allows periodic ADC measurements without software intervention, using the TRIGSEL bits of the AADCON2 register. When this trigger occurs, the GO/$\overline{\text{DONE}}$ bit is set by hardware from one of the following sources:

- CCP1
- CCP2
- Timer0 Overflow
- Timer1 Overflow
- Timer2 Match to PR2

TABLE 16-2: SPECIAL EVENT TRIGGER

Device	Source
PIC16(L)F1512/3	CCP1, CCP2, TMR0, TMR1, TMR2

Using the Special Event Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

Refer to **Section 21.0 "Capture/Compare/PWM Modules"**, **Section 17.0 "Timer0 Module"**, **Section 18.0 "Timer1 Module with Gate Control"**, and **Section 19.0 "Timer2 Module"** for more information.

TABLE 16-3: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	—	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON	130
ADCON1	ADFM	ADCS<2:0>			—	—	ADPREF<1:0>		131
ADRES0H	A/D Result Register High								132, 133
ADRES0L	A/D Result Register Low								132, 133
ANSELA	—	—	ANSA5	—	ANSA3	ANSA2	ANSA1	ANSA0	104
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	108
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	111
CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>				236
CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>				236
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	—	—	ADFVR<1:0>		120
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	69
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	70
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	72
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	103
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	107
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	110

Legend: — = unimplemented read as '0'. Shaded cells are not used for ADC module.

16.5 Hardware Capacitive Voltage Divider (CVD) Module

The hardware Capacitive Voltage Divider (CVD) module is a peripheral which allows the user to perform a relative capacitance measurement on any ADC channel using the internal ADC sample and hold capacitance as a reference. This relative capacitance measurement can be used to implement capacitive touch or proximity sensing applications.

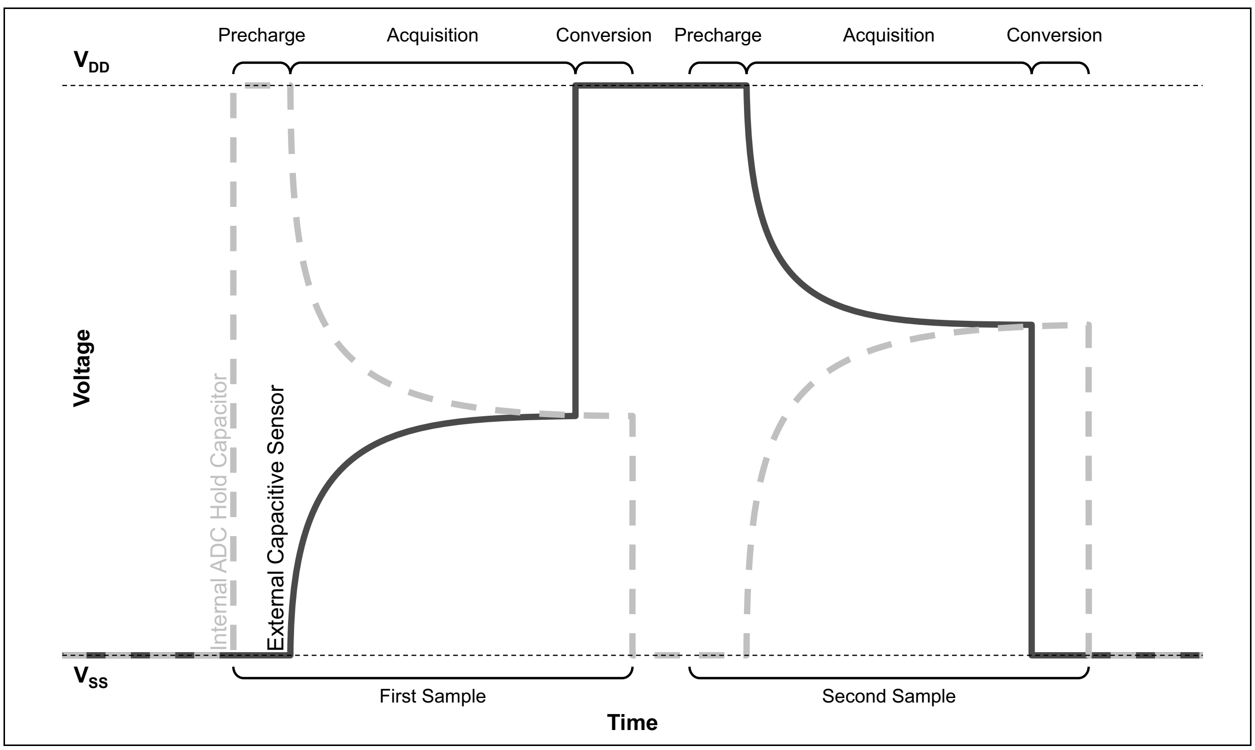
The CVD operation begins with the ADC's internal sample and hold capacitor (CHOLD) being disconnected from the path which connects it to the external capacitive sensor node. While disconnected, CHOLD is pre-charged to VDD or VSS while the path to the sensor node is also discharged to VDD or VSS – typically this node is discharged to the level opposite that of CHOLD. When the pre-charge phase is complete, the VDD/VSS bias paths for the two nodes are shut off and CHOLD and the path to the external sensor node are re-connected, at which time the acquisition phase of the CVD operation begins. During acquisition, a capacitive voltage divider is formed between the pre-charged CHOLD and sensor nodes which results in a final voltage level settling on CHOLD which is determined by the capacitances and pre-charge levels of the two nodes involved. After acquisition, the ADC converts the voltage level held on CHOLD. This process is then usually repeated with the selected pre-charge levels for both the CHOLD and sensor nodes inverted. Figure 16-6 shows the waveform for two inverted CVD measurements, which is also known is differential CVD measurement.

In a typical application, an Analog-to-Digital Converter (ADC) channel is attached to a pad on a Printed Circuit Board (PCB), which is electrically isolated from the end user. A capacitive change is detected on the ADC channel using the CVD conversion method when the end user places a finger over the PCB pad, the developer then can implement software to detect a touch or proximity event or change. Key features of this module include:

- Automated double sample conversions
- Two result registers
- Inversion of second sample
- 7-bit pre-charge timer
- 7-bit acquisition timer
- Two guard ring output drives
- Adjustable sample and hold capacitor array

Note:	For more information on capacitive voltage divider sensing method refer to the Application Note *AN1478, mTouch™ Sensing Solution Acquisition Methods Capacitive Voltage Divider* (DS01478).

FIGURE 16-6: DIFFERENTIAL CVD MEASUREMENT WAVEFORM



16.6.11 HARDWARE CVD REGISTER MAPPING

The hardware CVD module is an enhanced expansion of the standard ADC module as stated in **Section 16.0 "Analog-to-Digital Converter (ADC) Module"** and is backward compatible with the other devices in this family. Control of the standard ADC module uses Bank 1 registers, see Table 16-4. This set of registers is mapped into Bank 14 with the control registers for the hardware CVD module. Although this subset of registers has different names, they are identical. Since the registers for the standard ADC are mapped into the Bank 14 address space, any changes to registers in Bank 1 will be reflected in Bank 14 and vice-versa.

TABLE 16-4: HARDWARE CVD REGISTER MAPPING

[Bank 14 Address]	[Bank 1 Address]
Hardware CVD	**ADC**
[711h] AADCON0(1)	[09Dh] ADCON0(1)
[712h] AADCON1(1)	[09Eh] ADCON1(1)
[713h] AADCON2	
[714h] AADCON3	
[715h] AADSTAT	
[716h] AADPRE	
[717h] AADACQ	
[718h] AADGRD	
[719h] AADCAP	
[71Ah] AADRES0L(1)	[09Bh] ADRES0L(1)
[71Bh] AADRES0H(1)	[09Ch] ADRES0H(1)
[71Ch] AADRES1L	
[71Dh] AADRES1H	

Note 1: Register is mapped in Bank 1 and Bank 14, using different names in each bank.

17.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A software programmable prescaler is available for exclusive use with Timer0. The prescaler is enabled by clearing the PSA bit of the OPTION_REG register.

Note:	The Watchdog Timer (WDT) uses its own independent prescaler.

There are eight prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION_REG register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be disabled by setting the PSA bit of the OPTION_REG register.

The prescaler is not readable or writable. All instructions writing to the TMR0 register will clear the prescaler.

17.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The TMR0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The TMR0IF bit can only be cleared in software. The Timer0 interrupt enable is the TMR0IE bit of the INTCON register.

Note:	The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.

17.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in **Section 25.0 “Electrical Specifications”**.

17.1.6 OPERATION DURING SLEEP

Timer0 cannot operate while the processor is in Sleep mode. The contents of the TMR0 register will remain unchanged while the processor is in Sleep mode.

19.0 TIMER2 MODULE

The Timer2 module incorporates the following features:

- 8-bit Timer and Period registers (TMR2 and PR2, respectively)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4, 1:16, and 1:64)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on TMR2 match with PR2, respectively
- Optional use as the shift clock for the MSSP modules

See Figure 19-1 for a block diagram of Timer2.

FIGURE 19-1: TIMER2 BLOCK DIAGRAM

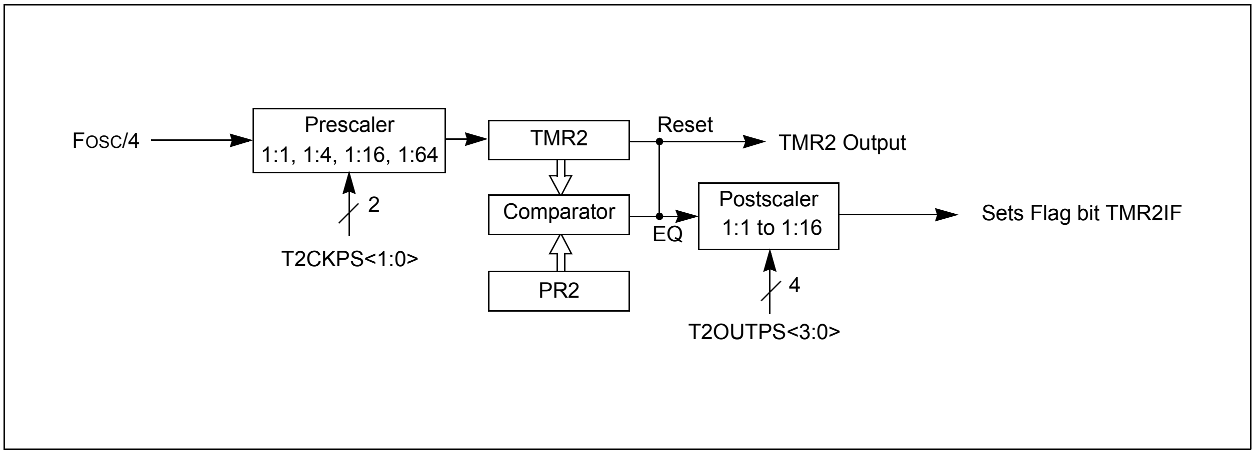
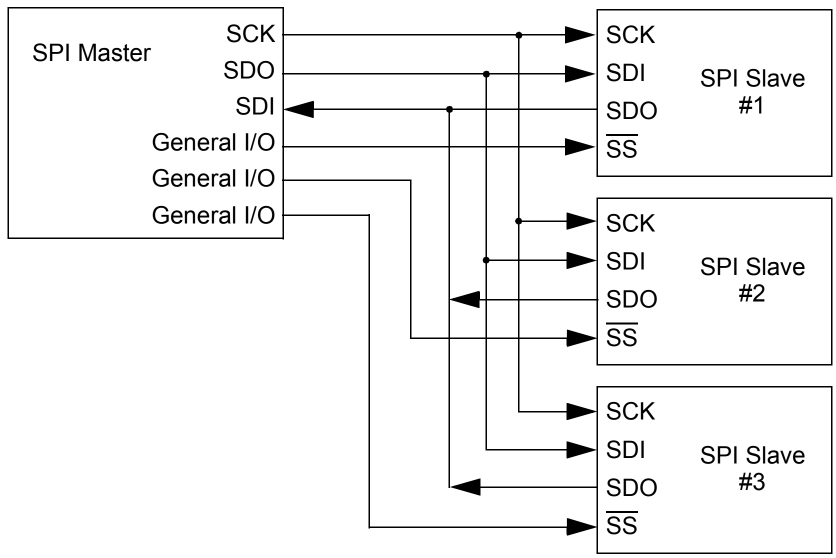


FIGURE 20-4: SPI MASTER AND MULTIPLE SLAVE CONNECTION



20.2.1 SPI MODE REGISTERS

The MSSP module has five registers for SPI mode operation. These are:

- MSSP STATUS register (SSPSTAT)
- MSSP Control Register 1 (SSPCON1)
- MSSP Control Register 3 (SSPCON3)
- MSSP Data Buffer register (SSPBUF)
- MSSP Address register (SSPADD)
- MSSP Shift Register (SSPSR) (Not directly accessible)

SSPCON1 and SSPSTAT are the control and STATUS registers in SPI mode operation. The SSPCON1 register is readable and writable. The lower six bits of the SSPSTAT are read-only. The upper two bits of the SSPSTAT are read/write.

In SPI master mode, SSPADD can be loaded with a value used in the Baud Rate Generator. More information on the Baud Rate Generator is available in **Section 20.7 “Baud Rate Generator”**.

SSPSR is the shift register used for shifting data in and out. SSPBUF provides indirect access to the SSPSR register. SSPBUF is the buffer register to which data bytes are written, and from which data bytes are read.

In receive operations, SSPSR and SSPBUF together create a buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSPIF interrupt is set.

During transmission, the SSPBUF is not buffered. A write to SSPBUF will write to both SSPBUF and SSPSR.

20.2.2 SPI MODE OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPCON1<5:0> and SSPSTAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

To enable the serial port, SSP Enable bit, SSPEN of the SSPCON1 register, must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, re-initialize the SSPCON registers and then set the SSPEN bit. This configures the SDI, SDO, SCK and $\overline{SS}$ pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed as follows:

- SDI must have corresponding TRIS bit set
- SDO must have corresponding TRIS bit cleared
- SCK (Master mode) must have corresponding TRIS bit cleared
- SCK (Slave mode) must have corresponding TRIS bit set
- $\overline{SS}$ must have corresponding TRIS bit set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

22.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 22-1 and Figure 22-2.

FIGURE 22-1: EUSART TRANSMIT BLOCK DIAGRAM

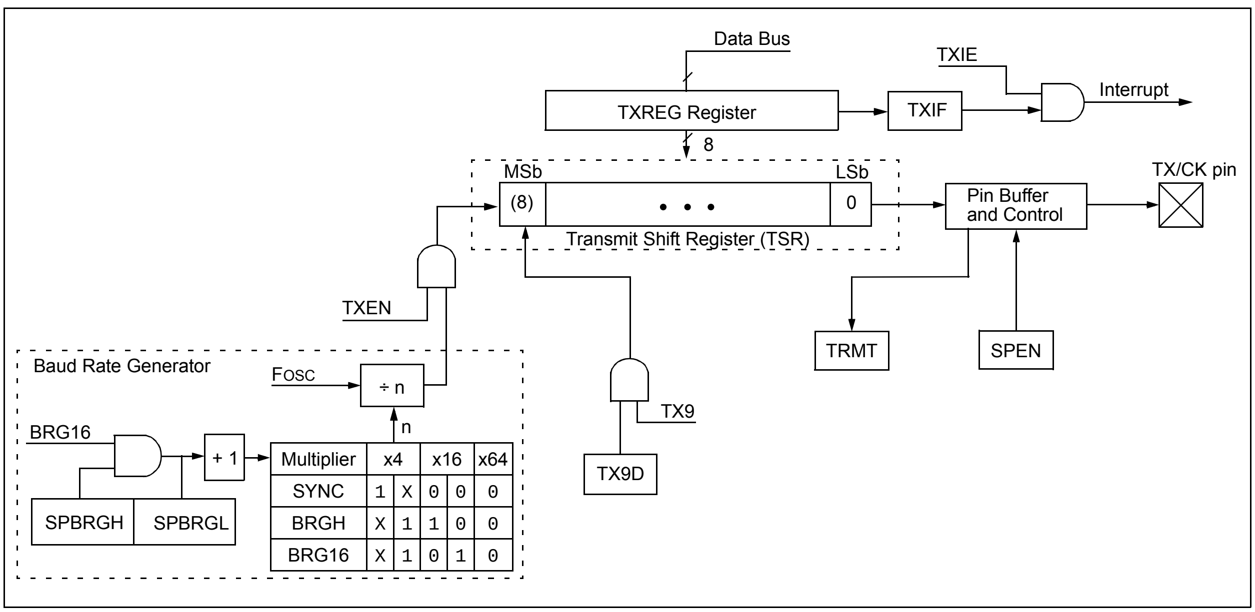
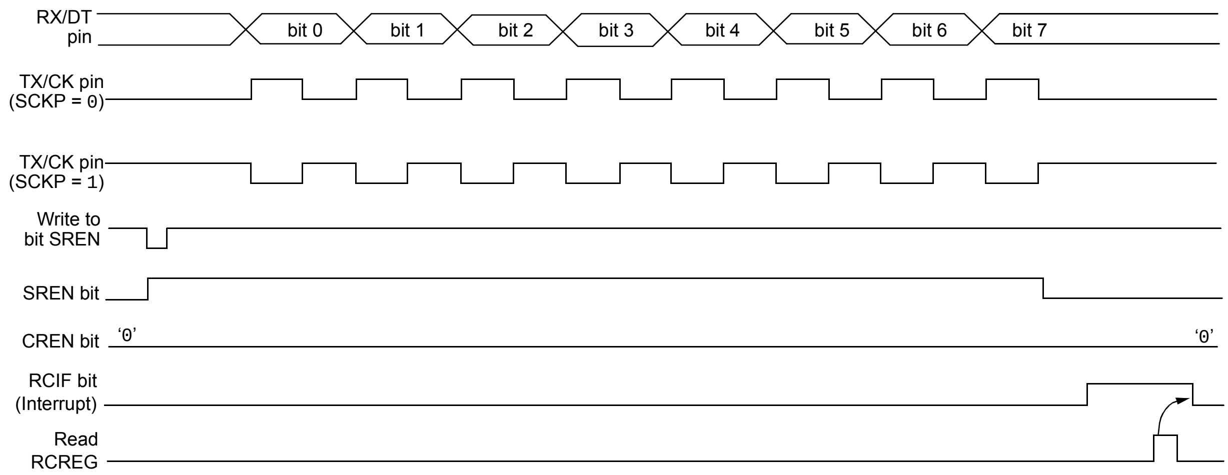


FIGURE 22-12: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0.

TABLE 22-7: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	249
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	69
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	70
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	72
RCREG	EUSART Receive Data Register								242*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	248
SPBRGL	BRG<7:0>								250*
SPBRGH	BRG<15:8>								250*
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	110
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	247

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous master reception.
* Page provides register information.

SWAPF — Swap Nibbles in f

Syntax:	[*label*] SWAPF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f<3:0>) → (destination<7:4>), (f<7:4>) → (destination<3:0>)
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

TRIS — Load TRIS Register with W

Syntax:	[*label*] TRIS f
Operands:	$5 \leq f \leq 7$
Operation:	(W) → TRIS register 'f'
Status Affected:	None
Description:	Move data from W register to TRIS register. When 'f' = 5, TRISA is loaded. When 'f' = 6, TRISB is loaded. When 'f' = 7, TRISC is loaded.

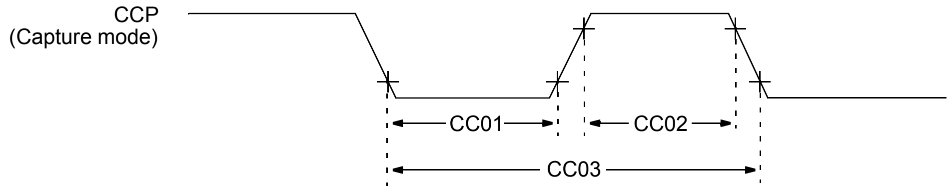
XORLW — Exclusive OR literal with W

Syntax:	[*label*] XORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .XOR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

XORWF — Exclusive OR W with f

Syntax:	[*label*] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) → (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

FIGURE 25-11: CAPTURE/COMPARE/PWM TIMINGS (CCP)



Note: Refer to Figure 25-4 for load conditions.

TABLE 25-11: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

Standard Operating Conditions (unless otherwise stated)								
Param No.	**Sym.**	**Characteristic**		**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
CC01*	TccL	CCP Input Low Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCP Input High Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCP Input Period		$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 25-12: ANALOG-TO-DIGITAL CONVERTER (ADC) CHARACTERISTICS(1,2,3)

Standard Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = 25°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	10	bit	
AD02	EIL	Integral Error	—	—	±1.25	LSb	VREF = 3.0V
AD03	EDL	Differential Error	—	—	±1	LSb	No missing codes VREF = 3.0V
AD04	EOFF	Offset Error	—	—	±2.5	LSb	VREF = 3.0V
AD05	EGN	Gain Error	—	—	±2.0	LSb	VREF = 3.0V
AD06	VREF	Reference Voltage(4)	1.8	—	VDD	V	
AD07	VAIN	Full-Scale Range	VSS	—	VREF	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: ADC VREF is from external VREF, VDD pin or FVR, whichever is selected as reference input.

4: FVR voltage selected must be 2.048V or 4.096V.

FIGURE 26-33: IPD, WATCHDOG TIMER (WDT), PIC16LF1512/3 ONLY

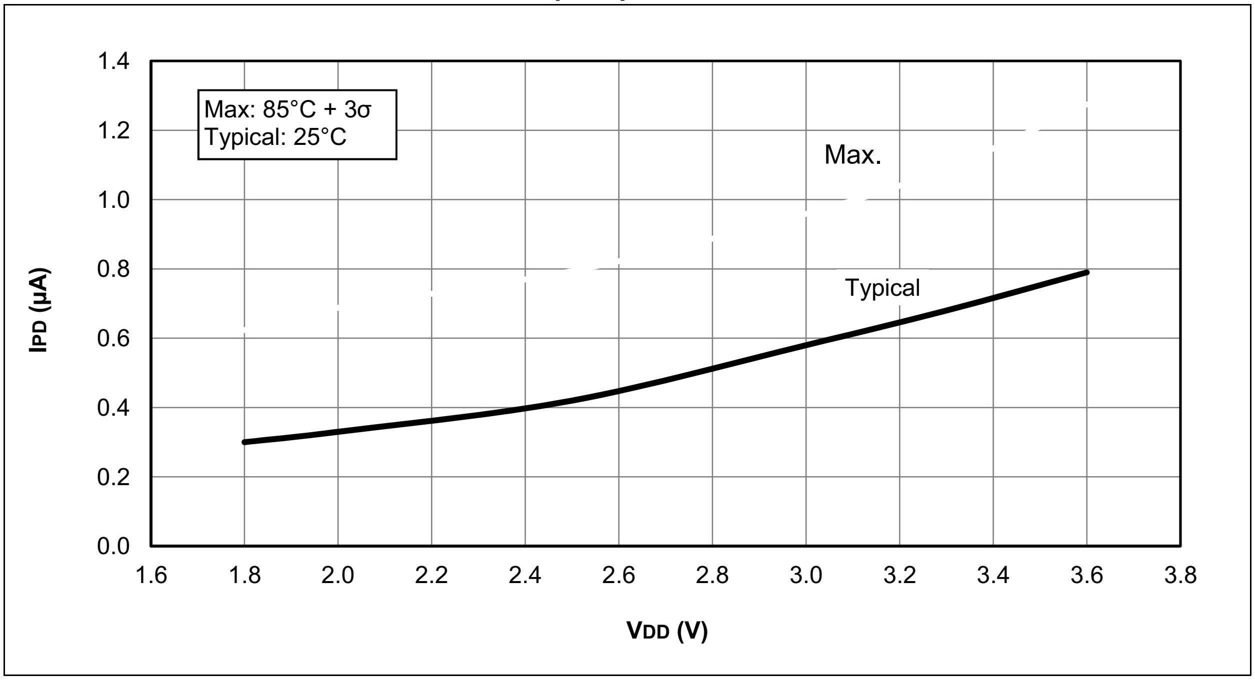


FIGURE 26-34: IPD, WATCHDOG TIMER (WDT), PIC16F1512/3 ONLY

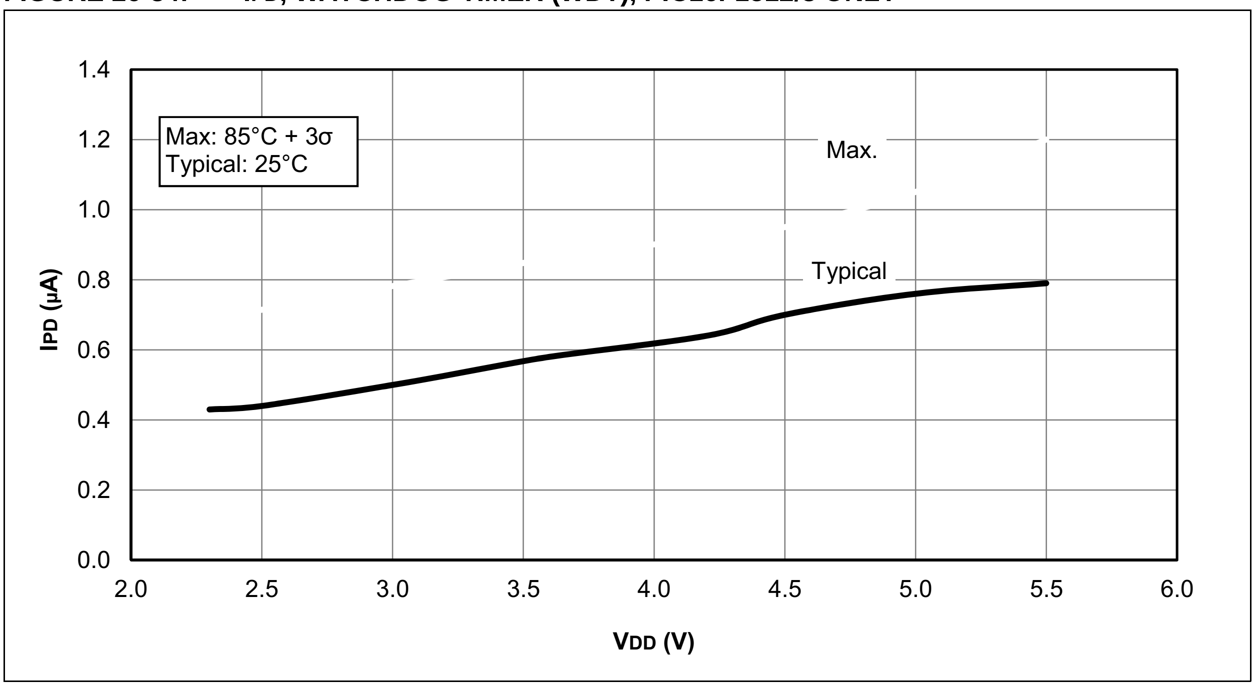


FIGURE 26-56: LFINTOSC FREQUENCY OVER VDD AND TEMPERATURE, PIC16LF1512/3 ONLY

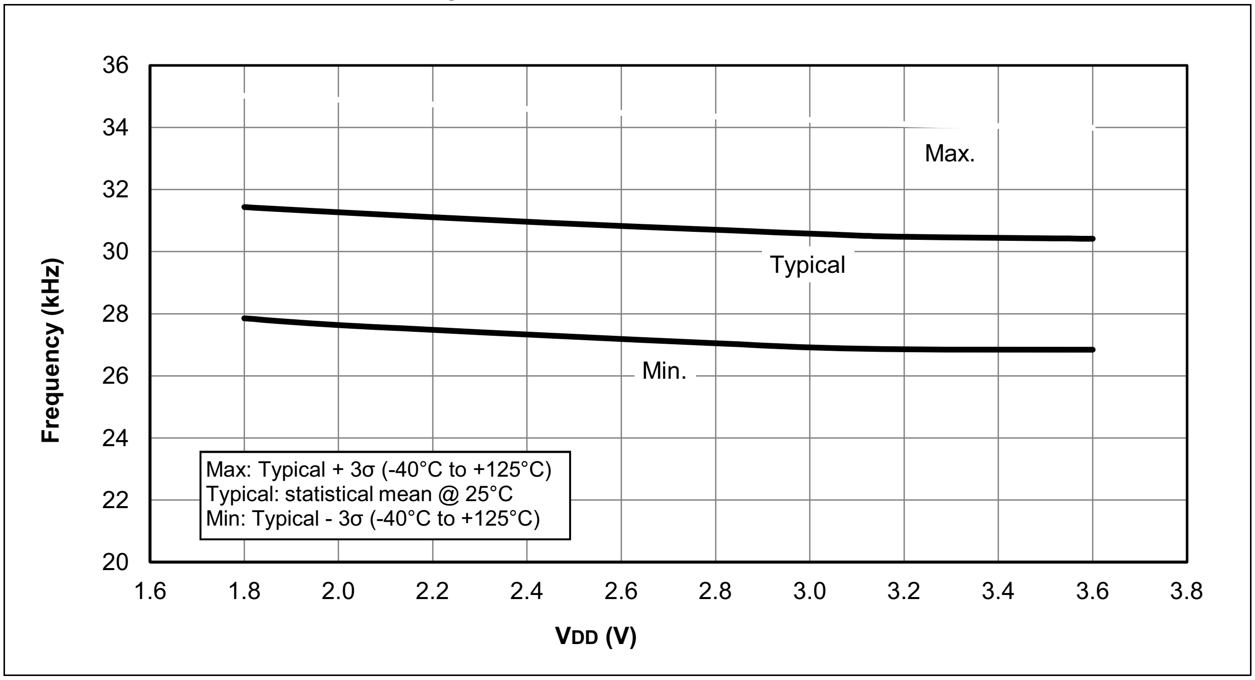


FIGURE 26-57: LFINTOSC FREQUENCY OVER VDD AND TEMPERATURE, PIC16F1512/3 ONLY