Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	UHF ASK/FSK
Core Processor	MARC4
Program Memory Type	FLASH (4kB)
Controller Series	MARC4 4-Bit
RAM Size	256 x 4
Interface	SSI
Number of I/O	11
Voltage - Supply	1.8V ~ 4V
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	24-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	24-SSO
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atam862p-tnqy8d

6. General Description

The fully-integrated PLL transmitter that allows particularly simple, low-cost RF miniature transmitters to be assembled. The VCO is locked to 64 × f_{XTAL}, thus, a 13.5672 MHz crystal is needed for a 868.3 MHz transmitter and a 14.2969 MHz crystal for a 915 MHz transmitter. All other PLL and VCO peripheral elements are integrated.

The XTO is a series resonance oscillator so that only one capacitor together with a crystal connected in series to GND are needed as external elements.

The crystal oscillator together with the PLL needs typically < 1 ms until the PLL is locked and the CLK output is stable. A wait time of ≥ 4 ms must be used until the CLK is used for the microcontroller and the PA is switched on.

The power amplifier is an open-collector output delivering a current pulse which is nearly independent from the load impedance. The delivered output power is controlled via the connected load impedance.

This output configuration enables a simple matching to any kind of antenna or to 50 Ω. A high power efficiency of $\eta = P_{out}/(I_{S,PA} \times V_S)$ of 24% for the power amplifier at 868.3 MHz results when an optimized load impedance of Z_{Load} = (166 + j226) Ω is used at 3 V supply voltage.

7. Functional Description

If ENABLE = L and PA_ENABLE = L, the circuit is in standby mode consuming only a very small amount of current, so that a lithium cell used as power supply can work for several years.

With ENABLE = H, the XTO, PLL and the CLK driver are switched on. If PA_ENABLE remains L, only the PLL and the XTO are running and the CLK signal is delivered to the microcontroller. The VCO locks to 64 times the XTO frequency.

With ENABLE = H and PA_ENABLE = H, the PLL, XTO, CLK driver and the power amplifier are on. With PA_ENABLE, the power amplifier can be switched on and off, which is used to perform the ASK modulation.

7.1 ASK Transmission

The PLL transmitter block is activated by ENABLE = H. PA_ENABLE must remain L for t ≥ 4 ms, then the CLK signal can be taken to clock the microcontroller and the output power can be modulated by means of pin PA_ENABLE. After transmission, PA_ENABLE is switched to L and the microcontroller switches back to internal clocking. The ATAM862-8 is switched back to standby mode with ENABLE = L.

7.2 FSK Transmission

The PLL transmitter block is activated by ENABLE = H. PA_ENABLE must remain L for t ≥ 4 ms, then the CLK signal can be taken to clock the microcontroller and the power amplifier is switched on with PA_ENABLE = H. The chip is then ready for FSK modulation. The microcontroller starts to switch on and off the capacitor between the XTAL load capacitor and GND with an open-drain output port, thus changing the reference frequency of the PLL. If the switch is closed, the output frequency is lower than if the switch is open. After transmission PA_ENABLE is switched to L and the microcontroller switches back to internal clocking. The PLL transmitter block is switched back to standby mode with ENABLE = L.

The accuracy of the frequency deviation with XTAL pulling method is about ±25% when the following tolerances are considered.

Figure 7-3. ASK Application Circuit

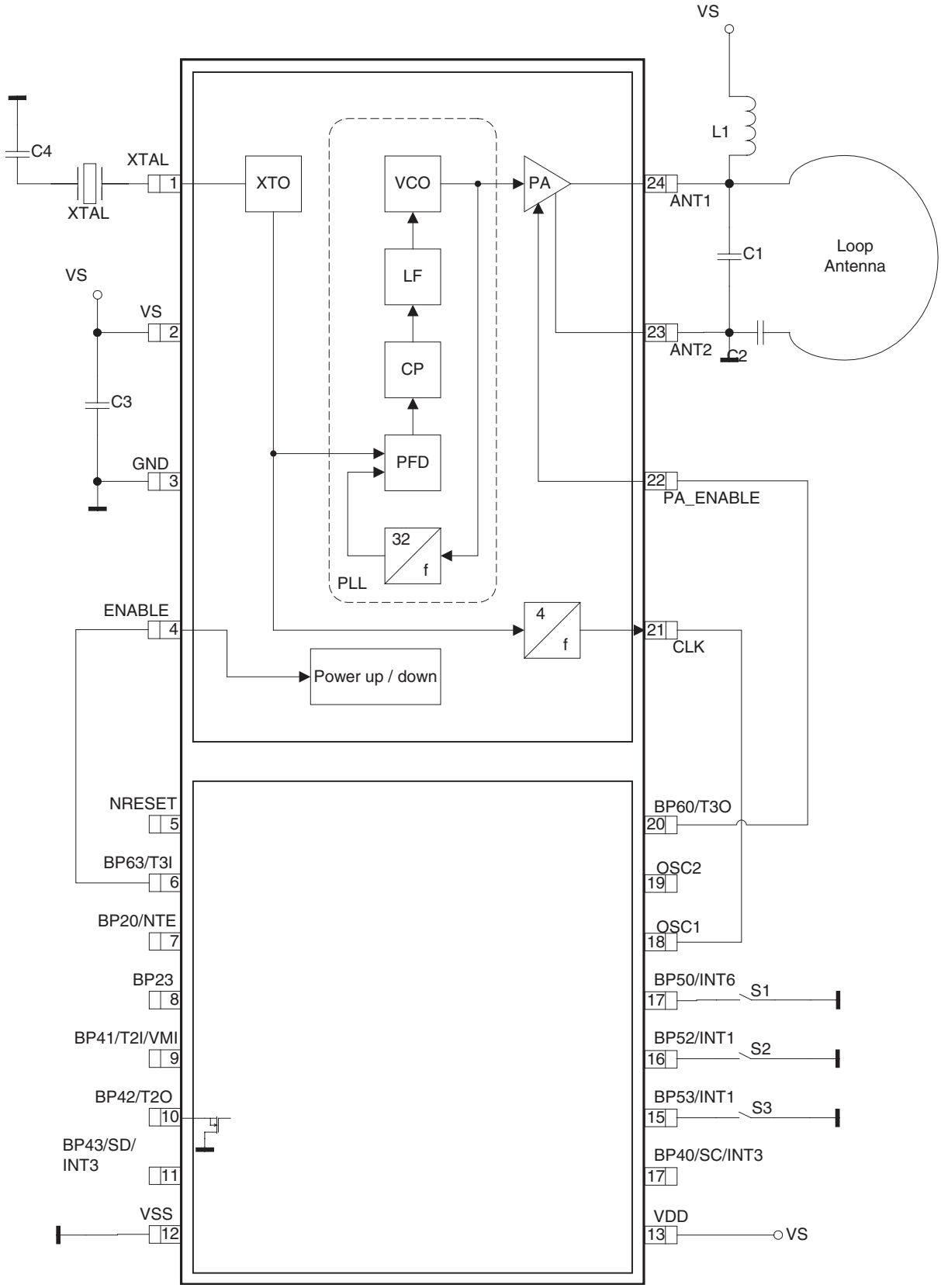
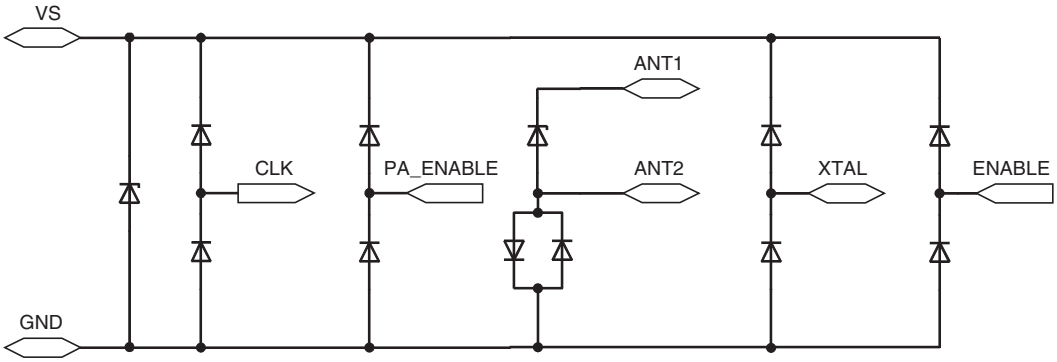


Figure 7-5. ESD Protection Circuit



8. Absolute Maximum Ratings: RF Part

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_S		5	V
Power dissipation	P_{tot}		100	mW
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	-55	+125	°C
Ambient temperature	T_{amb}	-55	+125	°C
Input voltage	V_{maxPA_ENABLE}	-0.3	$(V_S + 0.3)^{(1)}$	V

Note: 1. If V_S + 0.3 is higher than 3.7 V, the maximum voltage will be reduced to 3.7 V.

9. Thermal Resistance

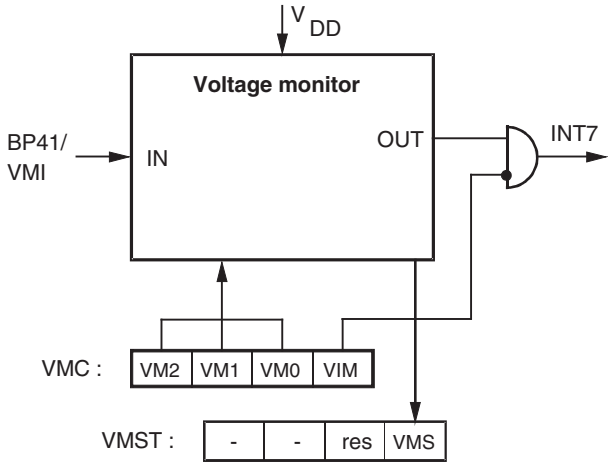
Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	135	K/W

10. Electrical Characteristics

V_S = 2.0 V to 4.0 V, T_{amb} = -40°C to +125°C unless otherwise specified.
Typical values are given at V_S = 3.0 V and T_{amb} = 25°C. All parameters are refered to GND (Pin 3).

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply current	Power down, V_{ENABLE} < 0.25 V, -40°C to 85°C V_{PA_ENABLE} < 0.25 V, -85°C to +125° C V_{PA_ENABLE} < 0.25 V, 25°C (100% correlation tested)	I_{S_Off}		 <10	350 7 	nA µA nA
Supply current	Power up, PA off, V_S = 3 V V_{ENABLE} > 1.7 V, V_{PA_ENABLE} < 0.25 V	I_S		3.6	4.6	mA
	Power up, V_S = 3.0 V V_{ENABLE} > 1.7 V, V_{PA_ENABLE} > 1.7 V	$I_{S\_Transmit}$		8.5	11	mA
Output power	V_S = 3.0 V, T_{amb} = 25° C f = 868.3 MHz, Z_{Load} = (166 + j226) Ω	P_{Ref}	3.5	5.5	8	dBm

Figure 18-1. Voltage Monitor



18.0.1 Voltage Monitor Control/Status Register

Primary register address: "F"hex

	Bit 3	Bit 2	Bit 1	Bit 0	
VMC: Write	**VM2**	**VM1**	**VM0**	**VIM**	**Reset value: 1111b**
VMST: Read	**–**	**–**	**Reserved**	**VMS**	**Reset value: xx11b**

VM2: **V**oltage monitor **M**ode bit **2**
VM1: **V**oltage monitor **M**ode bit **1**
VM0: **V**oltage monitor **M**ode bit **0**

Table 18-1. Voltage Monitor Modes

VM2	VM1	VM0	Function
1	1	1	Disable voltage monitor
1	1	0	External (VIM input), internal reference threshold (1.3 V), interrupt with negative slope
1	0	1	Not allowed
1	0	0	External (VMI input), internal reference threshold (1.3 V), interrupt with positive slope
0	1	1	Internal (supply voltage), high threshold (3.0 V), interrupt with negative slope
0	1	0	Internal (supply voltage), middle threshold (2.6 V), interrupt with negative slope
0	0	1	Internal (supply voltage), low threshold (2.2 V), interrupt with negative slope
0	0	0	Not allowed

VIM **V**oltage **I**nterrupt **M**ask bit
VIM = 0, voltage monitor interrupt is enabled
VIM = 1, voltage monitor interrupt is disabled

VMS **V**oltage **M**onitor **S**tatus bit
VMS = 0, the voltage at the comparator input is below V_{Ref}
VMS = 1, the voltage at the comparator input is above V_{Ref}

Figure 18-2. Internal Supply Voltage Supervisor

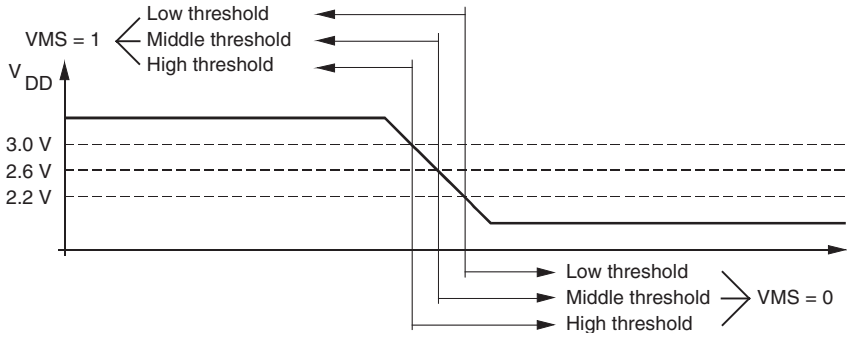
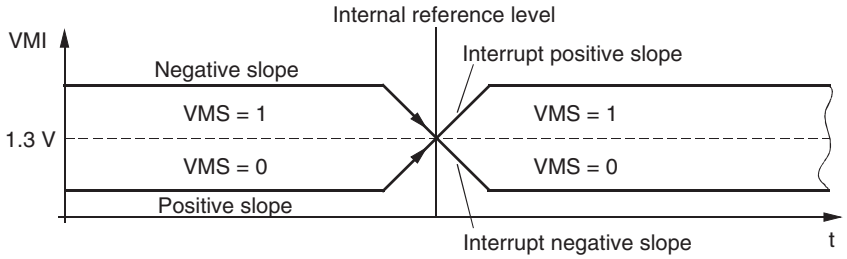


Figure 18-3. External Input Voltage Supervisor



19. Clock Generation

19.1 Clock Module

The ATAM862-8 contains a clock module with 4 different internal oscillator types: two RC-oscillators, one 4-MHz crystal oscillator and one 32-kHz crystal oscillator. The pins OSC1 and OSC2 are the interface to connect a crystal either to the 4-MHz, or to the 32-kHz crystal oscillator. OSC1 can be used as input for external clocks or to connect an external trimming resistor for the RC-oscillator 2. All necessary circuitry, except the crystal and the trimming resistor, is integrated on-chip. One of these oscillator types or an external input clock can be selected to generate the system clock (SYSCL).

In applications that do not require exact timing, it is possible to use the fully integrated RC-oscillator 1 without any external components. The RC-oscillator 1 center frequency tolerance is better than ±50%. The RC-oscillator 2 is a trimmable oscillator whereby the oscillator frequency can be trimmed with an external resistor attached between OSC1 and V_{DD}. In this configuration, the RC-oscillator 2 frequency can be maintained stable with a tolerance of ±15% over the full operating temperature and voltage range.

The clock module is programmable via software with the clock management register (CM) and the system configuration register (SC). The required oscillator configuration can be selected with the OS1 bit and the OS0 bit in the SC register. A programmable 4-bit divider stage allows the adjustment of the system clock speed. A special feature of the clock management is that an external oscillator may be used and switched on and off via a port pin for the power-down mode. Before the external clock is switched off, the internal RC-oscillator 1 must be selected with the CCS bit and then the SLEEP mode may be activated. In this state an interrupt can wake up the controller with the RC-oscillator, and the external oscillator can be activated and selected by

Table 21-1. Peripheral Addresses

Port Address			Name	Write/ Read	Reset Value	Register Function	Module Type
1			P1DAT	W/R	1xx1b	Port 1 - data register/input data	M3
2			P2DAT	W/R	1111b	Port 2 - data register/pin data	M2
	Auxiliary		P2CR	W	1111b	Port 2 - control register	
3			SC	W	1x11b	System configuration register	M3
			CWD	R	xxxxb	Watchdog reset	M3
	Auxiliary		CM	W	1111b	Clock management register	M2
4			P4DAT	W/R	1111b	Port 4 - data register/pin data	M2
	Auxiliary		P4CR	W	1111 1111b	Port 4 - control register (byte)	
5			P5DAT	W/R	1111b	Port 5 - data register/pin data	M2
	Auxiliary		P5CR	W	1111 1111b	Port 5 - control register (byte)	
6			P6DAT	W/R	1xx1b	Port 6 - data register/pin data	M2
	Auxiliary		P6CR	W	1111b	Port 6 - control register (byte)	
7			T12SUB	W	–	Data to Timer 1/2 subport	M1
		Subport address					
		0	T2C	W	0000b	Timer 2 control register	M1
		1	T2M1	W	1111b	Timer 2 mode register 1	M1
		2	T2M2	W	1111b	Timer 2 mode register 2	M1
		3	T2CM	W	0000b	Timer 2 compare mode register	M1
		4	T2CO1	W	1111b	Timer 2 compare register 1	M1
		5	T2CO2	W	1111 1111b	Timer 2 compare register 2 (byte)	M1
		6	–	–	–	Reserved	
		7	–	–	–	Reserved	
		8	T1C1	W	1111b	Timer 1 control register 1	M1
		9	T1C2	W	x111b	Timer 1 control register 2	M1
		A	WDC	W	1111b	Watchdog control register	M1
		B-F				Reserved	
8			ASW	W	1111b	Auxiliary/switch register	ASW
9			STB	W	xxxx xxxxb	Serial transmit buffer (byte)	M2
			SRB	R	xxxx xxxxb	Serial receive buffer (byte)	
	Auxiliary		SIC1	W	1111b	Serial interface control register 1	
A			SISC	W/R	1x11b	Serial interface status/control register	M2
	Auxiliary		SIC2	W	1111b	Serial interface control register 2	
B			T3SUB	W/R	–	Data to/from Timer 3 subport	M1
		Subport address					
		0	T3M	W	1111b	Timer 3 mode register	M1
		1	T3CS	W	1111b	Timer 3 clock select register	M1
		2	T3CM1	W	0000b	Timer 3 compare mode register 1	M1
		3	T3CM2	W	0000b	Timer 3 compare mode register 2	M1
		4	T3CO1	W	1111 1111b	Timer 3 compare register 1 (byte)	M1
		4	T3CP	R	xxxx xxxxb	Timer 3 capture register (byte)	M1
		5	T3CO2	W	1111 1111b	Timer 3 compare register 2 (byte)	M1
		6		W	1111b	Reserved	
		7-F			–	Reserved	
C		T3C		W	0000b	Timer 3 control register	M3
		T3ST		R	x000b	Timer 3 status register	M3
D, E		–			–	Reserved	
F		VMC		W	1111b	Voltage monitor control register	M3
		VMST		R	xx11b	Voltage monitor status register	M3

22. Bi-directional Ports

With the exception of Port 1 and Port 6, all other ports (2, 4 and 5) are 4 bits wide. Port 1 and Port 6 have a data width of 2 bits (bit 0 and bit 3). All ports may be used for data input or output. All ports are equipped with Schmitt trigger inputs and a variety of mask options for open-drain, open-source, full-complementary outputs, pull-up and pull-down transistors. All Port Data Registers (PxDAT) are I/O mapped to the primary address register of the respective port address and the Port Control Register (PxCR), to the corresponding auxiliary register.

There are five different directional ports available:

Port 1 — 2-bit wide bi-directional port with automatic full bus width direction switching.

Port 2 — 4-bit wide bitwise-programmable I/O port.

Port 5 — 4-bit wide bitwise-programmable bi-directional port with optional strong pull-ups and programmable interrupt logic.

Port 4 — 4-bit wide bitwise-programmable bi-directional port also provides the I/O interface to Timer 2, SSI, voltage monitor input and external interrupt input.

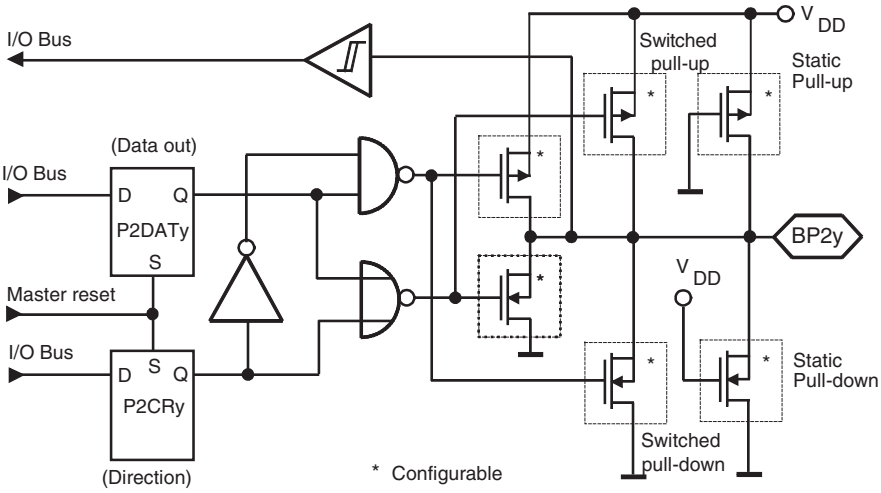
Port 6 — 2-bit wide bitwise-programmable bi-directional port also provides the I/O interface to Timer 3 and external interrupt input.

22.1 Bi-directional Port 1

In Port 1 the data direction register is not independently software programmable, the direction of the complete port being switched automatically when an I/O instruction occurs (see Figure 22-1 on page 36). The port is switched to output mode via an OUT instruction and to input via an IN instruction. The data written to a port will be stored into the output data latches and appears immediately at the port pin following the OUT instruction. After RESET all output latches are set to "1" and the port is switched to input mode. An IN instruction reads the condition of the associated pins.

Note: Care must be taken when switching the bi-directional port from output to input. The capacitive pin loading at this port in conjunction with the high resistance pull-ups may cause the CPU to read the contents of the output data register rather than the external input state. To avoid this, one of the following programming techniques should be used:
Use two IN-instructions and DROP the first data nibble. The first IN switches the port from output to input and the DROP removes the first invalid nibble. The second IN reads the valid pin state.
Use an OUT instruction followed by an IN instruction. Via the OUT instruction, the capacitive load is charged or discharged depending on the optional pull-up/pull-down configuration. Write a "1" for pins with pull-up resistors and a "0" for pins with pull-down resistors.

Figure 22-2. Bi-directional Port 2



22.2.1 Port 2 Data Register (P2DAT)

Primary register address: "2"hex

Bit 3 *	Bit 2	Bit 1	Bit 0
P2DAT3	P2DAT2	P2DAT1	P2DAT0

Reset value: 1111b

* Bit 3 -> MSB, Bit 0 -> LSB

22.2.2 Port 2 Control Register (P2CR)

Auxiliary register address: "2"hex

Bit 3	Bit 2	Bit 1	Bit 0
P2CR3	P2CR2	P2CR1	P2CR0

Reset value: 1111b

Value: 1111b means all pins in input mode

Table 22-1. Port 2 Control Register

Code 3 2 1 0	Function
x x x 1	BP20 in input mode
x x x 0	BP20 in output mode
x x 1 x	BP21 in input mode
x x 0 x	BP21 in output mode
x 1 x x	BP22 in input mode
x 0 x x	BP22 in output mode
1 x x x	BP23 in input mode
0 x x x	BP23 in output mode

22.12.6 Timer 2 Compare Mode Register (T2CM)

Address: "7"hex - Subaddress: "3"hex

Bit 3	Bit 2	Bit 1	Bit 0
T2OTM	**T2CTM**	**T2RM**	**T2IM**

Reset value: 0000b

T2OTM — **T**imer **2** **O**verflow **T**oggle **M**ask bit
T2OTM = 0, disable overflow toggle
T2OTM = 1, enable overflow toggle, a counter overflow (OVF2) toggles output flip-flop (TOG2). If the T2OTM bit is set, only a counter overflow can generate an interrupt except on the Timer 2 output mode 7.

T2CTM — **T**imer **2** **C**ompare **T**oggle **M**ask bit
T2CTM = 0, disable compare toggle
T2CTM = 1, enable compare toggle, a match of the counter with the compare register toggles output flip-flop (TOG2). In Timer 2 output mode 7 and when the T2CTM bit is set, only a match of the counter with the compare register can generate an interrupt.

T2RM — **T**imer **2** **R**eset **M**ask bit
T2RM = 0, disable counter reset
T2RM = 1, enable counter reset, a match of the counter with the compare register resets the counter

T2IM — **T**imer **2** **I**nterrupt **M**ask bit
T2IM = 0, disable Timer 2 interrupt
T2IM = 1, enable Timer 2 interrupt

Table 22-11. Timer 2 Toggle Mask Bits

Timer 2 Output Mode	T2OTM	T2CTM	Timer 2 Interrupt Source
1, 2, 3, 4, 5 and 6	0	x	Compare match (CM2)
1, 2, 3, 4, 5 and 6	1	x	Overflow (OVF2)
7	x	1	Compare match (CM2)

22.12.7 Timer 2 COmpare Register 1 (T2CO1)

Address: "7"hex - Subaddress: "4"hex

Write cycle	Bit 3	Bit 2	Bit 1	Bit 0

Reset value: 1111b

In prescaler mode the clock is bypassed if the compare register T2CO1 contains 0.

22.12.8 Timer 2 COmpare Register 2 (T2CO2) Byte Write

Address: "7"hex - Subaddress: "5"hex

First write cycle	Bit 3	Bit 2	Bit 1	Bit 0

Reset value: 1111b

Second write cycle	Bit 7	Bit 6	Bit 5	Bit 4

Reset value: 1111b

23.6 Timer 3 Registers

23.6.1 Timer 3 Mode Register (T3M)

Address: "B"hex - Subaddress: "0"hex

Bit 3	Bit 2	Bit 1	Bit 0
T3M3	**T3M2**	**T3M1**	**T3M0**

Reset value: 1111b

T3M3 **T**imer **3** **M**ode select bit **3**
T3M2 **T**imer **3** **M**ode select bit **2**
T3M1 **T**imer **3** **M**ode select bit **1**
T3M0 **T**imer **3** **M**ode select bit **0**

Table 23-1. Timer 3 Mode Select Bits

Mode	T3M3	T3M2	T3M1	T3M0	Timer 3 Modes
1	1	1	1	1	Timer/counter with a read access
2	1	1	1	0	Timer/counter, external capture and external trigger restart mode (T3I)
3	1	1	0	1	Timer/counter, internal capture and internal trigger restart mode (TOG2)
4	1	1	0	0	Timer/counter mode 1 without output (T2O -> T3O)
5	1	0	1	1	Timer/counter mode 2 without output (T2O -> T3O)
6	1	0	1	0	Burst modulation with Timer 2 (M2)
7	1	0	0	1	Burst modulation with shift register (SO)
8	1	0	0	0	FSK modulation with shift register (SO)
9	0	1	1	1	Pulse-width modulation with shift register (SO) and Timer 2 (TOG2), internal trigger restart (SCO) -> counter reset
10	0	1	1	0	Manchester demodulation/pulse-width demodulation (1) (T2O -> T3O)
11	0	1	0	1	Biphase demodulation (T2O -> T3O)
12	0	1	0	0	Timer/counter with external capture mode (T3I)
13	0	0	1	1	Not allowed
14	0	0	1	0	Not allowed
15	0	0	0	1	Not allowed
16	0	0	0	0	Not allowed

Note: 1. In this mode, the SSI can be used only as demodulator (8-bit NRZ rising edge). All other SSI modes are not allowed.

23.6.6 Timer 3 Compare-Mode Register 1 (T3CM1)

Address: "B"hex - Subaddress: "2"hex

	Bit 3	Bit 2	Bit 1	Bit 0	
T3CM1	**T3SM1**	**T3TM1**	**T3RM1**	**T3IM1**	**Reset value: 0000b**

T3SM1 — **T**imer **3** **S**ingle action **M**ask bit **1**
T3SM1 = 0, disables single-action compare mode
T3SM1 = 1, enables single-compare mode. After this bit is set, the compare register (T3CO1) is used until the next compare match.

T3TM1 — **T**imer **3** compare **T**oggle action **M**ask bit **1**
T3TM1 = 0, disables compare toggle
T3TM1 = 1, enables compare toggle. A match of Counter 3 with the compare register (T3CO1) toggles the output flip-flop (TOG3).

T3RM1 — **T**imer **3** **R**eset **M**ask bit **1**
T3RM1 = 0, disables counter reset
T3RM1 = 1, enables counter reset. A match of Counter 3 with the compare register (T3CO1) resets the Counter 3.

T3IM1 — **T**imer **3** **I**nterrupt **M**ask bit **1**
T3RM1 = 0, disables Timer 3 interrupt for T3CO1 register.
T3RM1 = 1, enables Timer 3 interrupt for T3CO1 register.

T3CM1 contains the mask bits for the match event of the Counter 3 compare register 1.

23.6.7 Timer 3 Compare Mode Register 2 (T3CM2)

Address: "B"hex - Subaddress: "3"hex

	Bit 3	Bit 2	Bit 1	Bit 0	
T3CM2	**T3SM2**	**T3TM2**	**T3RM2**	**T3IM2**	**Reset value: 0000b**

T3SM2 — **T**imer **3** **S**ingle action **M**ask bit **2**
T3SM2 = 0, disables single-action compare mode
T3SM2 = 1, enables single-compare mode. After this bit is set, the compare register (T3CO2) is used until the next compare match.

T3TM2 — **T**imer **3** compare **T**oggle action **M**ask bit **2**
T3TM2 = 0, disables compare toggle
T3TM2 = 1, enables compare toggle. A match of Counter 3 with the compare register (T3CO2) toggles the output flip-flop (TOG3).

T3RM2 — **T**imer **3** **R**eset **M**ask bit **2**
T3RM2 = 0, disables counter reset
T3RM2 = 1, enables counter reset. A match of Counter 3 with the compare register (T3CO2) resets the Counter 3.

T3IM2 — **T**imer **3** **I**nterrupt **M**ask bit **2**
T3RM2 = 0, disables Timer 3 interrupt for T3CO2 register.
T3RM2 = 1, enables Timer 3 interrupt for T3CO2 register.

T3CM2 contains the mask bits for the match event of Counter 3 compare register 2

23.8.5 9-bit Shift Mode (MCL compatible)

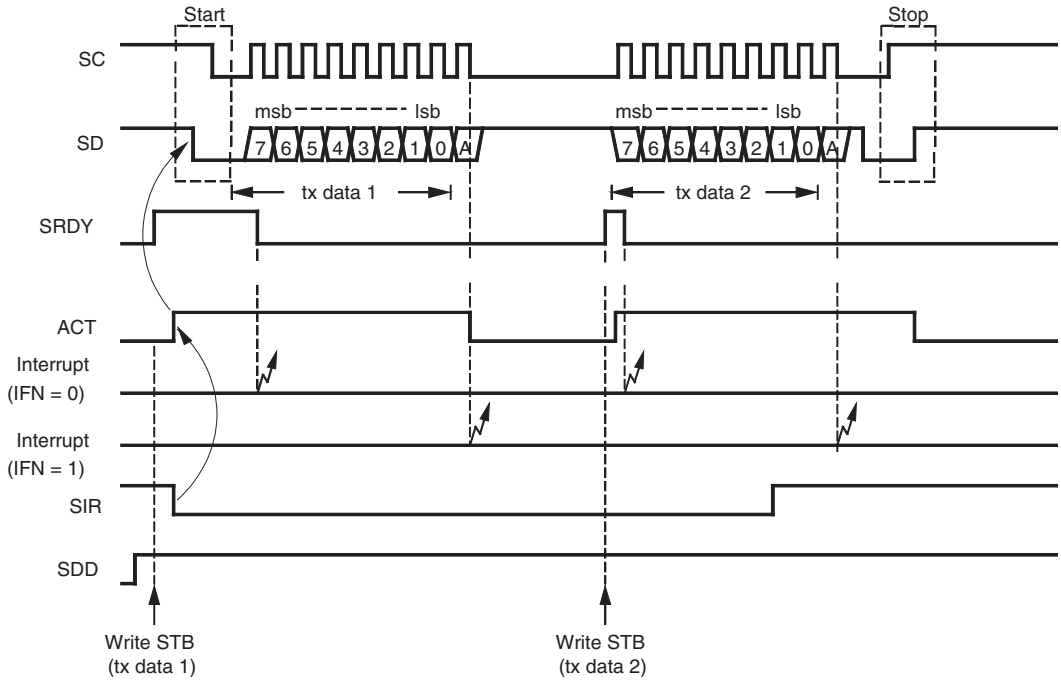
In the 9-bit shift mode, the SSI is able to handle the MCL protocol (described below). It always operates as an MCL master device, i.e., SC is always generated and output by the SSI. Both the MCL start and stop conditions are automatically generated whenever the SSI is activated or deactivated by the SIR bit. In accordance with the MCL protocol, the output data is always changed in the clock low phase and shifted in on the high phase.

Before activating the SSI (SIR = 0) and commencing an MCL dialog, the appropriate data direction for the first word must be set using the SDD control bit. The state of this bit controls the direction of the data port (BP43 or MCL_SD). Once started, the 8 data bits are, depending on the selected direction, either clocked into or out of the shift register. During the 9th clock period, the port direction is automatically switched over so that the corresponding acknowledge bit can be shifted out or read in. In transmit mode, the acknowledge bit received from the device is captured in the SSI Status Register (TACK) where it can be read by the controller. In receive mode, the state of the acknowledge bit to be returned to the device is predetermined by the SSI Status Register (RACK).

Changing the directional mode (TX/RX) should not be performed during the transfer of an MCL telegram. One should wait until the end of the telegram which can be detected using the SSI interrupt (IFN =1) or by interrogating the ACT status.

Once started, a 9-bit telegram will always run to completion and will not be prematurely terminated by the SIR bit. So, if the SIR bit is set to ‘1’ in telegram, the SSI will complete the current transfer and terminate the dialog with an MCL stop condition.

Figure 23-19. Example of MCL Transmit Dialog



23.9 Serial Interface Registers

23.9.1 Serial Interface Control Register 1 (SIC1)

Auxiliary register address: "9"hex

Bit 3	Bit 2	Bit 1	Bit 0
SIR	**SCD**	**SCS1**	**SCS0**

Reset value: 1111b

SIR — **S**erial **I**nterface **R**eset
SIR = 1, SSI inactive
SIR = 0, SSI active

SCD — **S**erial **C**lock **D**irection
SCD = 1, SC line used as output
SCD = 0, SC line used as input

Note: This bit has to be set to "1" during the MCL mode and the Timer 3 mode 10 or 11

SCS1 — **S**erial **C**lock source **S**elect bit **1**

SCS0 — **S**erial **C**lock source **S**elect bit **0**

Note: With SCD = 0 the bits SCS1 and SCS0 are insignificant

Table 23-4. Serial Clock Source Select Bits

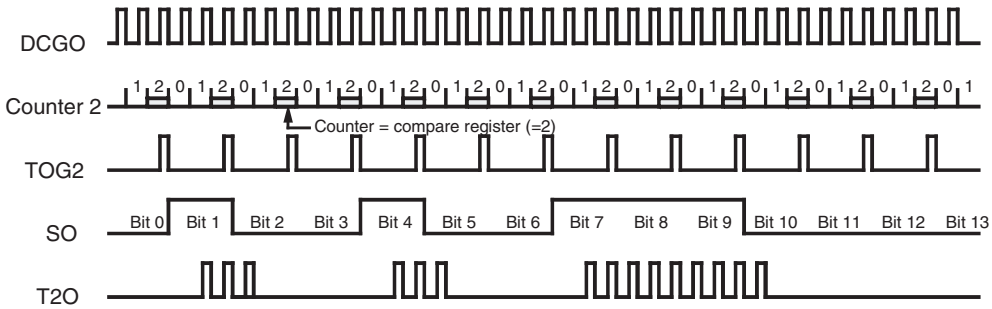
SCS1	SCS0	Internal Clock for SSI
1	1	SYSCL/2
1	0	T1OUT/2
0	1	POUT/2
0	0	TOG2/2

- In transmit mode (SDD = 1) shifting starts only if the transmit buffer has been loaded (SRDY = 1).
- Setting SIR-bit loads the contents of the shift register into the receive buffer (synchronous 8-bit mode only).
- In MCL modes, writing a 0 to SIR generates a start condition and writing a 1 generates a stop condition.

24.1.1 Combination Mode 1: Burst Modulation

SSI mode 1:	8-bit NRZ and internal data SO output to the Timer 2 modulator stage
Timer 2 mode 1, 2, 3 or 4:	8-bit compare counter with 4-bit programmable prescaler and DCG
Timer 2 output mode 3:	Duty cycle burst generator

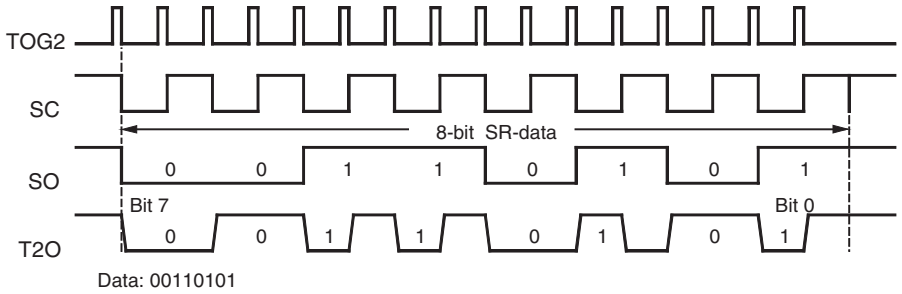
Figure 24-2. Carrier Frequency Burst Modulation with the SSI Internal Data Output



24.1.2 Combination Mode 2: Biphase Modulation 1

SSI mode 1:	8-bit shift register internal data output (SO) to the Timer 2 modulator stage
Timer 2 mode 1, 2, 3 or 4:	8-bit compare counter with 4-bit programmable prescaler
Timer 2 output mode 4:	The modulator 2 of Timer 2 modulates the SSI internal data output to Biphase code

Figure 24-3. Biphase Modulation 1



24.2.4 Combination Mode 9: Biphase Demodulation

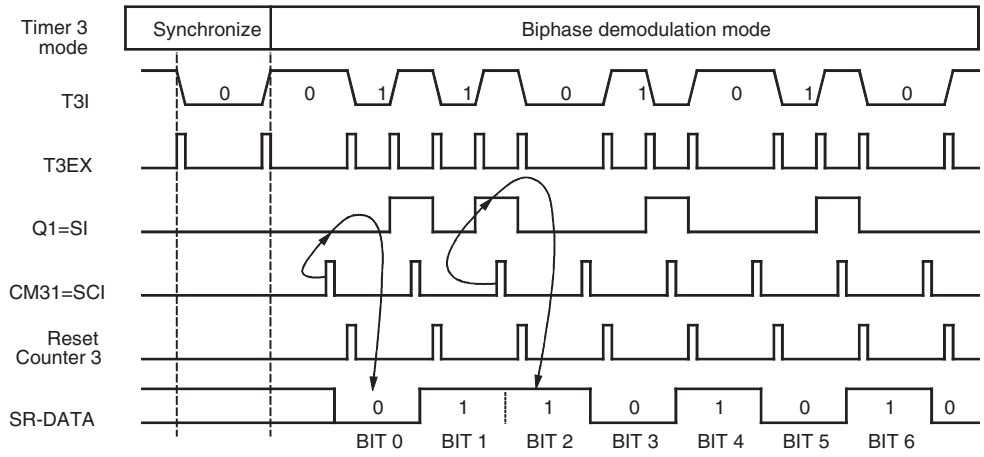
SSI mode 1: 8-bit shift register internal data input (SI) and the internal shift clock (SCI) from the Timer 3

Timer 3 mode 11: Biphase demodulation with Timer 3

In the Biphase demodulation mode the timer works like in the Manchester demodulation mode. The difference is that the bits are decoded with the toggle flip-flop. This flip-flop samples the edge in the middle of the bitframe and the compare register 1 match event shifts the toggle flip-flop output into shift register. Before activating the demodulation the timer and the demodulation stage must be synchronized with the bitstream. The Biphase code timing consists of parts with the half bitlength and the complete bitlength. The synchronization routine must start the demodulator after an interval with the complete bitlength.

The counter can be driven by any internal clock source and the output T3O can be used by Timer 2 in this mode.

Figure 24-11. Biphase Demodulation

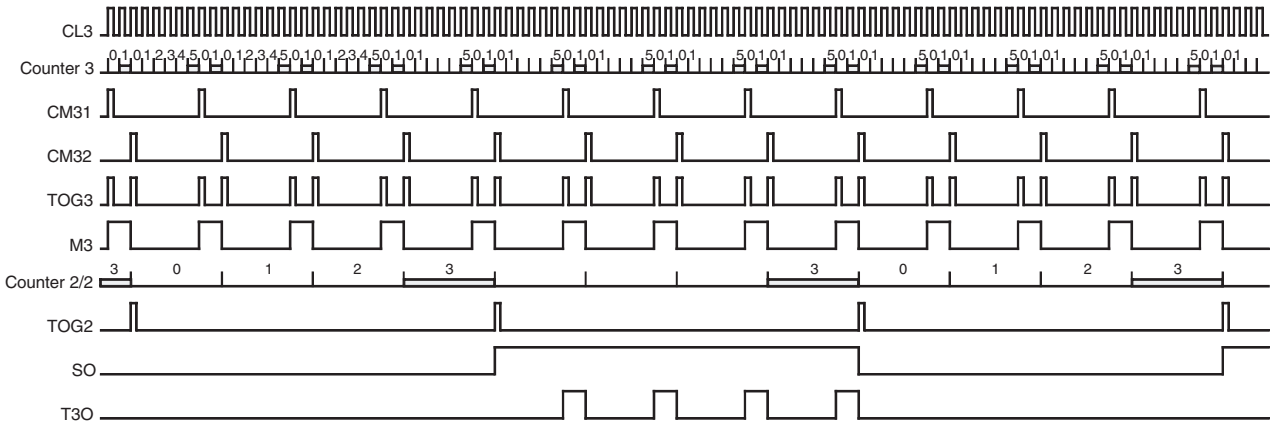


24.4.1 Combination Mode 12: Burst Modulation 2

SSI mode 1:	8-bit shift register internal data output (SO) to the Timer 3
Timer 2 output mode 2:	8-bit compare counter and 4-bit prescaler
Timer 2 output mode 1/6:	Timer 2 compare match toggles (TOG2) to the SSI
Timer 3 mode 7:	Carrier frequency burst modulation controlled by the internal output (SO) of SSI

The Timer 3 counter is driven by an internal or external clock source. Its compare- and compare mode registers must be programmed to generate the carrier frequency with the output toggle flip-flop (M3). The internal data output (SO) of the SSI is used to enable and disable the Timer 3 output. The SSI can be supplied with the toggle signal of Timer 2.

Figure 24-17. Burst Modulation 2



24.4.2 Combination Mode 13: FSK Modulation

SSI mode 1:	8-bit shift register internal data output (SO) to the Timer 3
Timer 2 output mode 3:	8-bit compare counter and 4-bit prescaler
Timer 2 output mode 1/6:	Timer 2 4-bit compare match signal (POUT) to the SSI
Timer 3 mode 8:	FSK modulation with shift register data output (SO)

The two compare registers are used to generate two different time intervals. The SSI data output selects which compare register is used for the output frequency generation. A "0" level at the SSI data output enables the compare register 1 and a "1" level enables the compare register 2. The compare- and compare mode registers must be programmed to generate the two frequencies via the output toggle flip-flop. The SSI can be supplied with the toggle signal of Timer 2 or any other clock source. The Timer 3 counter is driven by an internal or external clock source.

24.6 Serial Interface

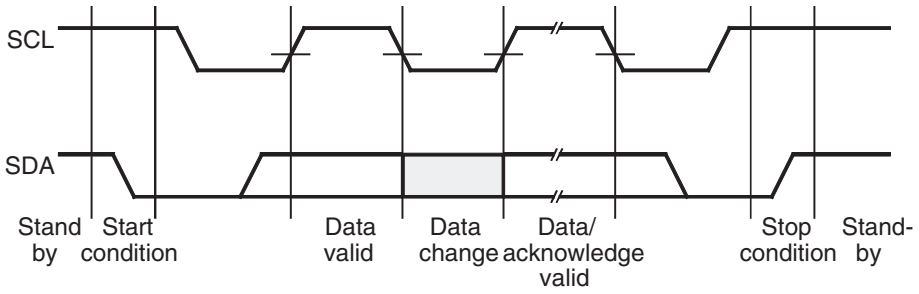
The EEPROM uses an two-wire serial (TWI) interface to the microcontroller for read and write accesses to the data. It is considered to be a slave in all these applications. That means, the controller has to be the master that initiates the data transfer and provides the clock for transmit and receive operations.

The serial interface is controlled by the microcontroller which generates the serial clock and controls the access via the SCL line and SDA line. SCL is used to clock the data into and out of the device. SDA is a bi-directional line that is used to transfer data into and out of the device. The following protocol is used for the data transfers.

24.6.1 Serial Protocol

- Data states on the SDA line changing only while SCL is low.
- Changes on the SDA line while SCL is high are interpreted as START or STOP condition.
- A START condition is defined as high to low transition on the SDA line while the SCL line is high.
- A STOP condition is defined as low to high transition on the SDA line while the SCL line is high.
- Each data transfer must be initialized with a START condition and terminated with a STOP condition. The START condition wakes the device from standby mode and the STOP condition returns the device to standby mode.
- A receiving device generates an acknowledge (A) after the reception of each byte. This requires an additional clock pulse, generated by the master. If the reception was successful the receiving master or slave device pulls down the SDA line during that clock cycle. If an acknowledge is not detected (N) by the interface in transmit mode, it will terminate further data transmissions and go into receive mode. A master device must finish its read operation by a non-acknowledge and then send a stop condition to bring the device into a known state.

Figure 24-20. MCL Protocol



- Before the START condition and after the STOP condition the device is in standby mode and the SDA line is switched as input with pull-up resistor.
- The control byte that follows the START condition determines the following operation. It consists of the 5-bit row address, 2 mode control bits and the READ/NWRITE bit that is used to control the direction of the following transfer. A "0" defines a write access and a "1" a read access.

27. DC Operating Characteristics (Continued)

V_{SS} = 0 V, T_{amb} = -40° C to +125° C unless otherwise specified.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Power-on Reset Threshold Voltage						
POR threshold voltage	BOT = 1	V_{POR}	1.54	1.7	1.88	V
POR threshold voltage	BOT = 0	V_{POR}	1.83	2.0	2.20	V
POR hysteresis		V_{POR}		50		mV
Voltage Monitor Threshold Voltage						
VM high threshold voltage	V_{DD} > VM, VMS = 1	V_{MThh}		3.0	3.35	V
VM high threshold voltage	V_{DD} < VM, VMS = 0	V_{MThh}	2.77	3.0		V
VM middle threshold voltage	V_{DD} > VM, VMS = 1	V_{MThm}		2.6	2.9	V
VM middle threshold voltage	V_{DD} < VM, VMS = 0	V_{MThm}	2.4	2.6		V
VM low threshold voltage	V_{DD} > VM, VMS = 1	V_{MThl}		2.2	2.44	V
VM low threshold voltage	V_{DD} < VM, VMS = 0	V_{MThl}	2.0	2.2		V
External Input Voltage						
VMI	V_{DD} = 3 V, VMS = 1	V_{VMI}		1.3	1.44	V
VMI	V_{DD} = 3 V, VMS = 0	V_{VMI}	1.18	1.3		V
All Bi-directional Ports						
Input voltage LOW	V_{DD} = 2.0 to 4.0 V	V_{IL}	V_{SS}		$0.2 \times V_{DD}$	V
Input voltage HIGH	V_{DD} = 2.0 to 4.0 V	V_{IH}	$0.8 \times V_{DD}$		V_{DD}	V
Input LOW current (switched pull-up)	V_{DD} = 2.0 V, V_{DD} = 3.0 V, V_{IL}= V_{SS}	I_{IL}	-3 -10	-8 -20	-14 -40	µA µA
Input HIGH current (switched pull-down)	V_{DD} = 2.0 V, V_{DD} = 3.0 V, V_{IH} = V_{DD}	I_{IH}	3 10	6 20	14 40	µA µA
Input LOW current (static pull-up)	V_{DD} = 2.0 V V_{DD} = 3.0 V, V_{IL}= V_{SS}	I_{IL}	-30 -80	-50 -160	-98 -320	µA µA
Input LOW current (static pull-down)	V_{DD} = 2.0 V V_{DD} = 3.0 V, V_{IH}= V_{DD}	I_{IH}	20 80	50 160	100 320	µA µA
Input leakage current	V_{IL} = V_{SS}	I_{IL}			100	nA
Input leakage current	V_{IH} = V_{DD}	I_{IH}			100	nA
Output LOW current	V_{OL} = 0.2 × V_{DD} V_{DD} = 2.0 V V_{DD} = 3.0 V	I_{OL}	0.9 3	1.8 5	3.6 8	mA mA
Output HIGH current	V_{OH} = 0.8 × V_{DD} V_{DD} = 2.0 V V_{DD} = 3.0 V	I_{OH}	-0.8 -3	-1.7 -5	-3.4 -8	mA mA

Note: The pin BP20/NTE has a static pull-up resistor during the reset-phase of the microcontroller

30. Emulation

The basic function of emulation is to test and evaluate the customer's program and hardware in real time. This therefore enables the analysis of any timing, hardware or software problem. For emulation purposes, all MARC4 controllers include a special emulation mode. In this mode, the internal CPU core is inactive and the I/O buses are available via Port 0 and Port 1 to allow an external access to the on-chip peripherals. The MARC4 emulator uses this mode to control the peripherals of any MARC4 controller (target chip) and emulates the lost ports for the application.

The MARC4 emulator can stop and restart a program at specified points during execution, making it possible for the applications engineer to view the memory contents and those of various registers during program execution. The designer also gains the ability to analyze the executed instruction sequences and all the I/O activities.

Figure 30-1. MARC4 Emulation