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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	UHF ASK/FSK
Core Processor	MARC4
Program Memory Type	FLASH (4kB)
Controller Series	MARC4 4-Bit
RAM Size	256 x 4
Interface	SSI
Number of I/O	11
Voltage - Supply	1.8V ~ 4V
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	24-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	24-SSO
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atam862p-tnsy8d

Figure 5-1. Block Diagram

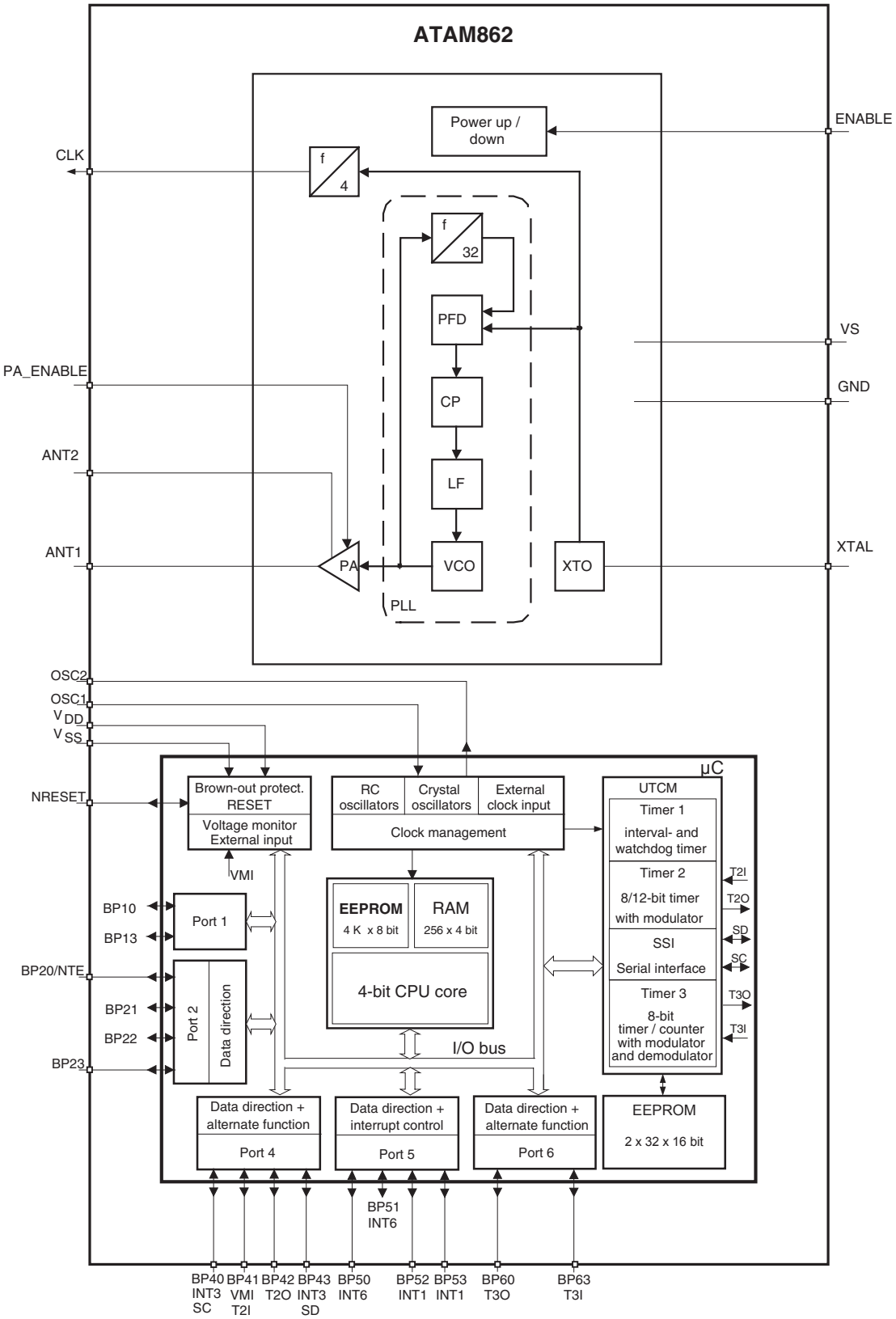
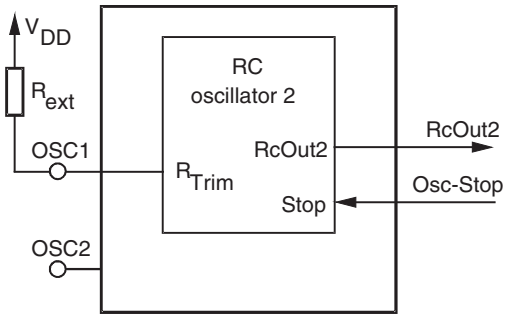


Figure 19-4. RC-oscillator 2



19.2.4 4-MHz Oscillator

The microcontroller block 4-MHz oscillator options need a crystal or ceramic resonator connected to the OSC1 and OSC2 pins to establish oscillation. All the necessary oscillator circuitry is integrated, except the actual crystal, resonator, C3 and C4.

Figure 19-5. 4-MHz Crystal Oscillator

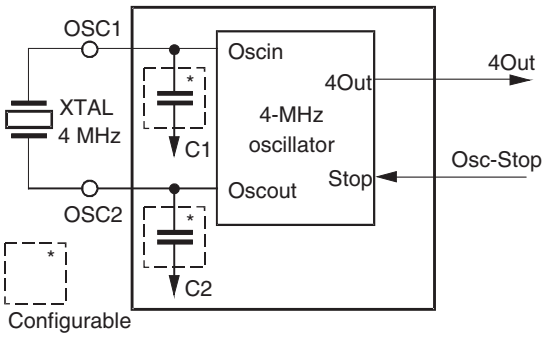
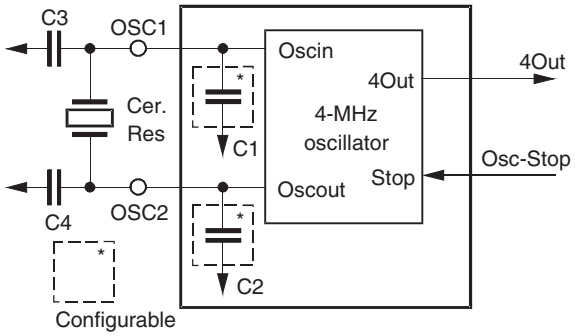


Figure 19-6. Ceramic Resonator



19.2.5 32-kHz Oscillator

Some applications require long-term time keeping or low resolution timing. In this case, an on-chip, low power 32-kHz crystal oscillator can be used to generate both the SUBCL and the SYSCL. In this mode, power consumption is greatly reduced. The 32-kHz crystal oscillator can not be stopped while the power-down mode is in operation.

22.3 Bi-directional Port 5

As all other bi-directional ports, this port includes a bitwise programmable Control Register (P5CR), which allows the individual programming of each port bit as input or output. It also opens up the possibility of reading the pin condition when in output mode. This is a useful feature for self testing and for serial bus applications.

The port pins can also be used as external interrupt inputs (see Figure 22-3 and Figure 22-4). The interrupts (INT1 and INT6) can be masked or independently configured to trigger on either edge. The interrupt configuration and port direction is controlled by the Port 5 Control Register (P5CR). An additional low resistance pull-up/pull-down transistor mask option provides an internal bus pull-up for serial bus applications.

The Port 5 Data Register (P5DAT) is I/O mapped to the primary address register of address "5"h and the Port 5 Control Register (P5CR) to the corresponding auxiliary register. The P5CR is a byte-wide register and is configured by writing first the low nibble and then the high nibble (see section "Addressing Peripherals" on page 32).

Figure 22-3. Bi-directional Port 5

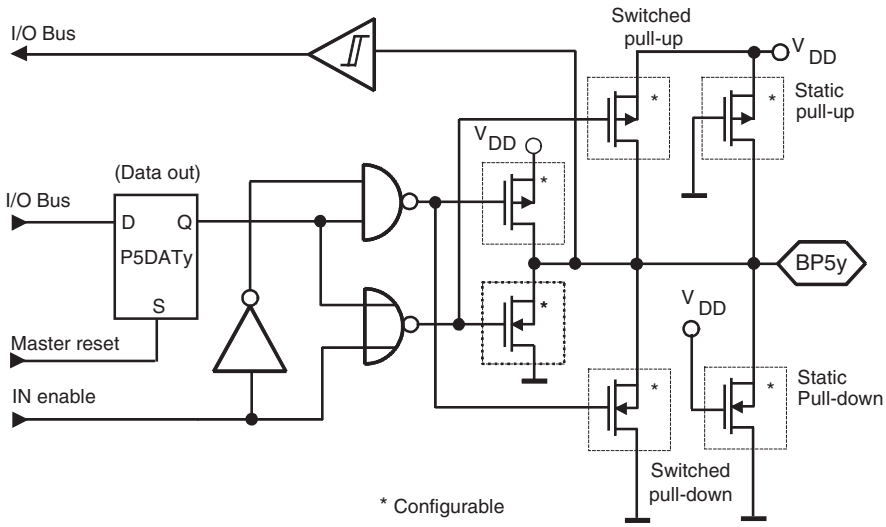
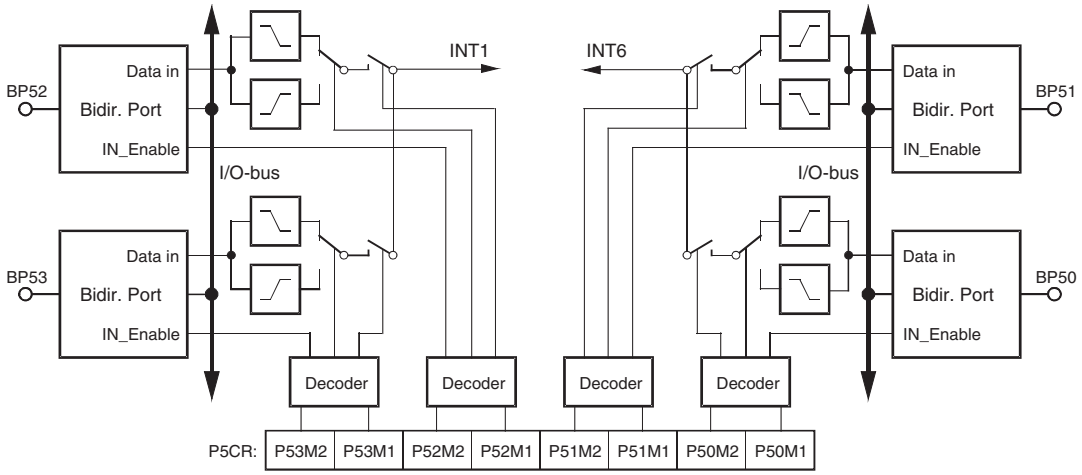


Figure 22-4. Port 5 External Interrupts



22.3.1 Port 5 Data Register (P5DAT)

Primary register address: "5"hex

Bit 3	Bit 2	Bit 1	Bit 0
P5DAT3	P5DAT2	P5DAT1	P5DAT0

Reset value: 1111b

22.3.2 Port 5 Control Register (P5CR) Byte Write

Auxiliary register address: "5"hex

	Bit 3	Bit 2	Bit 1	Bit 0	
First write cycle	P51M2	P51M1	P50M2	P50M1	**Reset value: 1111b**
	Bit 7	Bit 6	Bit 5	Bit 4	
Second write cycle	P53M2	P53M1	P52M2	P52M1	**Reset value: 1111b**

P5xM2, P5xM1 – Port 5x Interrupt Mode/Direction Code

Table 22-2. Port 5 Control Register

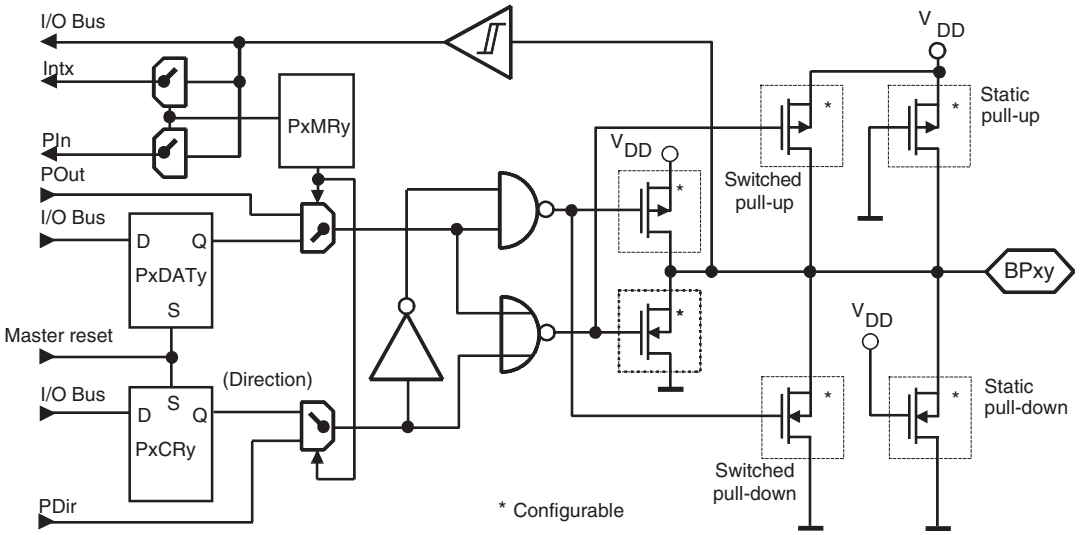
Auxiliary Address: "5"hex, First Write Cycle		**Second Write Cycle**	
Code 3 2 1 0	**Function**	**Code 3 2 1 0**	**Function**
x x 1 1	BP50 in input mode – interrupt disabled	x x 1 1	BP52 in input mode – interrupt disabled
x x 0 1	BP50 in input mode – rising edge interrupt	x x 0 1	BP52 in input mode – rising edge interrupt
x x 1 0	BP50 in input mode – falling edge interrupt	x x 1 0	BP52 in input mode – falling edge interrupt
x x 0 0	BP50 in output mode – interrupt disabled	x x 0 0	BP52 in output mode – interrupt disabled
1 1 x x	BP51 in input mode – interrupt disabled	1 1 x x	BP53 in input mode – interrupt disabled
0 1 x x	BP51 in input mode – rising edge interrupt	0 1 x x	BP53 in input mode – rising edge interrupt
1 0 x x	BP51 in input mode – falling edge interrupt	1 0 x x	BP53 in input mode – falling edge interrupt
0 0 x x	BP51 in output mode – interrupt disabled	0 0 x x	BP53 in output mode – interrupt disabled

22.4 Bi-directional Port 4

The bi-directional Port 4 is a bitwise configurable I/O port and provides the external pins for the Timer 2, SSI and the voltage monitor input (VMI). As a normal port, it performs in exactly the same way as bi-directional Port 2 (see Figure 22-5). Two additional multiplexes allow data and port direction control to be passed over to other internal modules (Timer 2, VM or SSI). The I/O pins for SC and SD line have an additional mode to generate an SSI interrupt.

All four Port 4 pins can be individually switched by the P4CR-register. Figure 22-5 shows the internal interfaces to bi-directional Port 4.

Figure 22-5. Bi-directional Port 4 and Port 6



22.4.1 Port 4 Data Register (P4DAT)

Primary register address: "4"hex

Bit 3	Bit 2	Bit 1	Bit 0	
P4DAT3	**P4DAT2**	**P4DAT1**	**P4DAT0**	**Reset value: 1111b**

22.4.2 Port 4 Control Register (P4CR) Byte Write

Auxiliary register address: "4"hex

	Bit 3	Bit 2	Bit 1	Bit 0	
First write cycle	**P41M2**	**P41M1**	**P40M2**	**P40M1**	**Reset value: 1111b**
	Bit 7	Bit 6	Bit 5	Bit 4	
Second write cycle	**P43M2**	**P43M1**	**P42M2**	**P42M1**	**Reset value: 1111b**

P4xM2, P4xM1 – Port 4x Interrupt mode/direction code

Table 22-4. Port 6 Control Register

Auxiliary Address: "6"hex		Write Cycle	
Code 3 2 1 0	**Function**	**Code 3 2 1 0**	**Function**
x x 1 1	BP60 in input mode	1 1 x x	BP63 in input mode
x x 1 0	BP60 in output mode	1 0 x x	BP63 in output mode
x x 0 x	BP60 enable alternate port function (T3O for Timer 3)	0 x x x	BP63 enable alternate port function (T3I for Timer 3)

22.6 Universal Timer/Counter/ Communication Module (UTCM)

The Universal Timer/counter/Communication Module (UTCM) consists of three timers (Timer 1,Timer 2, Timer 3) and a Synchronous Serial Interface (SSI).

- Timer 1 is an interval timer that can be used to generate periodical interrupts and as prescaler for Timer 2, Timer 3, the serial interface and the watchdog function.
- Timer 2 is an 8/12-bit timer with an external clock input (T2I) and an output (T2O).
- Timer 3 is an 8-bit timer/counter with its own input (T3I) and output (T3O).
- The SSI operates as two wire serial interface or as shift register for modulation and demodulation. The modulator and demodulator units work together with the timers and shift the data bits into or out of the shift register.

There is a multitude of modes in which the timers and the serial interface can work together.

This timer starts running automatically after any power-on reset! If the watchdog function is not activated, the timer can be restarted by writing into the T1C1 register with T1RM = 1.

Timer 1 can also be used as a watchdog timer to prevent a system from stalling. The watchdog timer is a 3-bit counter that is supplied by a separate output of Timer 1. It generates a system reset when the 3-bit counter overflows. To avoid this, the 3-bit counter must be reset before it overflows. The application software has to accomplish this by reading the CWD register.

After power-on reset the watchdog must be activated by software in the $RESET initialization routine. There are two watchdog modes, in one mode the watchdog can be switched on and off by software, in the other mode the watchdog is active and locked. This mode can only be stopped by carrying out a system reset.

The watchdog timer operation mode and the time interval for the watchdog reset can be programmed via the watchdog control register (WDC).

Figure 22-7. Timer 1 Module

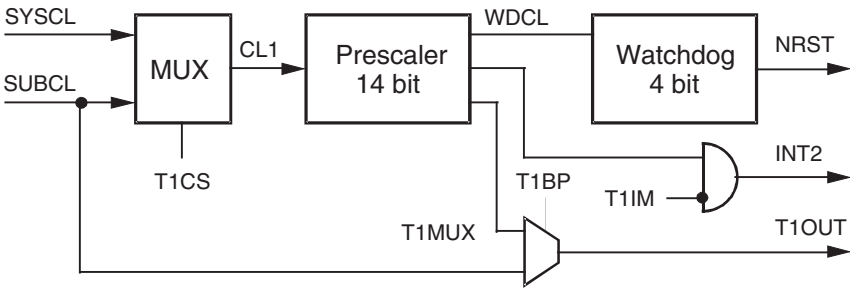


Figure 22-8. Timer 1 and Watchdog

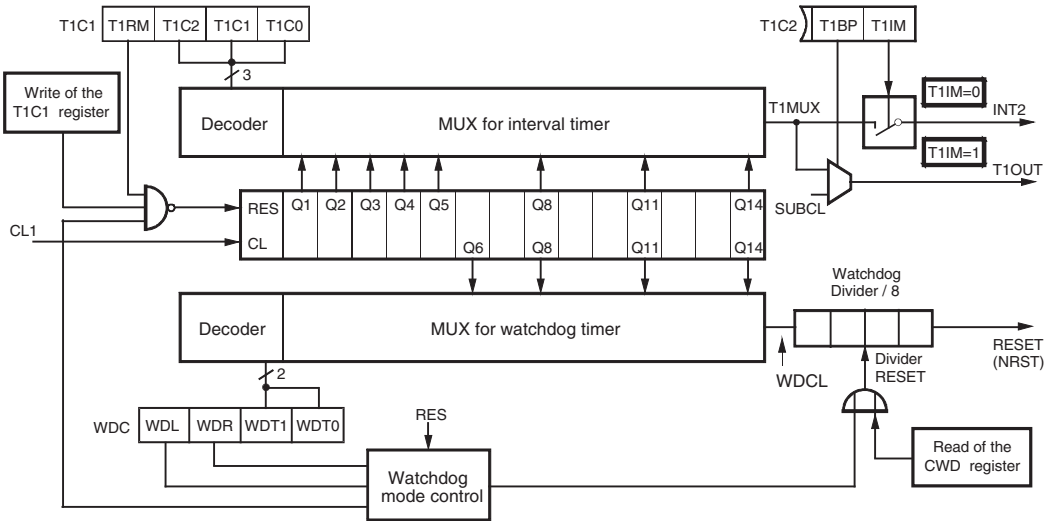
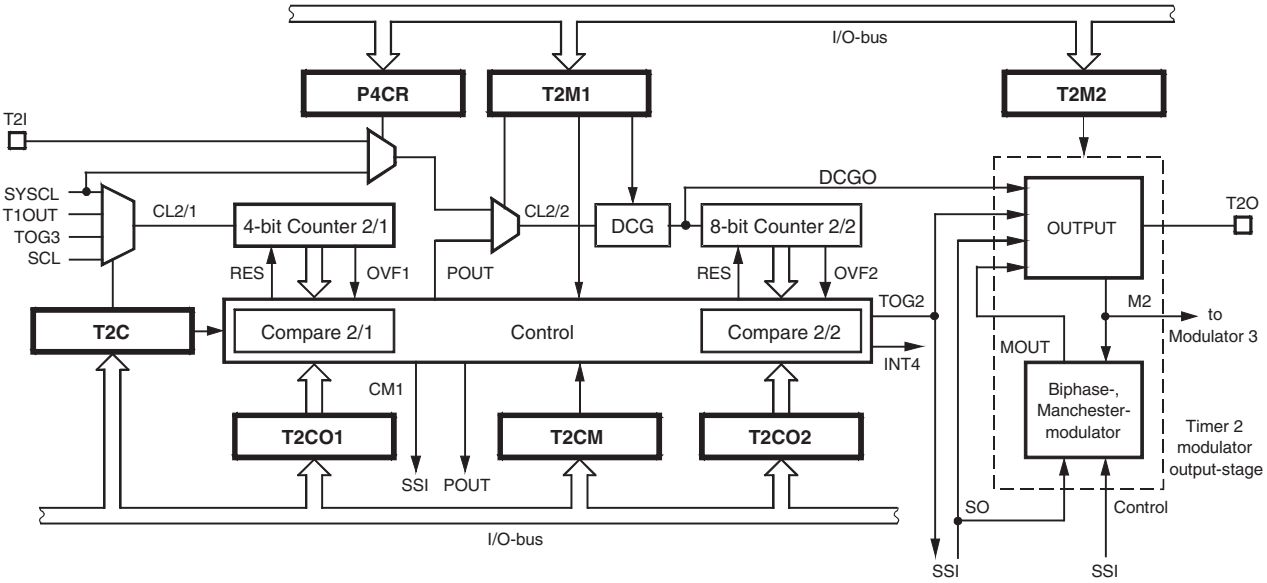


Figure 22-9. Timer 2

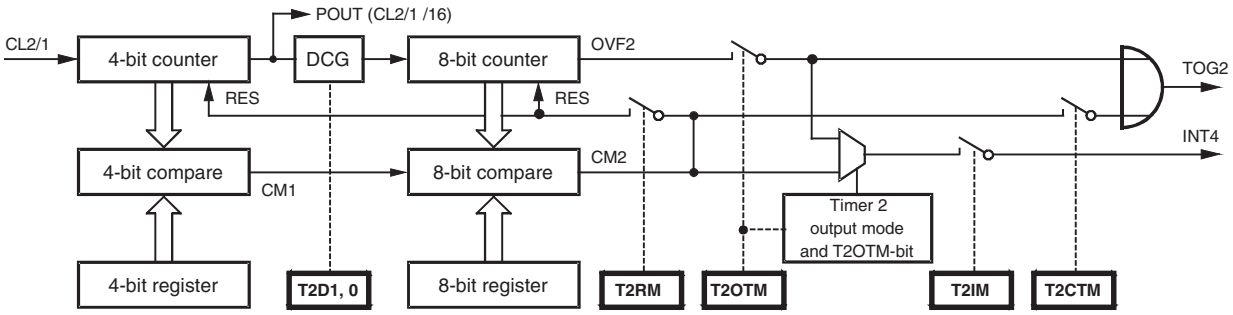


22.9 Timer 2 Modes

22.9.1 Mode 1: 12-bit Compare Counter

The 4-bit stage and the 8-bit stage work together as a 12-bit compare counter. A compare match signal of the 4-bit and the 8-bit stage generates the signal for the counter reset, toggle flip-flop or interrupt. The compare action is programmable via the compare mode register (T2CM). The 4-bit counter overflow (OVF1) supplies the clock output (POUT) with clocks. The duty cycle generator (DCG) has to be bypassed in this mode.

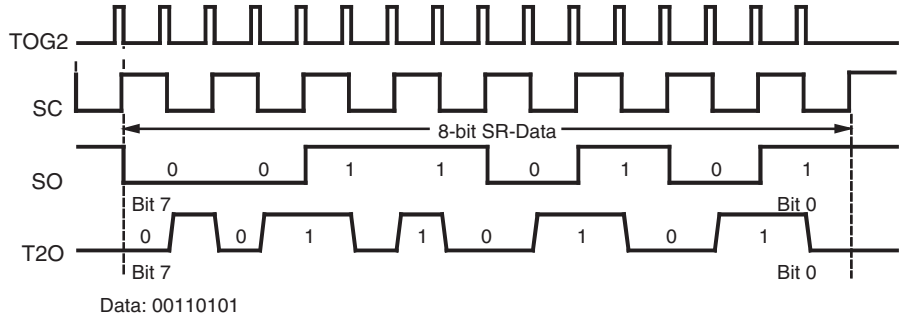
Figure 22-10. 12-bit Compare Counter



22.11.5 Timer 2 Output Mode 5

Manchester Modulator: Timer 2 modulates the SSI internal data output (SO) to Manchester code

Figure 22-20. Manchester Modulation

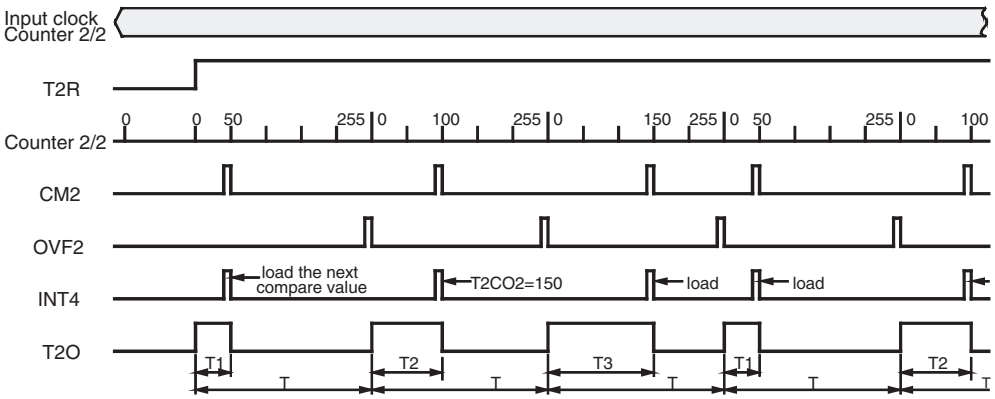


22.11.6 Timer 2 Output Mode 7

In this mode the timer overflow defines the period and the compare register defines the duty cycle. During one period only the first compare match occurrence is used to toggle the timer output flip-flop, until the overflow all further compare match are ignored. This avoids the situation that changing the compare register causes the occurrence of several compare match during one period. The resolution at the pulse-width modulation Timer 2 mode 1 is 12-bit and all other Timer 2 modes are 8-bit.

PWM Mode: Pulse-width modulation output on Timer 2 output pin (T2O)

Figure 22-21. PWM Modulation



22.12 Timer 2 Registers

Timer 2 has 6 control registers to configure the timer mode, the time interval, the input clock and its output function. All registers are indirectly addressed using extended addressing as described in section "Addressing Peripherals". The alternate functions of the Ports BP41 or BP42 must be selected with the Port 4 control register P4CR, if one of the Timer 2 modes require an input at T2I/BP41 or an output at T2O/BP42.

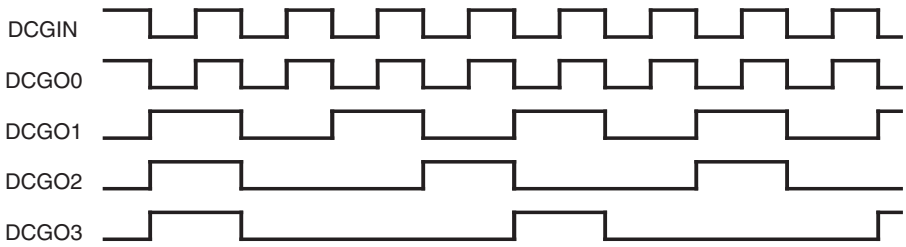
Table 22-9. Timer 2 Mode Select Bits

Mode	T2MS1	T2MS0	Clock Output (POUT)	Timer 2 Modes
1	1	1	4-bit counter overflow (OVF1)	12-bit compare counter; the DCG has to be bypassed in this mode
2	1	0	4-bit compare output (CM1)	8-bit compare counter with 4-bit programmable prescaler and duty cycle generator
3	0	1	4-bit compare output (CM1)	8-bit compare counter clocked by SYSCL or the external clock input T2I, 4-bit prescaler run, the counter 2/1 starts after writing mode 3
4	0	0	4-bit compare output (CM1)	8-bit compare counter clocked by SYSCL or the external clock input T2I, 4-bit prescaler stop and resets

22.12.3 Duty Cycle Generator

The duty cycle generator generates duty cycles of 25%, 33% or 50%. The frequency at the duty cycle generator output depends on the duty cycle and the Timer 2 prescaler setting. The DCG-stage can also be used as additional programmable prescaler for Timer 2.

Figure 22-22. DCG Output Signals



22.12.4 Timer 2 Mode Register 2 (T2M2)

Address: "7"hex - Subaddress: "2"hex

Bit 3	Bit 2	Bit 1	Bit 0
T2TOP	**T2OS2**	**T2OS1**	**T2OS0**

Reset value: 1111b

T2TOP	**T**imer **2** **T**oggle **O**utput **P**reset This bit allows the programmer to preset the Timer 2 output T2O. T2TOP = 0, resets the toggle outputs with the write cycle (M2 = 0) T2TOP = 1, sets toggle outputs with the write cycle (M2 = 1) **Note: If T2R = 1, no output preset is possible**
T2OS2	**T**imer **2** **O**utput **S**elect bit **2**
T2OS1	**T**imer **2** **O**utput **S**elect bit **1**
T2OS0	**T**imer **2** **O**utput **S**elect bit **0**

A special feature of this timer is the trigger- and single-action mode. In trigger mode, the counter starts counting triggered by the external signal at its input. In single-action mode, the counter counts only one time up to the programmed compare match event. These modes are very useful for modulation, demodulation, signal generation, signal measurement and phase controlling. For phase controlling, the timer input is protected against negative voltages and has zero-cross detection capability.

Timer 3 has a modulator output stage and input functions for demodulation. As modulator it works together with Timer 2 or the serial interface. When the shift register is used for modulation the data shifted out of the register is encoded bitwise. In all demodulation modes, the decoded data bits are shifted automatically into the shift register.

23.2 Timer/Counter Modes

Timer 3 has 6 timer modes and 6 modulator/demodulator modes. The mode is set via the Timer 3 Mode Register T3M.

In all these modes, the compare register and the compare-mode register belonging to it define the counter value for a compare match and the action of a compare match. A match of the current counter value with the content of one compare register triggers a counter reset, a Timer 3 interrupt or the toggling of the output flip-flop. The compare mode registers T3M1 and T3M2 contain the mask bits for enabling or disabling these actions.

The counter can also be enabled to execute single actions with one or both compare registers. If this mode is set the corresponding compare match event is generated only once after the counter start.

Most of the timer modes use their compare registers alternately. After the start has been activated, the first comparison is carried out via the compare register 1, the second is carried out via the compare register 2, the third is carried out again via the compare register 1 and so on. This makes it easy to generate signals with constant periods and variable duty cycle or to generate signals with variable pulse and space widths.

If single-action mode is set for one compare register, the comparison is always carried out after the first cycle via the other compare register.

The counter can be started and stopped via the control register T3C. This register also controls the initial level of the output before start. T3C contains the interrupt mask for a T3I input interrupt.

Via the Timer 3 clock-select register, the internal or external clock source can be selected. This register selects also the active edge of the external input. An edge at the external input T3I can generate also an interrupt if the T3EIM-bit is set and the Timer 3 is stopped (T3R = 0) in the T3C-register.

Figure 23-4. Counter Reset with Compare Register 2 and Toggle with Start

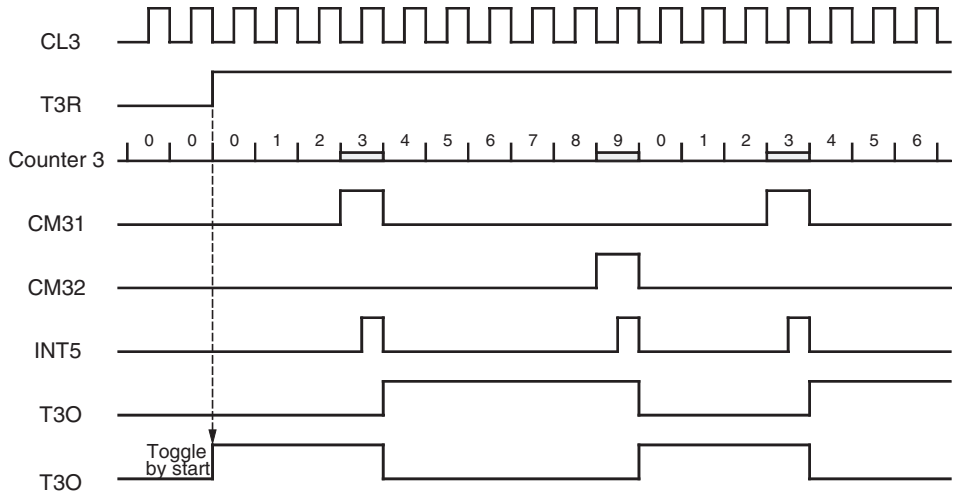
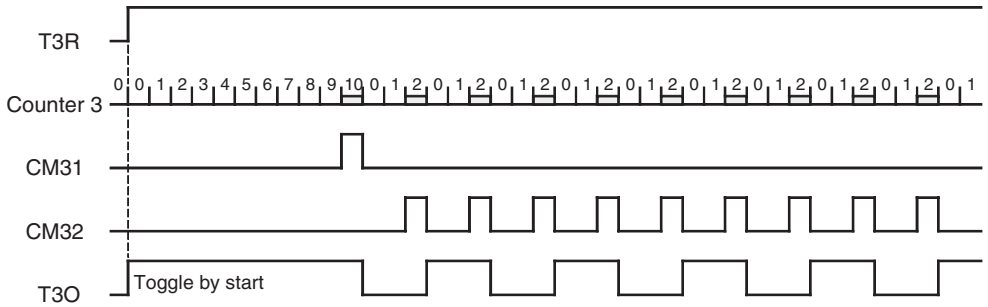


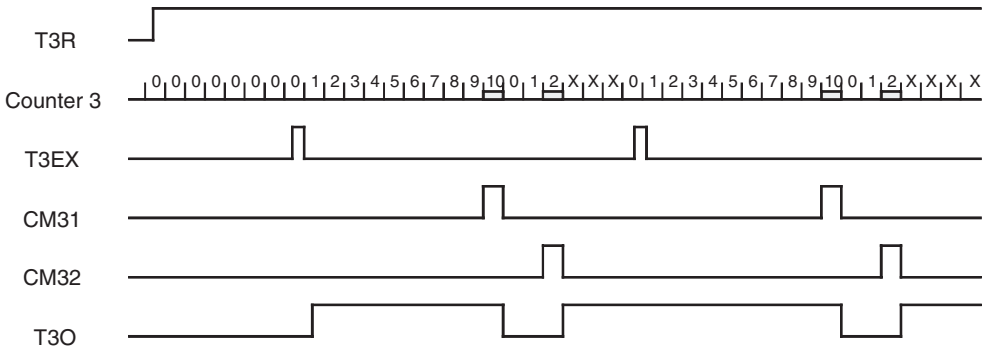
Figure 23-5. Single Action of Compare Register 1



23.2.2 Timer 3 – Mode 2: Timer/Counter, External Trigger Restart and External Capture (with T3I Input)

The counter is driven by an internal clock source. After starting with T3R, the first edge from the external input T3I starts the counter. The following edges at T3I load the current counter value into the capture register, reset the counter and restart it. The edge can be selected by the programmable edge decoder of the timer input stage. If single-action mode is activated for one or both compare registers the trigger signal restarts the single action.

Figure 23-6. Externally Triggered Counter Reset and Start Combined with Single-action Mode

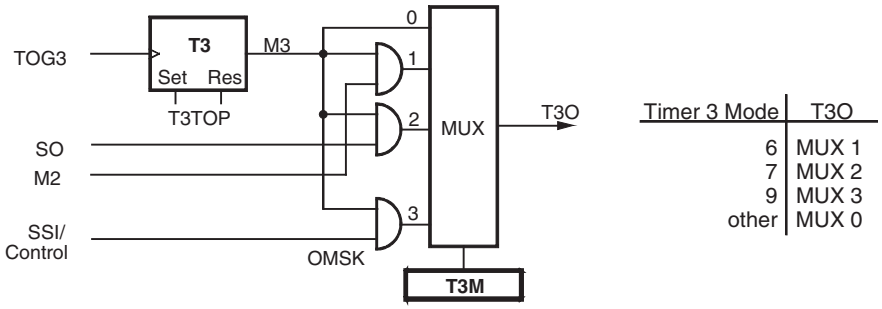


23.4 Timer 3 Modulator for Carrier Frequency Burst Modulation

If the output stage operates as pulse-width modulator for the shift register, the output can be stopped with stage 1 of Timer 2. For this task, the timer mode 3 must be used and the prescaler must be supplied by the internal shift clock of the shift register.

The modulator can be started with the start of the shift register (SIR = 0) and stopped either by a shift register stop (SIR = 1) or compare match event of stage 1 of Timer 2. For this task, the Timer 2 must be used in mode 3 and the prescaler stage must be supplied by the internal shift clock of the shift register.

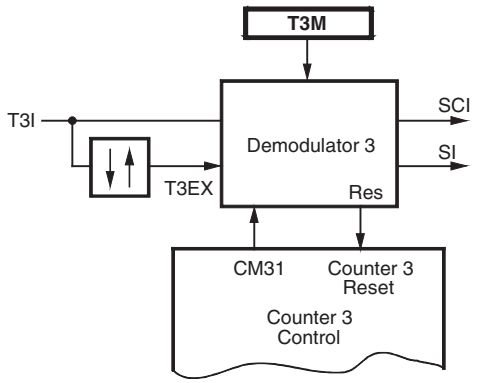
Figure 23-13. Modulator 3



23.5 Timer 3 Demodulator for Biphase, Manchester and Pulse-width-modulated Signals

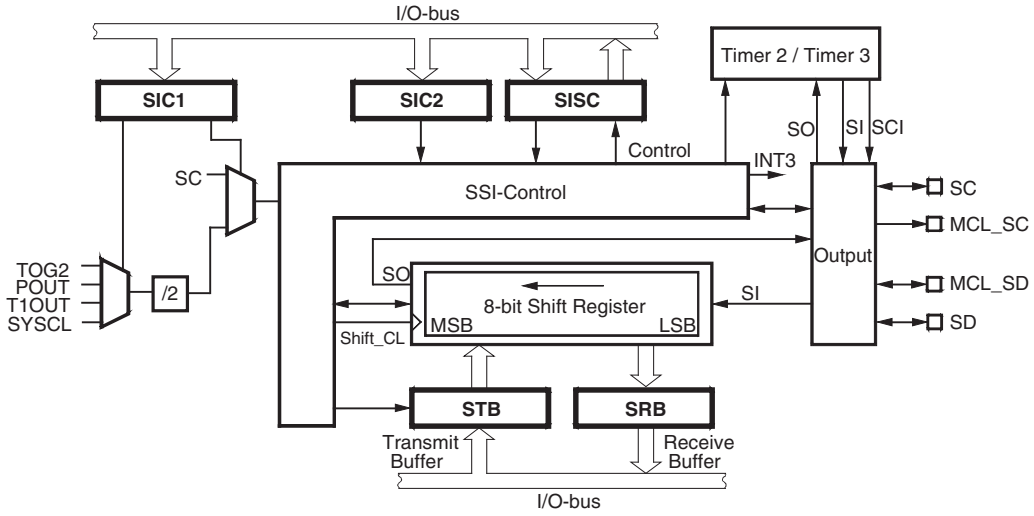
The demodulator stage of Timer 3 can be used to decode Biphase, Manchester and pulse-width-coded signals.

Figure 23-14. Timer 3 Demodulator 3



4. Multi-chip link (MCL) – the SSI can also be used as an interchip data interface for use in single package multi-chip modules or hybrids. For such applications, the SSI is provided with two dedicated pads (MCL_SD and MCL_SC) which act as a two-wire chip-to-chip link. The MCL can be activated by the MCL control bit. Should these MCL pads be used by the SSI, the standard SD and SC pins are not required and the corresponding Port 4 ports are available as conventional data ports.

Figure 23-15. Block Diagram of the Synchronous Serial Interface



23.8.3 General SSI Operation

The SSI is comprised essentially of an 8-bit shift register with two associated 8-bit buffers – the receive buffer (SRB) for capturing the incoming serial data and a transmit buffer (STB) for intermediate storage of data to be serially output. Both buffers are directly accessable by software. Transferring the parallel buffer data into and out of the shift register is controlled automatically by the SSI control, so that both single byte transfers or continuous bit streams can be supported.

The SSI can generate the shift clock (SC) either from one of several on-chip clock sources or accept an external clock. The external shift clock is output on, or applied to the Port BP40. Selection of an external clock source is performed by the Serial Clock Direction control bit (SCD). In the combinational modes, the required clock is selected by the corresponding timer mode.

The SSI can operate in three data transfer modes – synchronous 8-bit shift mode, MCL compatible 9-bit shift modes or 8-bit pseudo MCL protocol (without acknowledge-bit).

External SSI clocking is not supported in these modes. The SSI should thus generate and has full control over the shift clock so that it can always be regarded as an MCL Bus Master device.

All directional control of the external data port used by the SSI is handled automatically and is dependent on the transmission direction set by the Serial Data Direction (SDD) control bit. This control bit defines whether the SSI is currently operating in Transmit (TX) mode or Receive (RX) mode.

Serial data is organized in 8-bit telegrams which are shifted with the most significant bit first. In the 9-bit MCL mode, an additional acknowledge bit is appended to the end of the telegram for handshaking purposes (see “MCL Bus Protocol” on page 77).

and the SSI will continue clocking in the next telegram. Should, however, the first telegram not have been read (SRDY = 1), then the SSI will stop, temporarily holding the second telegram in the shift register until a certain point of time when the controller is able to service the receive buffer. In this way no data is lost or overwritten.

Deactivating the SSI (SIR = 1) in mid-telegram will immediately stop the shift clock and latch the present contents of the shift register into the receive buffer. This can be used for clocking in a data telegram of less than 8 bits in length. Care should be taken to read out the final complete 8-bit data telegram of a multiple word message before deactivating the SSI (SIR = 1) and terminating the reception. After termination, the shift register contents will overwrite the receive buffer.

Figure 23-17. Example of 8-bit Synchronous Transmit Operation

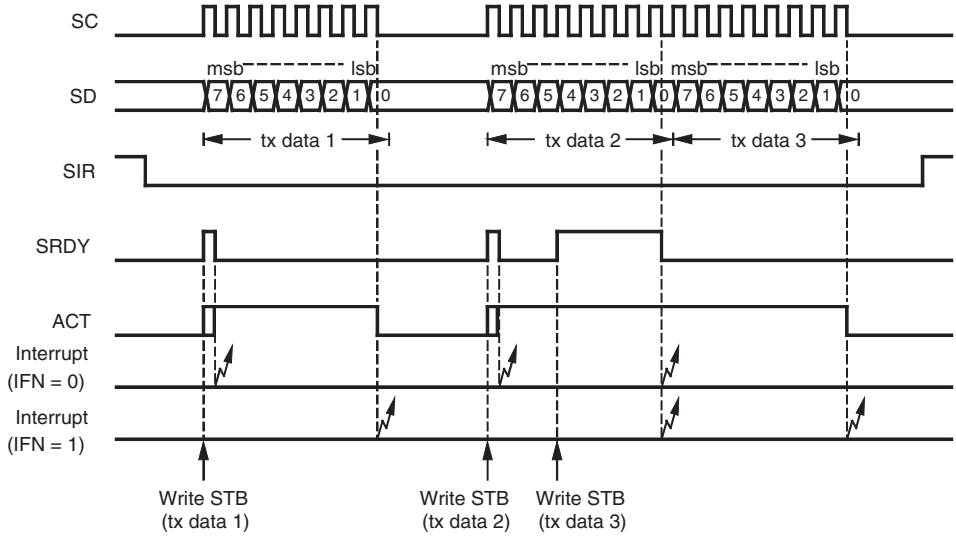
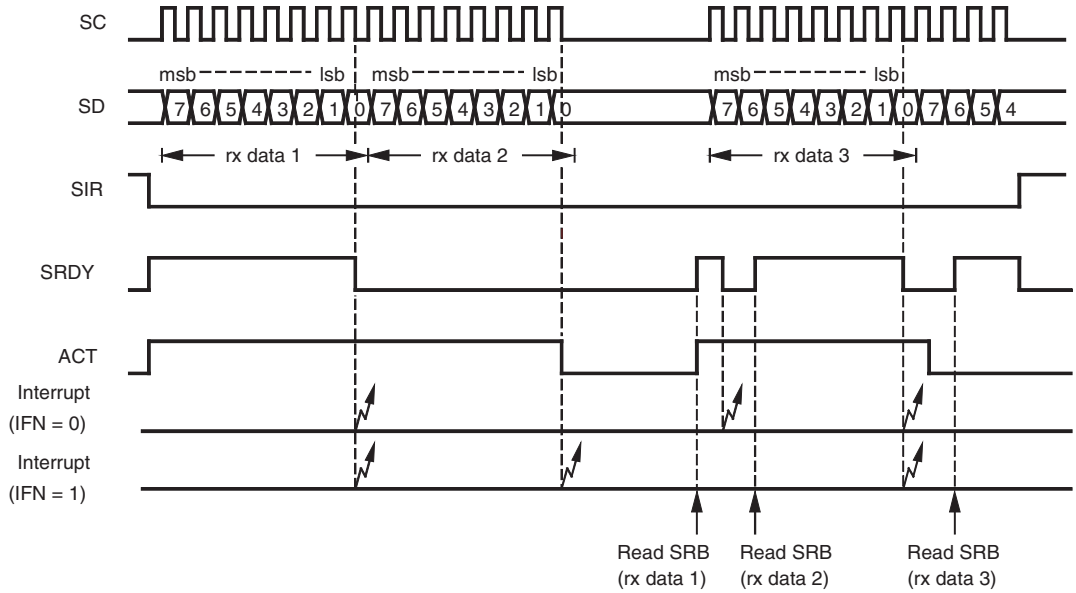


Figure 23-18. Example of 8-bit Synchronous Receive Operation



23.9 Serial Interface Registers

23.9.1 Serial Interface Control Register 1 (SIC1)

Auxiliary register address: "9"hex

Bit 3	Bit 2	Bit 1	Bit 0
SIR	**SCD**	**SCS1**	**SCS0**

Reset value: 1111b

SIR — **S**erial **I**nterface **R**eset
SIR = 1, SSI inactive
SIR = 0, SSI active

SCD — **S**erial **C**lock **D**irection
SCD = 1, SC line used as output
SCD = 0, SC line used as input

Note: This bit has to be set to "1" during the MCL mode and the Timer 3 mode 10 or 11

SCS1 — **S**erial **C**lock source **S**elect bit **1**

SCS0 — **S**erial **C**lock source **S**elect bit **0**

Note: With SCD = 0 the bits SCS1 and SCS0 are insignificant

Table 23-4. Serial Clock Source Select Bits

SCS1	SCS0	Internal Clock for SSI
1	1	SYSCL/2
1	0	T1OUT/2
0	1	POUT/2
0	0	TOG2/2

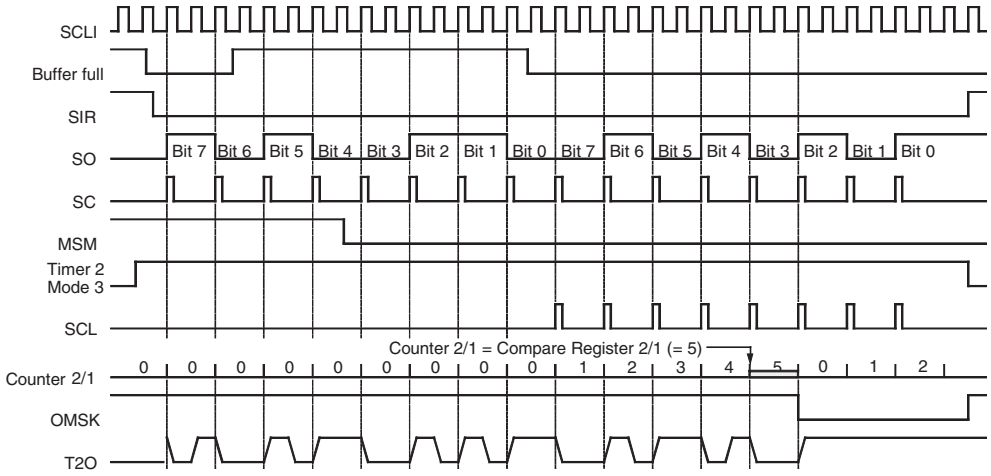
- In transmit mode (SDD = 1) shifting starts only if the transmit buffer has been loaded (SRDY = 1).
- Setting SIR-bit loads the contents of the shift register into the receive buffer (synchronous 8-bit mode only).
- In MCL modes, writing a 0 to SIR generates a start condition and writing a 1 generates a stop condition.

24.1.5 Combination Mode 5: Biphase Modulation 2

SSI mode 1:	8-bit shift register internal data output (SO) to the Timer 2 modulator stage
Timer 2 mode 3:	8-bit compare counter and 4-bit prescaler
Timer 2 output mode 4:	The modulator 2 of Timer 2 modulates the SSI data output to Biphase code

The 4-bit stage can be used as prescaler for the SSI to generate the stop signal for modulator 2. The SSI has a special mode to supply the prescaler via the shift clock. The control output signal (OMSK) of the SSI is used as stop signal for the modulator. Figure 24-6 shows an example for a 13-bit Biphase telegram.

Figure 24-6. Biphase Modulation 2



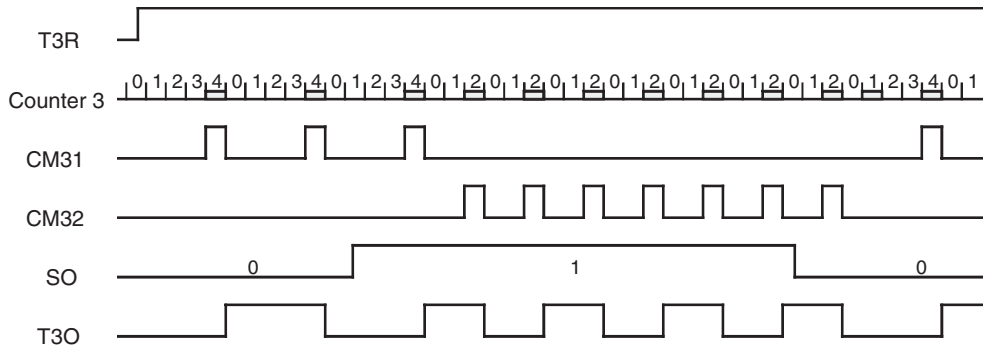
24.2.1 Combination Mode 6: FSK Modulation

SSI mode 1: 8-bit shift register internal data output (SO) to the Timer 3

Timer 3 mode 8: FSK modulation with shift register data (SO)

The two compare registers are used to generate two varied time intervals. The SSI data output selects which compare register is used for the output frequency generation. A "0" level at the SSI data output enables the compare register 1 and a "1" level enables the compare register 2. The compare and compare mode registers must be programmed to generate the two frequencies via the output toggle flip-lop. The SSI can be supplied with the toggle signal of Timer 2 or any other clock source. The Timer 3 counter is driven by an internal or external clock source.

Figure 24-8. FSK Modulation



24.2.2 Combination Mode 7: Pulse-width Modulation (PWM)

SSI mode 1: 8-bit shift register internal data output (SO) to the Timer 3

Timer 3 mode 9: Pulse-width modulation with the shift register data (SO)

The two compare registers are used to generate two varied time intervals. The SSI data output selects which compare register is used for the output pulse generation. In this mode, both compare and compare mode registers must be programmed to generate the two pulse width. It is also useful to enable the single-action mode for extreme duty cycles. Timer 2 is used as baudrate generator and for the triggered restart of Timer 3. The SSI must be supplied with the toggle signal of Timer 2. The counter is driven by an internal or external clock source.

Figure 24-9. Pulse-width Modulation

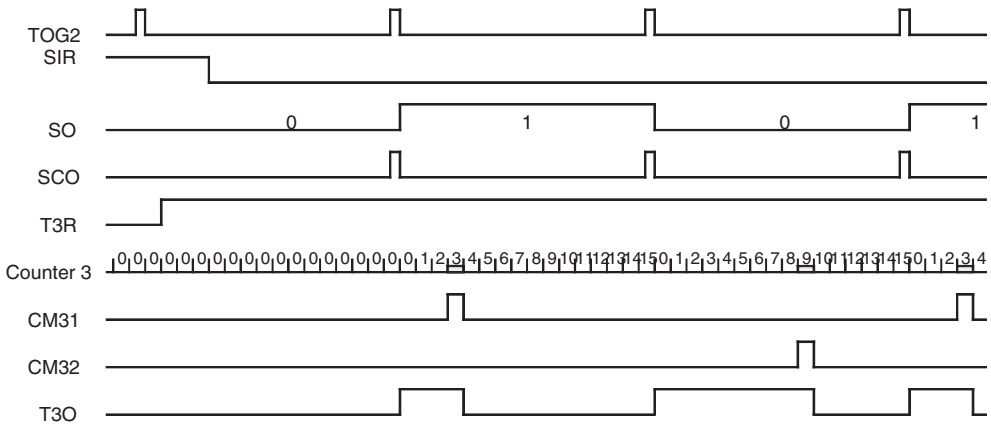
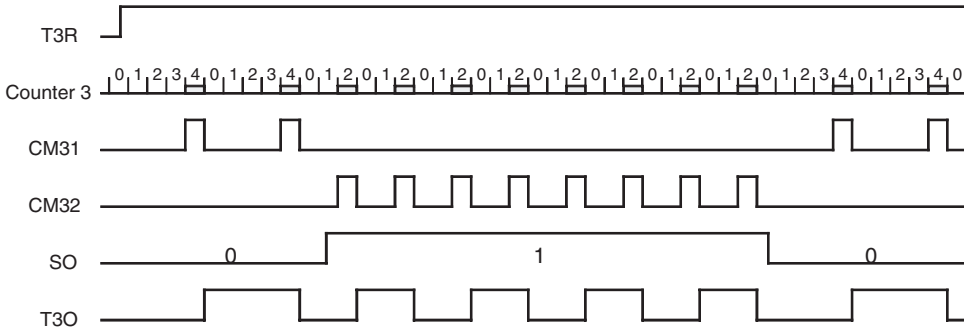


Figure 24-18. FSK Modulation



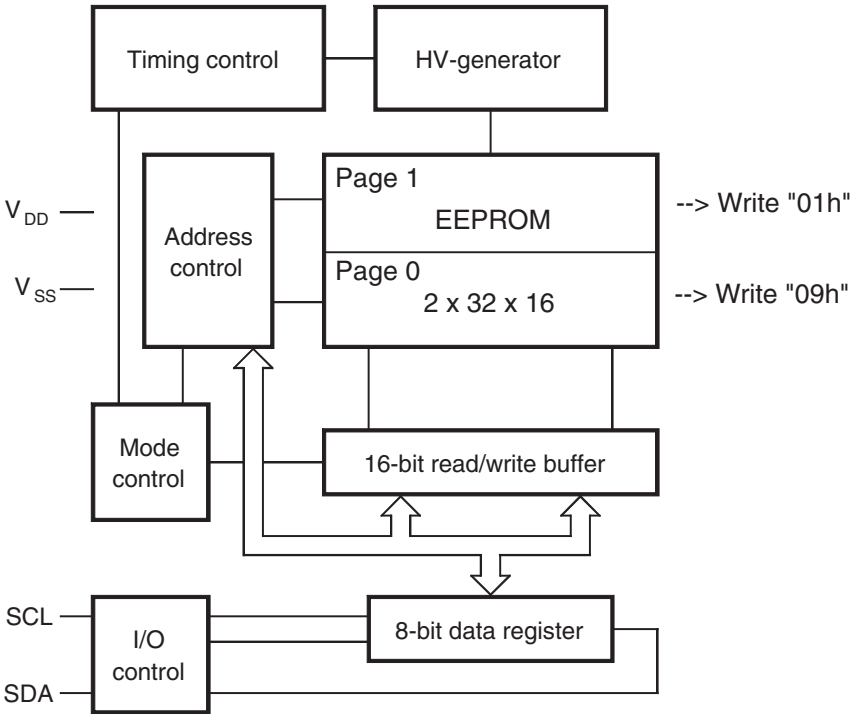
24.5 Data EEPROM

The internal data EEPROM offers 2 pages of 512 bits each. Both pages are organized as 32 × 16-bit words. The programming voltage as well as the write cycle timing is generated on chip. To be compatible with the ROM parts, two restrictions have to be taken into account:

- To use the same EEPROM page as with the ROM parts the application software has to write the MCL-command “09h” to the EEPROM. This command has no effect for the microcontroller if it is left inside the HEX-file for the ROM version.
- Data handling for read and write is performed using the serial interface MCL.

The page select is performed by either writing “01h” (page 1) or “09h” (page 0) to the EEPROM.

Figure 24-19. Data EEPROM



24.6 Serial Interface

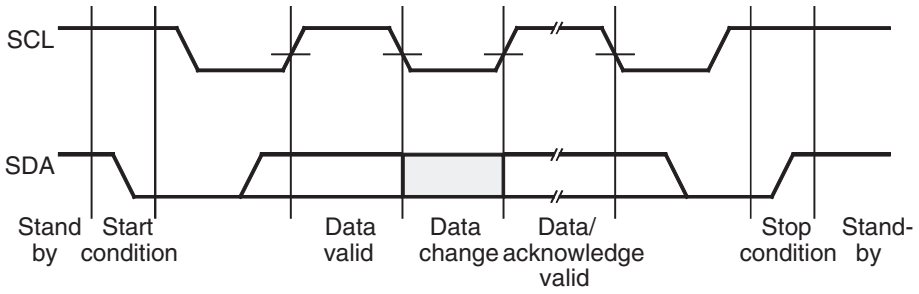
The EEPROM uses an two-wire serial (TWI) interface to the microcontroller for read and write accesses to the data. It is considered to be a slave in all these applications. That means, the controller has to be the master that initiates the data transfer and provides the clock for transmit and receive operations.

The serial interface is controlled by the microcontroller which generates the serial clock and controls the access via the SCL line and SDA line. SCL is used to clock the data into and out of the device. SDA is a bi-directional line that is used to transfer data into and out of the device. The following protocol is used for the data transfers.

24.6.1 Serial Protocol

- Data states on the SDA line changing only while SCL is low.
- Changes on the SDA line while SCL is high are interpreted as START or STOP condition.
- A START condition is defined as high to low transition on the SDA line while the SCL line is high.
- A STOP condition is defined as low to high transition on the SDA line while the SCL line is high.
- Each data transfer must be initialized with a START condition and terminated with a STOP condition. The START condition wakes the device from standby mode and the STOP condition returns the device to standby mode.
- A receiving device generates an acknowledge (A) after the reception of each byte. This requires an additional clock pulse, generated by the master. If the reception was successful the receiving master or slave device pulls down the SDA line during that clock cycle. If an acknowledge is not detected (N) by the interface in transmit mode, it will terminate further data transmissions and go into receive mode. A master device must finish its read operation by a non-acknowledge and then send a stop condition to bring the device into a known state.

Figure 24-20. MCL Protocol



- Before the START condition and after the STOP condition the device is in standby mode and the SDA line is switched as input with pull-up resistor.
- The control byte that follows the START condition determines the following operation. It consists of the 5-bit row address, 2 mode control bits and the READ/NWRITE bit that is used to control the direction of the following transfer. A "0" defines a write access and a "1" a read access.