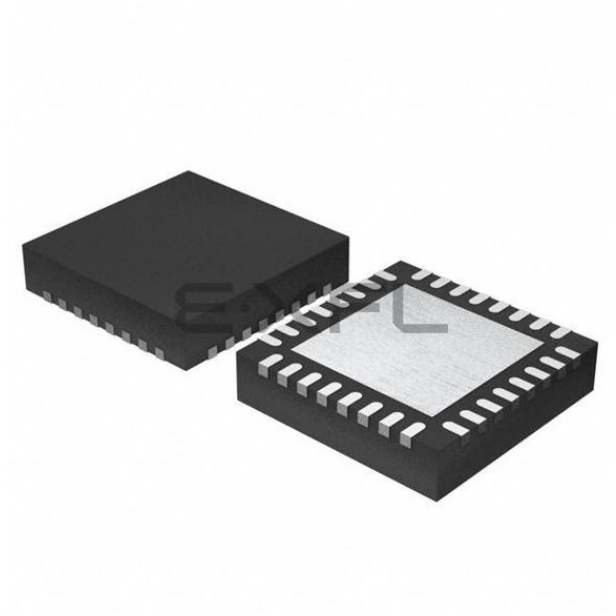

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Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	20.48MHz
Connectivity	LINbus, SPI
Peripherals	POR, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 32
Voltage - Supply (Vcc/Vdd)	3.5V ~ 18V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 115°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad, CSP
Supplier Device Package	32-LFCSP-VQ (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7039bcp6z

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Solutions Bulletins & Brochures

- Emerging Energy Applications Solutions Bulletin, Volume 10, Issue 4

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	V_{DD} = 7.0 V … 18 V t_{BIT} = 96 µs D4 = $t_{BUS\_REC(MAX)}/(2 \times t_{BIT})$				
t_{RX_PDR}[1, 20]	Propagation delay of receiver			6	µs
t_{RX_SYM}[1, 20]	Symmetry of receiver propagation delay rising edge, with respect to falling edge ($t_{RX\_SYM} = t_{RF\_PDR} - t_{RX\_PDF}$)	−2		+2	µs
PACKAGE THERMAL SPECIFICATIONS					
Thermal Impedance (θ_{JA})[21]	32-lead CSP, stacked die		32		°C/W
POWER REQUIREMENTS[1]					
Power Supply Voltages					
VDD (Battery Supply)		3.5		18	V
REG_DVDD, REG_AVDD[22]		2.45	2.6	2.75	V
Power Consumption					
I_{DD} (MCU Normal Mode)[23]	ADC off (20.48 MHz)		10	20	mA
	ADC off (10.24 MHz)		7.5	16	mA
I_{DD} (MCU Powered Down)[1]	ADC low power mode, measured over an ambient temperature range of T_A = −10°C to +40°C, continuous ADC conversion		750	1000	µA
I_{DD} (MCU Powered Down)[1]	Precision oscillator turned off, ADC off				
	Average current, measured with wake-up and watchdog timers clocked from low power oscillator (−40°C to +85°C)		95	300	µA
	Average current, measured with wake-up and watchdog timers clocked from low power oscillator over an ambient temperature range of −10°C to +40°C		95	175	µA
I_{DD} (Current ADC)			1.7		mA
I_{DD} (Voltage/Temperature ADC)			0.5		mA
I_{DD} (Precision Oscillator)			400		µA

[1] Not guaranteed by production test but by design and/or characterization data at production release.
[2] Valid for current ADC gain setting of PGA up to 64.
[3] These numbers include temperature drift.
[4] The offset error drift is included in the offset error. This typical specification is an indicator of the offset error due to temperature drift. This typical value is the mean of the temperature drift characterization data distribution.
[5] Includes internal reference temperature drift.
[6] User system calibration removes this error at a given temperature and at a given gain on the current channel.
[7] The gain drift is included in the total gain error. This typical specification is an indicator of the gain error due to temperature drift. This typical value is the mean of the temperature drift characterization data distribution.
[8] Voltage channel specifications include resistive attenuator input stage.
[9] RMS noise is referred to voltage attenuator input; for example, at f_{ADC} = 1 kHz, typical rms noise at the ADC input is 7.5 µV, scaled by the attenuator (24) yields these input referred noise figures.
[10] Valid after an initial self calibration.
[11] It is possible to extend the ADC input range by up to 10% by modifying the factory set value of the gain calibration register or using system calibration. This approach can also be used to reduce the ADC input range (LSB size).
[12] In ADC low power mode, the input range is fixed at ±2.34375 mV.
[13] Valid for a differential input less than 10 mV.
[14] The absolute value of the voltage of VTEMP and GND_SW must be 100mV minimum, for accurate operation of the T-ADC.
[15] Measured using box method.
[16] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.
[17] Die temperature.
[18] Endurance is qualified to 10,000 cycles, as per JEDEC Std. 22 Method A117 and measured at −40°C, +25°C, and +125°C. Typical endurance at 25°C is 170,000 cycles.
[19] Retention lifetime equivalent at junction temperature (T_J) = 85°C, as per JEDEC Std. 22 Method A117. Retention lifetime derates with junction temperature.
[20] These numbers are not production tested but are supported by LIN compliance testing.
[21] Thermal impedance can be used to calculate the thermal gradient from ambient to die temperature.
[22] Internal regulated supply available at REG_DVDD (I_{SOURCE} = 5 mA) and REG_AVDD (I_{SOURCE} =1 mA).
[23] Typical additional supply current consumed during Flash/EE memory program and erase cycles is 7 mA and 5 mA, respectively.

ABSOLUTE MAXIMUM RATINGS

T_A = −40°C to +115°C, unless otherwise noted.

Table 2.

Parameter	Rating
AGND to DGND to VSS to IO_VSS	−0.3 V to +0.3 V
VBAT to AGND	−22 V to +40 V
VDD to VSS	−0.3 V to +40 V
LIN to IO_VSS	−16 V to +40 V
LIN Short-Circuit Current[1]	200 mA
Digital I/O Voltage to DGND	−0.3 V to REG_DVDD + 0.3 V
ADC Inputs to AGND	−0.3 V to REG_AVDD + 0.3 V
ESD (HBM) Rating	
HBM-ADI0082 (Based on ANSI/ESD STM5.1-2007); All Pins Except LIN and VBAT	2.5 kV
LIN and VBAT	±6 kV
IEC61000-4-2 for LIN and VBAT	±7 kV
Storage Temperature	150°C
Junction Temperature	
Transient	150°C
Continuous	130°C
Lead Temperature	
Soldering Reflow (15 sec)	260°C

[1] 200 mA can be sustained on the LIN pin for 2 seconds. The active internal short circuit protection HVCFG[1] = 0 is required to be enabled on this device during LIN operation and is the default operation. This disconnects the LIN pin, if a short circuit event occurs, after the specified maximum period of 90 µs.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

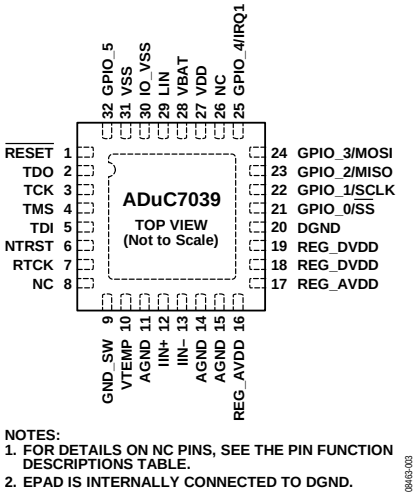

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	$\overline{\text{RESET}}$	I	Reset Input Pin. Active low. This pin has an internal, weak, pull-up resistor to REG_DVDD. When not in use, this pin can be left unconnected. For added security and robustness, it is recommended that this pin be strapped via a resistor to REG_DVDD.
2	TDO	O	JTAG Test Data Output. This data output pin is one of the standard 6-pin JTAG debug ports on the part. TDO is an output pin only. At power-on, this output is disabled and pulled high via an internal, weak, pull-up resistor. This pin can be left unconnected when not in use.
3	TCK	I	JTAG Test Clock. This clock input pin is one of the standard 6-pin JTAG debug ports on the part. TCK is an input pin only and has an internal, weak, pull-up resistor. This pin can be left unconnected when not in use.
4	TMS	I	JTAG Test Mode Select. This mode select input pin is one of the standard 6-pin JTAG debug ports on the part. TMS is an input pin only and has an internal, weak, pull-up resistor. This pin can be left unconnected when not in use.
5	TDI	I	JTAG Test Data Input. This data input pin is one of the standard 6-pin JTAG debug ports on the part. TDI is an input pin only and has an internal, weak, pull-up resistor. This pin can be left unconnected when not in use.
6	NTRST	I	JTAG Test Reset. This reset input pin is one of the standard 6-pin JTAG debug ports on the part. NTRST is an input pin only and has an internal, weak, pull-down resistor. This pin can be left unconnected when not in use. NTRST is also monitored by the on-chip kernel to enable LIN boot load mode.
7	RTCK	O	JTAG Return Test Clock. This output pin is used to adjust the JTAG clock speed to the highest possible rate of the ADuC7039.
8	NC		No Connect. This pin is internally connected; therefore, do not externally connect this pin.
9	GND_SW	I	Switch to Internal Analog Ground Reference. This pin is the negative input for the external temperature channel and external reference. If this input is not used, connect it directly to the AGND system ground.
10	VTEMP	I	External Pin for NTC/PTC Temperature Measurement.
11, 14, 15	AGND	S	Ground Reference for On-Chip Precision Analog Circuits.
12	IIN+	I	Positive Differential Input for Current Channel.
13	IIN–	I	Negative Differential Input for Current Channel.
16, 17	REG_AVDD	S	Nominal 2.6 V analog Output from On-Chip Regulator. Pin 16 and Pin 17 must be connected together to a capacitor to ground.
18, 19	REG_DVDD	S	Nominal 2.6 V digital Output from On-Chip Regulator. Pin 18 and Pin 19 must be connected together to capacitors to ground.
20	DGND	S	Ground Reference for On-Chip Digital Circuits.

Pin No.	Mnemonic	Type[1]	Description
21	GPIO_0/$\overline{SS}$	I/O	General-Purpose Digital I/O 0, or SPI Interface. By default, this pin is configured as an input. The pin has an internal, weak, pull-up resistor and, when not in use, can be left unconnected. This multifunction pin can be configured in one of two states, namely General-Purpose Digital I/O 0. SPI interface, slave select input.
22	GPIO_1/SCLK	I/O	General-Purpose Digital I/O 1 or SPI Interface. By default, this pin is configured as an input. The pin has an internal, weak, pull-up resistor and, when not in use, can be left unconnected. This multifunction pin can be configured in one of two states, namely General-Purpose Digital I/O 1. SPI interface, serial clock input.
23	GPIO_2/MISO	I/O	General-Purpose Digital I/O 2 or SPI Interface. By default, this pin is configured as an input. The pin has an internal, weak, pull-up resistor and, when not in use, can be left unconnected. This multifunction pin can be configured in one of two states, namely General-Purpose Digital I/O 2. SPI interface, master input/slave output pin.
24	GPIO_3/MOSI	I/O	General-Purpose Digital I/O 3 or SPI Interface. By default, this pin is configured as an input. The pin has an internal, weak, pull-up resistor and, when not in use, can be left unconnected. This multifunction pin can be configured in one of two states, namely General-Purpose Digital I/O 3. SPI interface, master output/slave input pin.
25	GPIO_4/IRQ1	I/O	General-Purpose I/O 4/External Interrupt Request 1. By default, this pin is configured as an input. The pin has an internal, weak, pull-up resistor and when not in use, can be left unconnected.
26	NC		No Connect. This pin is not internally connected, but is reserved for possible future use. Therefore, do not externally connect this pin.
27	VDD	S	Battery Power Supply to On-Chip Regulator.
28	VBAT	I	Battery Voltage Input to Resistor Divider.
29	LIN	I/O	LIN Serial Interface Input/Output Pin.
30	IO_VSS	S	Ground Reference for LIN Pin.
31	VSS	S	Ground Reference. This is the ground reference for the internal voltage regulators.
32	GPIO_5	I/O	General-Purpose I/O 5. By default, this pin is configured as an input. The pin has an internal, weak, pull-up resistor and when not in use, can be left unconnected.
EPAD	EPAD		The exposed pad is internally connected to DGND.

[1] I = input, O = output, S = supply.

MEMORY ORGANIZATION

The ARM7, a von Neumann architecture, MCU core sees memory as a linear array of 2^{32} byte locations. As shown in Figure 5, the ADuC7039 maps this into four distinct user areas, namely: a memory area that can be remapped, an SRAM area, a Flash/EE area, and a memory mapped register (MMR) area.

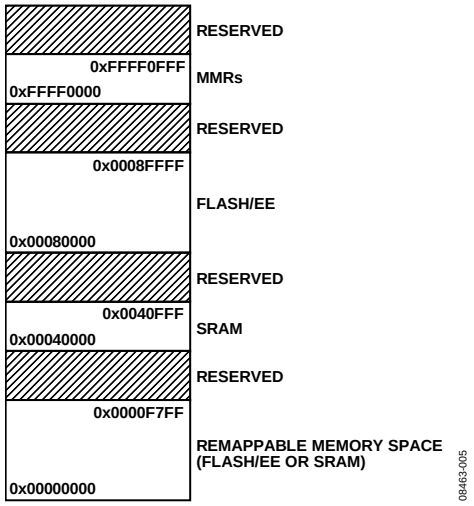

Figure 5. ADuC7039 Memory Map, 64 kB Flash Option

- The first 64 kB of this memory space is used as an area into which the on-chip Flash/EE or SRAM can be remapped.
- The ADuC7039 features a second 4 kB area at the top of the memory map used to locate the MMRs, through which all on-chip peripherals are configured and monitored.
- The ADuC7039 features an SRAM size of 4 kB.
- The ADuC7039 features 64 kB of on-chip Flash/EE memory. However, 62 kB of on-chip Flash/EE memory are available to the user. In addition, 2 kB are reserved for the on-chip kernel.

Any access, either reading or writing, to an area not defined in the memory map results in a data abort exception.

Memory Format

The ADuC7039 memory organization is configured in little endian format: the least significant byte is located in the lowest byte address, and the most significant byte in the highest byte address.

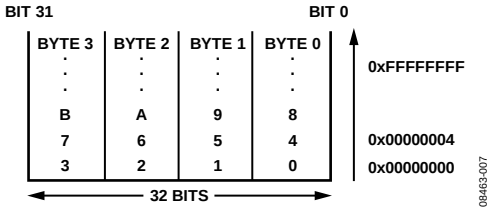

Figure 6. Little Endian Format

SRAM

The ADuC7039 features 4 kB of SRAM, organized as 1024 × 32 bits, that is, 1024 words, which is located at 0x40000.

The RAM space can be used as data memory and also as a volatile program space.

ARM code can run directly from SRAM at full clock speed given that the SRAM array is configured as a 32-bit wide memory array. SRAM is read/writeable in 8-, 16-, and 32-bit segments.

Remap

The ARM exception vectors are all situated at the bottom of the memory array, from Address 0x00000000 to Address 0x00000020.

By default, after a reset, the Flash/EE memory is logically mapped to Address 0x00000000. It is possible to logically remap the SRAM to Address 0x00000000. This is accomplished by setting Bit 0 of the SYSMAP MMR located at 0xFFFF0220. To revert Flash/EE to 0x00000000, Bit 0 of SYSMAP is cleared.

It is sometimes desirable to remap RAM to 0x00000000 to execute code from SRAM while erasing a page of Flash/EE memory.

Remap Operation

When a reset occurs on the ADuC7039, execution starts automatically in the factory programmed internal configuration code. This so-called kernel is hidden and cannot be accessed by user code. If the ADuC7039 is in normal mode, it executes the power-on configuration routine of the kernel and then jumps to the reset vector, Address 0x00000000, to execute the user's reset exception routine. Because the Flash/EE is mirrored at the bottom of the memory array at reset, the reset routine must always be written in Flash/EE.

FEEMOD Register

Name: FEEMOD

Address: 0xFFFF0E04

Default Value: 0x0000

Access: Read/write

Function: This register is written by user code to configure the mode of operation of the Flash/EE memory controller.

Table 12. FEEMOD MMR Bit Designation

Bit	Description
15 to 7	Not used. These bits are reserved for future functionality and should be written as 0 by user code.
6 to 5	Flash/EE security lock bits. These bits must be written as [6:5] = 1, 0 to complete the Flash/EE security protect sequence.
4	Flash/EE controller command complete interrupt enable. This bit is set by user code to enable the Flash/EE controller to generate an interrupt upon completion of a Flash/EE command. This bit is cleared by user code to disable the generation of a Flash/EE interrupt upon completion of a Flash/EE command.
3	Flash/EE erase/write enable. This bit is set by user code to enable the Flash/EE erase and write access via FEECON. This bit is cleared by user code to disable the Flash/EE erase and write access via FEECON.
2	Reserved.
1	Flash/EE controller abort enable. This bit is set by user code to enable the Flash/EE controller abort functionality. This bit is cleared by user code to disable the Flash/EE controller abort functionality.
0	Reserved.

FEEADR Registers

Name: FEEADR

Address: 0xFFFF0E10

Default Value: Updated by kernel

Access: Read/write

Function: This 16-bit register dictates the address upon which any Flash/EE command executed via FEECON acts.

FEEDAT Registers

Name: FEEDAT

Address: 0xFFFF0E0C

Default Value: 0x0000

Access: Read/write

Function: This 16-bit register contains the data either read from, or to be written to, the Flash/EE memory.

COMPLETE MMR LISTING

In the following MMR tables, addresses are listed in hex code. Access types include R for read, W for write, and RW for read and write.

Table 14. IRQ Address Base = 0xFFFF0000

Address	Name	Byte	Access Type	Default Value	Description
0x0000	IRQSTA	4	R	0x00000000	Active IRQ source.
0x0004	IRQSIG	4	R	0x00003080	Current state of all IRQ sources (enabled and disabled).
0x0008	IRQEN	4	RW	0x00000000	Enabled IRQ sources.
0x000C	IRQCLR	4	W	N/A	MMR to disable IRQ sources.
0x0010	SWICFG	4	W	N/A	Software interrupt configuration MMR.
0x0100	FIQSTA	4	R	0x00000000	Active IRQ source.
0x0104	FIQSIG	4	R	0x00003081	Current state of all IRQ sources (enabled and disabled).
0x0108	FIQEN	4	RW	0x00000000	Enabled IRQ sources.
0x010C	FIQCLR	4	W	N/A	MMR to disable IRQ sources.

Table 15. System Control Address Base = 0xFFFF0200

Address	Name	Byte	Access Type	Default Value	Description
0x0220	SYSMAP	1	RW	N/A	REMAP control register.
0x0230	RSTSTA	1	RW	N/A	Reset status MMR.
0x0234	RSTCLR	1	W	N/A	RSTSTA clear MMR.
0x0244	SYSCHK[1]	4	RW	N/A	Kernel checksum. See the System Kernel Checksum section.

[1] Updated by kernel.

Table 16. Timer Address Base = 0xFFFF0300

Address	Name	Byte	Access Type	Default Value	Description
0x0300	T0LD	2	RW	0x0000	Timer0 load register.
0x0304	T0VAL	2	R	0x0000	Timer0 Value Register 0.
0x0308	T0CON	4	RW	0x0000	Timer0 control MMR.
0x030C	T0CLRI	1	W	N/A	Timer0 interrupt clear register.
0x0320	T1LD	4	RW	0x00000000	Timer1 load register.
0x0324	T1VAL	4	R	0xFFFFFFFF	Timer1 value register.
0x0328	T1CON	4	RW	0x0000	Timer1 control MMR.
0x032C	T1CLRI	1	W	N/A	Timer1 interrupt clear register.
0x0340	T2LD[1]	4	RW	0x0050	Timer2 load register.
0x0344	T2VAL	4	R	0x00000050	Timer2 value register.
0x0348	T2CON	2	RW	0x0000	Timer2 control MMR.
0x034C	T2CLRI	1	W	N/A	Timer2 interrupt clear register.

[1] Updated by kernel.

ADC Filter Register

Name: ADCFLT

Address: 0xFFFF0518

Default Value: 0x0007

Access: Read/write

Function: The ADC filter MMR is a 16-bit register that controls the speed and resolution of the on-chip ADCs.

Note: If ADCFLT is modified, the current and voltage/temperature ADCs are reset. It is recommended that all bits of this MMR are written in a single write operation.

Table 31. ADCFLT MMR Bit Designations

Bit	Description
15	Chop enable. This bit is set by the user to enable system chopping of all active ADCs. When this bit is set, the ADC has very low offset errors and drift, but the ADC output rate is reduced by a factor of three if AF = 0 (see sinc3 decimation factor, Bits[6:0] in this table). If AF > 0, then the ADC output update rate is the same with chop on or off. When chop is enabled, the settling time is two output periods.
14	Running average. This bit is set by the user to enable a running-average-by-two function reducing ADC noise. This function is automatically enabled when chopping is active. It is an optional feature when chopping is inactive, and if enabled (when chopping is inactive) does not reduce the ADC output rate but does increase the settling time by one conversion period. This bit is cleared by the user to disable the running average function.
13 to 8	Averaging factor (AF). The values written to these bits are used to implement a programmable first-order sinc3 postfilter. The averaging factor can further reduce ADC noise at the expense of the output rate as described in Bits[6:0] sinc3 decimation factor in this table.
7	Sinc3 modify. This bit is set by the user to modify the standard sinc3 frequency response to increase the filter stop-band rejection by approximately 5 dB. This is achieved by inserting a second notch (NOTCH2) at $f_{NOTCH2} = 1.333 \times f_{NOTCH}$ where f_{NOTCH} is the location of the first notch in the response.
6 to 0	Sinc3 decimation factor (SF)[1]. The value (SF) written in these bits controls the oversampling (decimation factor) of the sinc3 filter. The output rate from the sinc3 filter is given by $f_{ADC} = (512{,}000/([SF + 1] \times 64))$ Hz when the chop bit (Bit 15, chop enable) = 0 and the averaging factor (AF) = 0. This is valid for all SF values ≤ 125. For SF = 126, f_{ADC} is forced to 60 Hz. For SF = 127, f_{ADC} is forced to 50 Hz. For information on calculating the f_{ADC} for SF (other than 126 and 127) and AF values, refer to Table 32.

[1] Due to limitations on the digital filter internal data path, there are some limitations on the combinations of the sinc3 decimation factor (SF) and averaging factor (AF) that can be used to generate a required ADC output rate. This restriction limits the minimum ADC update to 10 Hz.

Understanding the Offset and Gain Calibration Registers

The output of the average block in the ADC signal flow can be considered a fractional number with a span for a ±full-scale input of approximately ±0.75. The span is less than ±1.0 because there is attenuation in the modulator to accommodate some overrange capacity on the input signal. The exact value of the attenuation varies slightly from part-to-part because of manufacturing tolerances.

The offset coefficient is read from the ADC0OF calibration register. This value is a 16-bit, twos complement number. The range of this number, in terms of the signal chain, is effectively ±1.0. Therefore, 1 LSB of the ADC0OF register is not the same as 1 LSB of ADC0DAT.

A positive value of ADC0OF indicates that when offset is subtracted from the output of the filter, a negative value is added. The nominal value of this register is 0x0000, indicating zero offset is to be removed. The actual offset of the ADC can vary slightly from part-to-part and at different PGA gains. The offset within the ADC is minimized if the chopping mode is active (ADCFLT[15] = 1).

The gain coefficient is a unitless scaling factor. The 16-bit value in this register is divided by 16,384 and then multiplied by the offset corrected value. The nominal value of this register equals 0x5555, corresponding to a multiplication factor of 1.3333. This scales the nominal ±0.75 signal to produce a full-scale output signal of ±1.0 which is checked for overflow/underflow and converted to twos complement or unipolar mode, as appropriate, before being output to the data register.

The actual gain, and the required scaling coefficient for zero gain error, varies slightly from part to part and at different PGA settings. The value downloaded into ADC0GN at power-on-reset represents the scaling factor for a PGA gain = 4. There is some level of gain error if this value is used at different PGA settings. User code can run ADC calibrations and overwrite the calibration coefficients to correct the gain error at the current PGA setting.

In summary, the simplified ADC transfer function can be described as

$$ADC_{OUT} = \left[\frac{V_{IN} \times PGA}{V_{REF}} - ADCOF\right] \times \frac{ADCGN}{ADCGN_{NOM}}$$

This equation is valid for the voltage/temperature channel ADC.

For the current channel ADC,

$$ADC_{OUT} = \left[\frac{V_{IN} \times PGA}{V_{REF}} - K \times ADCOF\right] \times \frac{ADCGN}{ADCGN_{NOM}}$$

where *K* is dependent on the PGA gain setting and ADC mode.

For PGA gains of 4 and 32, the K factor is 1. For a PGA gain of 512, the K factor is 8.

ADC CONFIGURATION

Fast Temperature Conversion Mode

The battery temperature can be derived through the on-chip temperature sensor. By default, the time to a first valid (fully settled) result after switching the ADC input from the voltage to the temperature channel or from the temperature to the voltage channel is three ADC conversion cycles with chop mode turned off as shown in Figure 17.

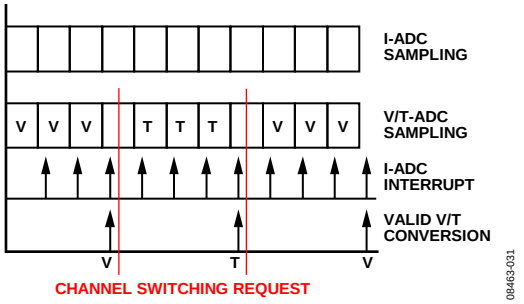

Figure 17. Default Temperature Mode, Chop Off

A fast mode is provided on the temperature channel to minimize the switching delay between voltage conversion and temperature conversions as shown in Figure 18 and in Table 36.

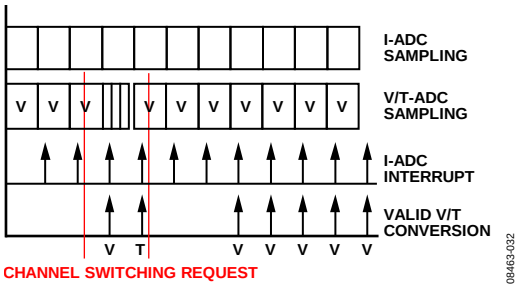

Figure 18. Fast Temperature Mode, Chop Off (ADCFLT = 0x07)

A request for a fast temperature conversion is executed with a delay of one ADC conversion. The fast temperature mode must be cleared after the temperature measurement is available but before a new temperature request.

Table 36. Fast Temperature Mode

Interrupt	Valid Flags	User code
1	I and V	Voltage = ADC1DAT.
2	I and V	Voltage = ADC1DAT. Set fast temperature request bit.
3	I and V	Voltage = ADC1DAT. This data must be read for the next temperature channel flag to be valid.
4	I and T	Temperature = ADC1DAT. Clear fast temperature request bit.
5	I	
6	I	
7	I and V	Voltage = ADC1DAT.
8	I and V	Voltage = ADC1DAT.

The operating mode and clocking mode are controlled using two MMRs, PLLCON and POWCON, and the status of the PLL, PLL lock and PLL interrupt, is indicated by PLLSTA.

It is recommended that before powering down the ADuC7039, switch the clock source for the PLL to the low power oscillator to reduce wake-up time. The low power oscillator is always active.

When the ADuC7039 wakes up from power-down, the MCU core begins executing code as soon as the PLL begins oscillating. This occurs before the PLL has locked to a frequency of 20.48 MHz. To ensure the Flash/EE memory controller is executing with a valid clock, the controller is driven with a PLL output divide-by-eight clock source while the PLL is locking. When the PLL locks, the PLL output is switched from the PLL output divide-by-eight to the locked PLL output.

If user code requires an accurate PLL output, user code must poll the lock bit (PLLSTA[1]) after wake-up before resuming normal code execution.

The PLL is locked within 2 ms after waking up.

PLLCON is a protected MMR with two 32-bit keys: PLLKEY0 (prewrite key) and PLLKEY1 (postwrite key).

PLLKEY0 = 0x000000AA

PLLKEY1 = 0x00000055

POWCON is a protected MMR with two 32-bit keys: POWKEY0 (prewrite key) and POWKEY1 (postwrite key).

POWKEY0 = 0x00000001

POWKEY1 = 0x000000F4

Sequence Example

An example of writing to both MMRs is as follows:

For programming the POWCON MMR:

//Function Prototype

```
Void PowerDown (void)


PowerDown PROC
  LDR    r2, = 0x98765432       ; Load random number for multiplication
  LDR    r3, = 0x12345678
  LDR    r0, = 0xffff0400       ;Base address
  MOVS   r1,#0x1                ;POWKEY0 = 1
  STR    r1,[r0,#4]             ;Set POWKEY0
  MOVS   r1,#0x01               ;Set POWCON value to recommended value of 0x01 to ensure a
                                 10 MHz core clock
  STR    r1,[r0,#8]
  MOVS   r1,#0xf4
  STR    r1,[r0,#0xc]           ;Set POWKEY1
  UMLAL  r1,r3,r2,r0            ;longest possible assembly multiplication instruction
  BX     lr                     ;Flush ARM7 pipeline
ENDP
```

For programming the PLLCON MMR:

```
PLLKEY0      =     0xAA   //PLLCON key
PLLCON       =     0x1    //Switch to precision oscillator.
PLLKEY1      =     0x55   //PLLCON key
iA1*iA2                   //PSEUDOCODE-dummy cycle to prevent Flash/EE access during clock
change
```

PLLSTA Register

Name: PLLSTA

Address: 0xFFFF0400

Default Value: 0xXX

Access: Read only

Function: This 8-bit register allows user code to monitor the lock state of the PLL.

Table 37. PLLSTA MMR Bit Designations

Bit	Description
7 to 2	Reserved.
1	PLL lock status bit, read only. This bit is set automatically when the PLL is locked and outputting 20.48 MHz. This bit is cleared automatically when the PLL is not locked and outputting an f_{CORE} divide-by-8 clock source.
0	PLL interrupt. Set this bit if the PLL lock status bit signal goes low. This bit is cleared by user code when writing 1 to this bit.

PLLCON Prewrite Key PLLKEY0

Name: PLLKEY0

Address: 0xFFFF0410

Access: Write only

Key: 0x000000AA

Function: PLLCON is a keyed register that requires a 32-bit key value to be written before and after PLLCON. PLLKEY0 is the prewrite key.

PLLCON Postwrite Key PLLKEY1

Name: PLLKEY1

Address: 0xFFFF0418

Access: Write only

Key: 0x00000055

Function: PLLCON is a keyed register that requires a 32-bit key value to be written before and after PLLCON. PLLKEY1 is the postwrite key.

PLLCON Register

Name: PLLCON

Address: 0xFFFF0414

Default Value: 0x00

Access: Read/write

Function: This 8-bit register allows user code to dynamically select the PLL source clock from two different oscillator sources.

Table 39. POWCON MMR Bit Designations

Bit	Description
11 to 9	Reserved. These bits should be written as 0.
8	Precision oscillator enable. This bit is set by the user to enable the precision oscillator. This bit is cleared by the user to power down the precision oscillator.
7 to 6	Reserved. These bits should be written as 0.
5	PLL power-down. Timer peripherals power down if driven from the PLL output clock. Timers driven from an active clock source remain active. This bit is set by default, and set by hardware on a wake-up event. This bit is cleared to 0 to power down the PLL. The PLL should not be powered down if either the core or peripherals are enabled: Bit 3, Bit 4, and Bit 5 must be cleared simultaneously.
4	Peripherals power-down. The peripherals that are powered down by this bit are as follows: SRAM, Flash/EE memory and GPIO interfaces, and SPI port. This bit is set by default, and/or by hardware, on a wake-up event. Wake-up timer (Timer2) can still be active if driven from low power oscillator even if this bit is set. This bit is cleared to power down the peripherals. The peripherals cannot be powered down if the core is enabled: Bit 3 and Bit 4 must be cleared simultaneously. LIN can still respond to wake-up events even if this bit is cleared.
3	Core power-down. If user code powers down the MCU, include a dummy MCU cycle after the power-down command is written to POWCON. This bit is set by default, and set by hardware on a wake-up event. This bit is cleared to power down the ARM core.
2 to 0	Core clock divider (CD) bits. 000 = 20.48 MHz, 48.83 ns. 001 = 10.24 MHz, 97.66 ns (this is the default setting at power-up). 010 = 5.12 MHz, 195.31 ns. 011 = 2.56 MHz, 390.63 ns. 100 = 1.28 MHz, 781.25 ns. 101 = 640 kHz, 1.56 µs. 110 = 320 kHz, 3.125 µs. 111 = 160 kHz, 6.25 µs.

LOCUSR0 Register

Name: LOCUSR0

Address: 0xFFFF0484

Default Value: Updated by kernel

Access: Read/write (key protected)

Function: User trim register for the low power oscillator.

LOCUSR1 Register

Name: LOCUSR1

Address: 0xFFFF0488

Default Value: Updated by kernel

Access: Read/write (key protected)

Function: User trim register for the precision oscillator.

LOCMAX Register

Name: LOCMAX

Address: 0xFFFF048C

Default Value: 0x00000

Access: Read/write

Function: Maximum limit expectable in the LINBR for a predefined baud rate.

LOCMIN Register

Name: LOCMIN

Address: 0xFFFF0490

Default Value: 0x00000

Access: Read/write

Function: Minimum limit expectable in the LINBR for a predefined baud rate.

LOCSTA Register

Name: LOCSTA

Address: 0xFFFF0494

Default Value: 0x01

Access: Read only

Function: Calibration status register.

Table 43. LOCSTA MMR Bit Designations

Bit	Description
7 to 3	Reserved. Read 0.
2	Low power oscillator trim value modified. This bit is set by hardware when the precision oscillator trim value is altered. This bit is cleared by hardware on a read of LOCSTA MMR.
1	Precision oscillator trim value modified. This bit is set by hardware when the precision oscillator trim value is altered. This bit is cleared by hardware on a read of LOCSTA MMR.
0	Oscillator selected. This bit is set by hardware to indicate that the low power oscillator is selected for calibration. This bit is cleared by hardware to indicate that the precision oscillator is selected for calibration.

LOCVAL0 Register

Name: LOCVAL0

Address: 0xFFFF0498

Default Value: Updated by kernel

Access: Read only

Function: Current low power oscillator trim value, read-only.

LOCVAL1 Register

Name: LOCVAL1

Address: 0xFFFF049C

Default Value: Updated by kernel

Access: Read only

Function: Current precision oscillator trim value, read-only.

LOCKEY Register

Name: LOCKEY

Address: 0xFFFF04A0

Access: Write only

Function: Must be written to unlock any of the writable calibration register. The value to write to this MMR is 0x1324.

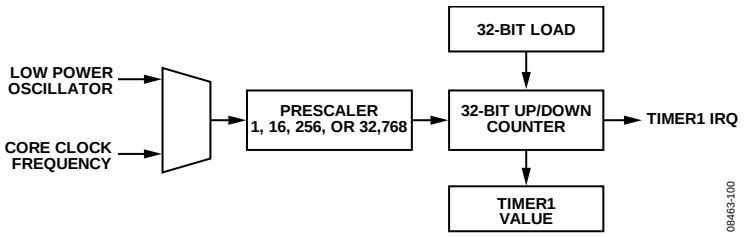

Figure 26. Timer1 Block Diagram

Table 47. T1CON MMR Bit Designations

Bit	Description
15 to 6	Reserved. These bits should be written as 0.
5	Timer1 mode. This bit is set by user code to operate in periodic mode. This bit is cleared by user code to operate in free running mode (default).
4	Count up. This bit is set by user code for Timer1 to count up. This bit is cleared by user code for Timer1 to count down (default).
3	Timer1 enable bit. This bit is set by user code to enable Timer1. This bit is cleared by user code to disable Timer1 (default).
2	Clock select. 0 = core clock (default). 1 = low power (32.768 kHz) oscillator.
1 to 0	Prescaler. 00 = source clock/1 (default). 01 = source clock/16. 10 = source clock/256. 11 = source clock/32,768.

SPI Control Register

Name: SPICON

Address: 0xFFFF0A10

Default Value: 0x0000

Access: Read/write

Function: This 16-bit MMR configures the SPI peripheral in both master and slave modes.

Table 55. SPICON MMR Bit Designations

Bit	Description
15 to 14	SPI IRQ mode bits. These bits configure when the Tx/Rx interrupts occur in a transfer. 00 = Tx interrupt occurs when 1 byte has been transferred. Rx interrupt occurs when 1 or more bytes have been received into the FIFO. 01 = Tx interrupt occurs when 2 bytes have been transferred. Rx interrupt occurs when 1 or more bytes have been received into the FIFO. 10 = Tx interrupt occurs when 3 bytes have been transferred. Rx interrupt occurs when 3 or more bytes have been received into the FIFO. 11 = Tx interrupt occurs when 4 bytes have been transferred. Rx interrupt occurs when the Rx FIFO is full, or 4 bytes are present.
13	SPI Tx FIFO flush enable bit. Set this bit to flush the Tx FIFO. This bit does not clear itself and should be toggled if a single flush is required. If this bit is left high, then either the last transmitted value or 0x00 is transmitted depending on SPICON[7]. Any writes to the Tx FIFO are ignored while this bit is set. Clear this bit to disable Tx FIFO flushing.
12	SPI Rx FIFO flush enable bit. Set this bit to flush the Rx FIFO. This bit does not clear itself and should be toggled if a single flush is required. If this bit is set, all incoming data is ignored and no interrupts are generated. If set and SPICON[6] = 0, a read of the Rx FIFO initiates a transfer. Clear this bit to disable Rx FIFO flushing.
11	Continuous transfer enable. This bit is set by the user to enable continuous transfer. In master mode, the transfer continues until no valid data is available in the SPITX register. $\overline{SS}$ is asserted and remains asserted for the duration of each 8-bit serial transfer until TX is empty. This bit is cleared by the user to disable continuous transfer. Each transfer consists of a single 8-bit serial transfer. If valid data exists in the SPITX register, then a new transfer is initiated after a stall period of 1 serial clock cycle.
10	Loop back enable bit. This bit is set by the user to connect MISO to MOSI and test software. This bit is cleared by the user to be in normal mode.
9	Slave MISO output enable bit. Set this bit to disable the output driver on the MISO pin. The MISO pin becomes open drain when this bit is set. Clear this bit for MISO to operate as normal.
8	SPIRX overflow overwrite enable. This bit is set by the user; the valid data in the SPIRX register is overwritten by the new serial byte received. This bit is cleared by the user; the new serial byte received is discarded.
7	SPI transmit zeros when Tx FIFO enable bit. Set this bit to transmit 0x00 when there is no valid data in the Tx FIFO. Clear this bit to transmit the last transmitted value when there is no valid data in the Tx FIFO.
6	SPI transfer and interrupt mode. This bit is set by the user to initiate a transfer with a write to the SPITX register. Interrupt only occurs when SPITX is empty. This bit is cleared by the user to initiate a transfer with a read of the SPIRX register. Interrupt only occurs when SPIRX is full.
5	LSB first transfer enable bit. This bit is set by the user; the LSB is transmitted first. This bit is cleared by the user; the MSB is transmitted first.

Bit	Description
4	SPI wired or mode enable bit. This bit is set to 1 to enable open-drain data output enable. External pull-ups are required on data out pins. Clear this bit for normal output levels.
3	Serial clock polarity mode bit. This bit is set by the user; the serial clock idles high. This bit is cleared by the user; the serial clock idles low.
2	Serial clock phase mode bit. This bit is set by the user; the serial clock pulses at the beginning of each serial bit transfer. This bit is cleared by the user; the serial clock pulses at the end of each serial bit transfer.
1	Master mode enable bit. This bit is set by the user to enable master mode. This bit is cleared by the user to enable slave mode.
0	SPI enable bit. This bit is set by the user to enable the SPI. This bit is cleared by the user to disable the SPI.

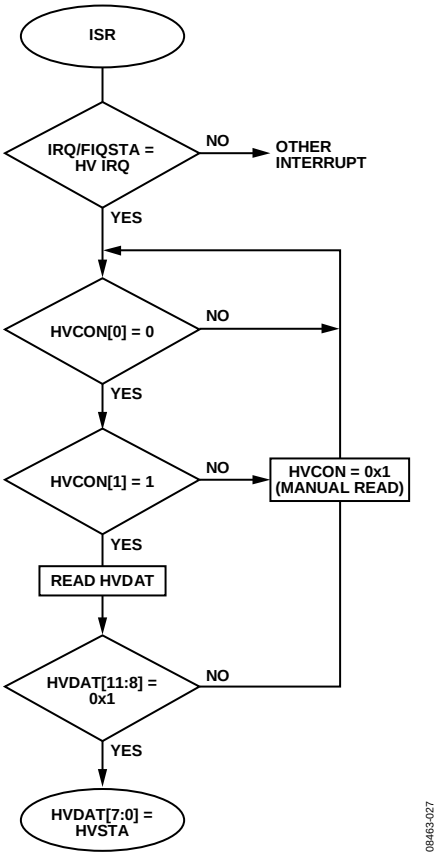

Figure 30. High Voltage Interface Interrupt Flow Chart

HV Configuration

Following is a code example to enable LIN.

```
char HVstatus;
      do{                              // Enable LIN
            HVDAT = 0x01;              // Enable LIN physical layer mode
            HVCON = 0x08;              // Write to HVCFG
            do{
                  HVstatus = HVCON;
            }
            while(HVstatus & 0x1);     // Wait until command is finished
      }
      while (!(HVstatus & 0x4));       // Transmit command is correct
```

It is best practice to implement the high voltage communication routine in a function and call this function throughout the code.

LIN DIAGNOSTIC

The ADuC7039 features a short-circuit protection on the LIN pin. If a short-circuit condition is detected on the LIN pin, HVSTA[0] is set. This generates a high voltage interrupt if enabled in IRQEN[10]. This bit is cleared by re-enabling the LIN driver using HVCFG[2]. It is possible to disable this feature through HVCFG[1].

LIN COMMUNICATION

LIN uses frames for data communication. A frame consists of a header, break, synch, PID issued by the master, and data bytes, plus checksum generated by a slave as shown in Figure 32. In a LIN communication, the PID dictates the behavior of the slave: receive, transmit, or ignore.

Break

The LIN interface of the ADuC7039 automatically detects the break and sets a flag in the LINSTA register after receiving a valid break. The minimum length of the break symbol is 11 nominal slave clocks (at 20 kB). The maximum length of a valid break symbol is programmable and can be configured in the LINBK MMR. The LIN interface recognizes a valid break at any time during a LIN communication and flags a collision (Bit 4 of LINSTA) if the break occurred during an existing communication.

Synch

The LIN interface automatically detects the synch byte and sets the baud rate for the subsequent data of the current LIN frame. This operation is transparent to the user.

PID

The LIN peripheral sees the PID as a data byte. It is available in the LINDAT MMR. The software must decode the PID. After reception of the PID stop bit, an interrupt is generated to read the contents of the LINDAT register before the contents are overwritten by the next data byte.

Data Bytes

Subsequent data bytes similarly set the interrupt bit to indicate that a data byte has been received.

In transmit mode, up to 8 data bytes can be transmitted at a time followed by a checksum.

Checksum

Checksums are automatically calculated as each byte is received or transmitted with the inverted value being stored in the LINCS MMR. By default, checksum calculation are per LIN 2.1 specifications, that is, with enhanced checksum calculations for all frames except the diagnostic frames and reserved frames where the classic checksum calculation is used. The hardware automatically recognizes the PID and calculates the checksum accordingly. There is no requirement for user code to write to the LINCON register to change the checksum calculation.

To operate in LIN 1.3 mode, user code LIN initialization routine must set LINCON[7] to 1, to force the hardware in classic checksum calculation. This register should not be modified during LIN communication in receive mode.

LIN MMRS

The interface to the LIN block consists of 8 MMRs:

- LINCON is a 16-bit control register. This MMR is described in Table 61. This register should not be accessed during data reception.
- LINDAT is an 8-bit user accessible data register. This MMR is double-buffered: a shadow register is used to receive and transmit while user code reads and writes from/to LINDAT. The LINSTA MMR indicates the status of the data.
- LINSTA is a 16-bit status register. This MMR is described in Table 62.
- LINBR is a 19-bit baud rate register. The baud rate is automatically set by the LIN peripheral and this register should not be altered by user code. It indicates the number of core clock ticks during an 8-bit transmission.
- LINBK is a 19-bit break timer register controlling the maximum length of a break symbol to be detected by the LIN slave interface as valid. The default count is 5500 core clock ticks. This represents the time taken for 11 bits to be transmitted at 20 kHz.
- LINCS is an 8-bit checksum register. It contains the inverted result of the current checksum calculation. The checksum calculation is performed on every byte that is received or transmitted according to the setting of Bit 4 in LINCON MMR. In transmit mode, the user sets the bit after the last data to transmit has been written in the peripheral. The checksum is sent automatically. In receive mode, the checksum is calculated on receiving each byte, regardless if this byte is a data byte or the frame checksum. For example, when receiving a frame with 4 data bytes, the LINCS MMR contains the expected frame checksum once the fourth data byte is received. LINCS should contain 0x00 after receiving a correct checksum.
- LINLOW is a 19-bit counter clocked at 10 MHz to wake up the LIN nodes on the bus. The LIN bus is forced low as long as the LINLOW MMR is greater than 0. For example, LINLOW = 0x234 generates an 11-bit break at 20 kB.
- LINWU is a 19-bit counter clocked by the low power oscillator. It is used in sleep mode to specify the length of the low signal that wakes up the device via LIN. For example, LINWU = 0x13 ignores any breaks of less than 150 μs, and the ADuC7039 remains asleep.

System Identification FEEADR

Name: FEEADR

Address: 0xFFFF0E10

Default Value: 0xF009

Access: Read/write

Function: This 16-bit register dictates the address upon which any Flash/EE command executed via FEECON acts.

Note: This MMR is also used to identify ADuC703x family member and prerelease silicon revision.

Table 67. FEEADR System Identification MMR Bit Designations

Bit	Description
15 to 4	Reserved
3 to 0	ADuC703x family ID 0x0 = ADuC7030 0x2 = ADuC7032 0x3 = ADuC7033 0x4 = ADuC7034 0x6 = ADuC7036 0x9 = ADuC7039 Others = reserved for future use