



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	16MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	69
Program Memory Size	96KB (32K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj96ga008t-i-pt

PIC24FJ128GA010 FAMILY

Table of Contents

1.0	Device Overview	7
2.0	Guidelines for Getting Started with 16-bit Microcontrollers	19
3.0	CPU	25
4.0	Memory Organization	31
5.0	Flash Program Memory	51
6.0	Resets	57
7.0	Interrupt Controller	63
8.0	Oscillator Configuration	97
9.0	Power-Saving Features	105
10.0	I/O Ports	107
11.0	Timer1	111
12.0	Timer2/3 and Timer4/5	113
13.0	Input Capture	119
14.0	Output Compare	121
15.0	Serial Peripheral Interface (SPI)	127
16.0	Inter-Integrated Circuit (I ² C™)	137
17.0	Universal Asynchronous Receiver Transmitter (UART)	145
18.0	Parallel Master Port (PMP)	153
19.0	Real-Time Clock and Calendar (RTCC)	163
20.0	Programmable Cyclic Redundancy Check (CRC) Generator	175
21.0	10-bit High-Speed A/D Converter	179
22.0	Comparator Module	189
23.0	Comparator Voltage Reference	193
24.0	Special Features	195
25.0	Instruction Set Summary	205
26.0	Development Support	213
27.0	Electrical Characteristics	217
28.0	Packaging Information	231
	Appendix A: Revision History	245
	Index	247
	The Microchip Web Site	251
	Customer Change Notification Service	251
	Customer Support	251
	Reader Response	252
	Product Identification System	253

PIC24FJ128GA010 FAMILY

TABLE 1-2: PIC24FJ128GA010 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin	80-Pin	100-Pin			
$\overline{\text{U1CTS}}$	43	37	47	I	ST	UART1 Clear-to-Send Input.
$\overline{\text{U1RTS}}$	35	38	48	O	—	UART1 Request-to-Send Output.
U1RX	34	42	52	I	ST	UART1 Receive.
U1TX	33	41	51	O	DIG	UART1 Transmit Output.
$\overline{\text{U2CTS}}$	21	27	40	I	ST	UART2 Clear-to-Send Input.
$\overline{\text{U2RTS}}$	29	35	39	O	—	UART2 Request-to-Send Output.
U2RX	31	39	49	I	ST	UART 2 Receive Input.
U2TX	32	40	50	O	—	UART2 Transmit Output.
VDD	10, 26, 38	12, 32, 48	2, 16, 37, 46, 62	P	—	Positive Supply for Peripheral Digital Logic and I/O Pins.
VDDCAP	56	70	85	P	—	External Filter Capacitor Connection (regulator is enabled).
VDDCORE	56	70	85	P	—	Positive Supply for Microcontroller Core Logic (regulator is disabled).
VREF-	15	23	28	I	ANA	A/D and Comparator Reference Voltage (Low) Input.
VREF+	16	24	29	I	ANA	A/D and Comparator Reference Voltage (High) Input.
VSS	9, 25, 41	11, 31, 51	15, 36, 45, 65, 75	P	—	Ground Reference for Logic and I/O Pins.

Legend: TTL = TTL input buffer, ST = Schmitt Trigger input buffer, ANA = Analog level input/output, I²C™ = I²C/SMBus input buffer

PIC24FJ128GA010 FAMILY

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 μF (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μF in parallel with 0.001 μF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including microcontrollers to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF .

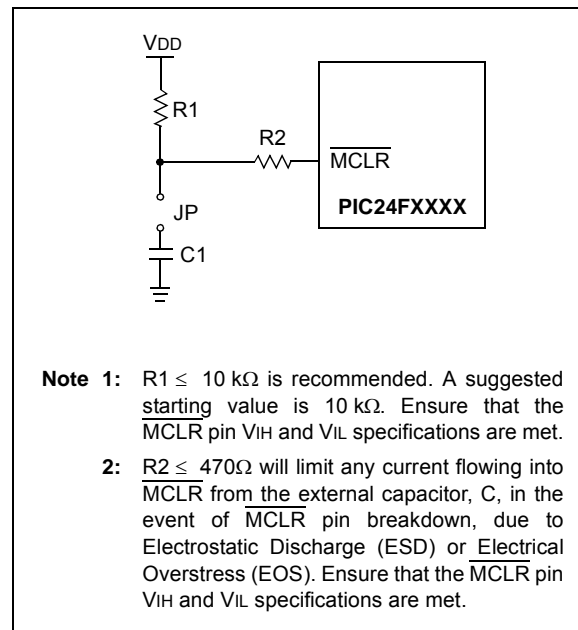
2.3 Master Clear ($\overline{\text{MCLR}}$) Pin

The $\overline{\text{MCLR}}$ pin provides two specific device functions: device Reset, and device programming and debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the MCLR pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{\text{MCLR}}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF $\overline{\text{MCLR}}$ PIN CONNECTIONS



PIC24FJ128GA010 FAMILY

3.3 Arithmetic Logic Unit (ALU)

The PIC24F ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

The PIC24F CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.3.1 MULTIPLIER

The ALU contains a high-speed, 17-bit x 17-bit multiplier. It supports unsigned, signed or mixed sign operation in several multiplication modes:

1. 16-bit x 16-bit signed
2. 16-bit x 16-bit unsigned
3. 16-bit signed x 5-bit (literal) unsigned
4. 16-bit unsigned x 16-bit unsigned
5. 16-bit unsigned x 5-bit (literal) unsigned
6. 16-bit unsigned x 16-bit signed
7. 8-bit unsigned x 8-bit unsigned

3.3.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operation with the following data sizes:

1. 32-bit signed/16-bit signed divide
2. 32-bit unsigned/16-bit unsigned divide
3. 16-bit signed/16-bit signed divide
4. 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m+1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.3.3 MULTI-BIT SHIFT SUPPORT

The PIC24F ALU supports both single bit and single-cycle, multi-bit arithmetic and logic shifts. Multi-bit shifts are implemented using a shifter block, capable of performing up to a 15-bit arithmetic right shift, or up to a 15-bit left shift, in a single cycle. All multi-bit shift instructions only support Register Direct Addressing for both the operand source and result destination.

A full summary of instructions that use the shift operation is provided below in Table 3-2.

TABLE 3-2: INSTRUCTIONS THAT USE THE SINGLE AND MULTI-BIT SHIFT OPERATION

Instruction	Description
ASR	Arithmetic shift right source register by one or more bits.
SL	Shift left source register by one or more bits.
LSR	Logical shift right source register by one or more bits.

TABLE 4-5: ICN REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	—	—	—	—	—	—	—	—	—	CN21IE ⁽¹⁾	CN20IE ⁽¹⁾	CN19IE ⁽¹⁾	CN18IE	CN17IE	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	—	—	—	—	—	—	—	—	—	CN21PUE ⁽¹⁾	CN20PUE ⁽¹⁾	CN19PUE ⁽¹⁾	CN18PUE	CN17PUE	CN16PUE	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal

Note 1: Implemented in 80-pin and 100-pin devices only.

TABLE 4-6: TIMER REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																xxxx
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register																xxxx
TMR3HLD	0108	Timer3 Holding Register (For 32-bit timer operations only)																xxxx
TMR3	010A	Timer3 Register																xxxx
PR2	010C	Period Register 2																FFFF
PR3	010E	Period Register 3																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR4	0114	Timer4 Register																xxxx
TMR5HLD	0116	Timer5 Holding Register (For 32-bit operations only)																xxxx
TMR5	0118	Timer5 Register																xxxx
PR4	011A	Period Register 4																FFFF
PR5	011C	Period Register 5																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

PIC24FJ128GA010 FAMILY

REGISTER 5-1: NVMCON: FLASH MEMORY CONTROL REGISTER

R/SO-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	U-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0 ⁽¹⁾	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
—	ERASE	—	—	NVMOP3 ⁽²⁾	NVMOP2 ⁽²⁾	NVMOP1 ⁽²⁾	NVMOP0 ⁽²⁾
bit 7							bit 0

Legend:	SO = Settable Only bit
R = Readable bit	W = Writable bit
U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

- bit 15 **WR:** Write Control bit
 1 = Initiates a Flash memory program or erase operation. The operation is self-timed and the bit is cleared by hardware once operation is complete.
 0 = Program or erase operation is complete and inactive
- bit 14 **WREN:** Write Enable bit
 1 = Enables Flash program/erase operations
 0 = Inhibits Flash program/erase operations
- bit 13 **WRERR:** Write Sequence Error Flag bit
 1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
 0 = The program or erase operation completed normally
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **ERASE:** Erase/Program Enable bit
 1 = Performs the erase operation specified by NVMOP<3:0> on the next WR command
 0 = Performs the program operation specified by NVMOP<3:0> on the next WR command
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits⁽²⁾
 1111 = Memory bulk erase operation (ERASE = 1) or no operation (ERASE = 0)⁽³⁾
 0011 = Memory word program operation (ERASE = 0) or no operation (ERASE = 1)
 0010 = Memory page erase operation (ERASE = 1) or no operation (ERASE = 0)
 0001 = Memory row program operation (ERASE = 0) or no operation (ERASE = 1)

- Note 1:** These bits can only be reset on a POR.
2: All other combinations of NVMOP<3:0> are unimplemented.
3: Available in ICSP™ mode only. Refer to the device programming specifications.

PIC24FJ128GA010 FAMILY

REGISTER 7-13: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	RTCIE	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0
—	INT4IE	INT3IE	—	—	MI2C2IE	SI2C2IE	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14 **RTCIE:** Real-Time Clock/Calendar Interrupt Enable bit
 - 1 = Interrupt request is enabled
 - 0 = Interrupt request is not enabled
- bit 13-7 **Unimplemented:** Read as '0'
- bit 6 **INT4IE:** External Interrupt 4 Enable bit
 - 1 = Interrupt request is enabled
 - 0 = Interrupt request is not enabled
- bit 5 **INT3IE:** External Interrupt 3 Enable bit
 - 1 = Interrupt request is enabled
 - 0 = Interrupt request is not enabled
- bit 4-3 **Unimplemented:** Read as '0'
- bit 2 **MI2C2IE:** Master I2C2 Event Interrupt Enable bit
 - 1 = Interrupt request is enabled
 - 0 = Interrupt request is not enabled
- bit 1 **SI2C2IE:** Slave I2C2 Event Interrupt Enable bit
 - 1 = Interrupt request is enabled
 - 0 = Interrupt request is not enabled
- bit 0 **Unimplemented:** Read as '0'

PIC24FJ128GA010 FAMILY

REGISTER 7-27: IPC12: INTERRUPT PRIORITY CONTROL REGISTER 12

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	MI2C2IP2	MI2C2IP1	MI2C2IP0
bit 15						bit 8	

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	SI2C2IP2	SI2C2IP1	SI2C2IP0	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **MI2C2IP<2:0>:** Master I2C2 Event Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SI2C2IP<2:0>:** Slave I2C2 Event Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

PIC24FJ128GA010 FAMILY

10.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, each port pin can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired digital only pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

10.2 Configuring Analog Port Pins

The use of the AD1PCFG and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level).

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

10.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP.

10.2.2 ANALOG INPUT PINS AND VOLTAGE CONSIDERATIONS

The voltage tolerance of pins used as device inputs is dependent on the pin's input function. Pins that are used as digital only inputs are able to handle DC voltages up to 5.5V, a level typical for digital logic circuits. In contrast, pins that also have analog input functions of any kind can only tolerate voltages up to VDD. On these pins, voltage excursions beyond VDD are always to be avoided. Table 10-1 summarizes the input capabilities. Refer to **Section 27.1 “DC Characteristics”** for more details.

Note: For easy identification, the pin diagrams at the beginning of this data sheet also indicate 5.5V tolerant pins with dark grey shading.

TABLE 10-1: INPUT VOLTAGE LEVELS⁽¹⁾

Port or Pin	Tolerated Input	Description
PORTA<10:9>	VDD	Only VDD input levels are tolerated.
PORTB<15:0>		
PORTC<15:12>		
PORTA<15:14>	5.5V	Tolerates input levels above VDD, useful for most standard logic.
PORTA<7:0>		
PORTC<4:1>		
PORTD<15:0>		
PORTE<9:0>		
PORTF<13:12>		
PORTF<8:0>		
PORTG<15:12>		
PORTG<9:6>		
PORTG<3:0>		

Note 1: Not all port pins shown here are implemented on 64-pin and 80-pin devices. Refer to **Section 1.0 “Device Overview”** to confirm which ports are available in specific devices.

EXAMPLE 10-1: PORT WRITE/READ EXAMPLE

```
MOV    0xFF00, W0          ; Configure PORTB<15:8> as inputs
MOV    W0, TRISBB          ; and PORTB<7:0> as outputs
NOP                                ; Delay 1 cycle
btss   PORTB, #13          ; Next Instruction
```

PIC24FJ128GA010 FAMILY

REGISTER 12-2: TyCON: TIMER3 AND TIMER5 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON ⁽¹⁾	—	TSIDL ⁽¹⁾	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE ⁽¹⁾	TCKPS1 ⁽¹⁾	TCKPS0 ⁽¹⁾	—	—	TCS ⁽¹⁾	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **TON:** Timery On bit⁽¹⁾

1 = Starts 16-bit Timery

0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Stop in Idle Mode bit⁽¹⁾

1 = Discontinues module operation when the device enters Idle mode

0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit⁽¹⁾

When TCS = 1:

This bit is ignored.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits⁽¹⁾

11 = 1:256

10 = 1:64

01 = 1:8

00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit⁽¹⁾

1 = External clock from pin, TyCK (on the rising edge)

0 = Internal clock (Fosc/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through T2CON.

PIC24FJ128GA010 FAMILY

REGISTER 18-1: PMCON: PARALLEL PORT CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP	CS2P	CS1P	BEP	WRSP	RDSP
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **PMPEN:** Parallel Master Port Enable bit
 1 = PMP is enabled
 0 = PMP is disabled, no off-chip access is performed
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **PSIDL:** Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
 11 = Reserved
 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper 8 bits are on PMA<15:8> pins
 00 = Address and data appear on separate pins
- bit 10 **PTBEEN:** Byte Enable Port Enable bit (16-Bit Master mode)
 1 = PMBE port is enabled
 0 = PMBE port is disabled
- bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
 1 = PMWR/PMENB port is enabled
 0 = PMWR/PMENB port is disabled
- bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
 1 = PMRD/PMWR port is enabled
 0 = PMRD/PMWR port is disabled
- bit 7-6 **CSF<1:0>:** Chip Select Function bits
 11 = Reserved
 10 = PMCS1 and PMCS2 function as chip select
 01 = PMCS2 functions as chip select, PMCS1 functions as Address Bit 14
 00 = PMCS1 and PMCS2 function as Address Bits 15 and 14
- bit 5 **ALP:** Address Latch Polarity bit⁽¹⁾
 1 = Active-high (PMALL and PMALH)
 0 = Active-low (PMALL and PMALH)
- bit 4 **CS2P:** Chip Select 2 Polarity bit⁽¹⁾
 1 = Active-high (PMCS2)
 0 = Active-low (PMCS2)
- bit 3 **CS1P:** Chip Select 1 Polarity bit⁽¹⁾
 1 = Active-high (PMCS1/PMCS)
 0 = Active-low (PMCS1/PMCS)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

PIC24FJ128GA010 FAMILY

REGISTER 18-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

- bit 2 **BEP:** Byte Enable Polarity bit
1 = Byte enable is active-high (PMBE)
0 = Byte enable is active-low (PMBE)
- bit 1 **WRSP:** Write Strobe Polarity bit
For Slave modes and Master mode 2 (PMMODE<9:8> = 00,01,10):
1 = Write strobe is active-high (PMWR)
0 = Write strobe is active-low (PMWR)
For Master mode 1 (PMMODE<9:8> = 11):
1 = Enable strobe is active-high (PMENB)
0 = Enable strobe is active-low (PMENB)
- bit 0 **RDSP:** Read Strobe Polarity bit
For Slave modes and Master mode 2 (PMMODE<9:8> = 00,01,10):
1 = Read strobe is active-high (PMRD)
0 = Read strobe is active-low (PMRD)
For Master mode 1 (PMMODE<9:8> = 11):
1 = Read/write strobe is active-high (PMRD/PMWR)
0 = Read/write strobe is active-low (PMRD/PMWR)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

PIC24FJ128GA010 FAMILY

REGISTER 18-5: PMSTAT: PARALLEL PORT STATUS REGISTER

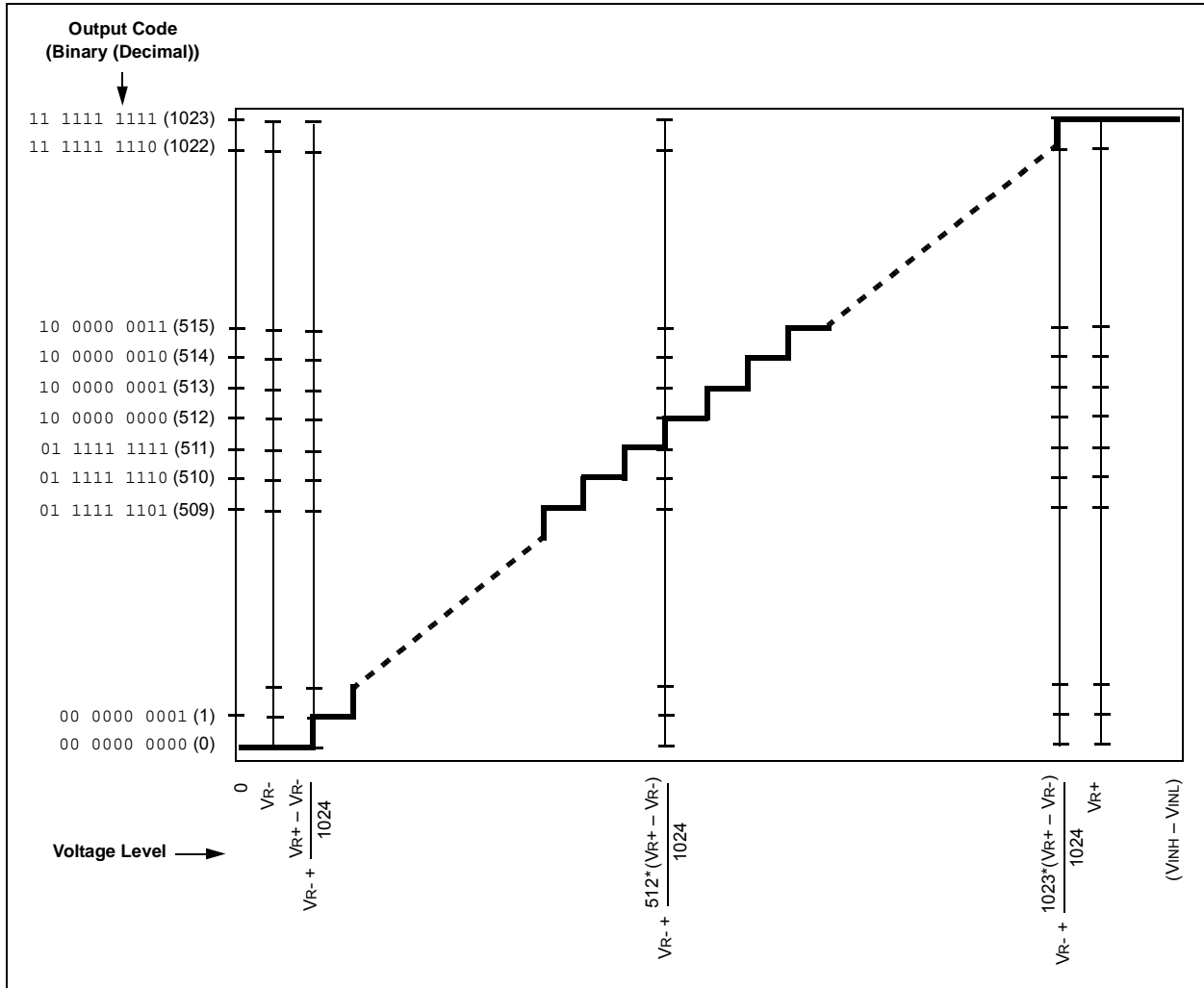
R-0	R/W-0, HS	U-0	U-0	R-0	R-0	R-0	R-0
IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
bit 15							bit 8

R-1	R/W-0, HS	U-0	U-0	R-1	R-1	R-1	R-1
OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable Input Buffer registers are full
0 = Some or all of the writable Input Buffer registers are empty
- bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full Input Byte register occurred (must be cleared in software)
0 = No overflow occurred
- bit 13-12 **Unimplemented:** Read as '0'
- bit 11-8 **IB3F:IB0F:** Input Buffer n Status Full bit
1 = Input buffer contains data that has not been read (reading the buffer will clear this bit)
0 = Input buffer does not contain any unread data
- bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable Output Buffer registers are empty
0 = Some or all of the readable Output Buffer registers are full
- bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty Output Byte register (must be cleared in software)
0 = No underflow occurred
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3-0 **OB3E:OB0E:** Output Buffer n Status Empty bit
1 = Output buffer is empty (writing data to the buffer will clear this bit)
0 = Output buffer contains data that has not been transmitted

FIGURE 21-3: A/D TRANSFER FUNCTION



REGISTER 22-1: CMCON: COMPARATOR CONTROL REGISTER (CONTINUED)

bit 5	C2INV: Comparator 2 Output Inversion bit 1 = C2 output is inverted 0 = C2 output is not inverted
bit 4	C1INV: Comparator 1 Output Inversion bit 1 = C1 output is inverted 0 = C1 output is not inverted
bit 3	C2NEG: Comparator 2 Negative Input Configure bit 1 = C2IN+ is connected to VIN- 0 = C2IN- is connected to VIN- See Figure 22-1 for the Comparator modes.
bit 2	C2POS: Comparator 2 Positive Input Configure bit 1 = C2IN+ is connected to VIN+ 0 = CVREF is connected to VIN+ See Figure 22-1 for the Comparator modes.
bit 1	C1NEG: Comparator 1 Negative Input Configure bit 1 = C1IN+ is connected to VIN- 0 = C1IN- is connected to VIN- See Figure 22-1 for the Comparator modes.
bit 0	C1POS: Comparator 1 Positive Input Configure bit 1 = C1IN is connected to VIN+ 0 = CVREF is connected to VIN+ See Figure 22-1 for the Comparator modes.

PIC24FJ128GA010 FAMILY

TABLE 25-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
GOTO	GOTO Expr	Go to Address	2	2	None
	GOTO Wn	Go to Indirect	1	2	None
INC	INC f	$f = f + 1$	1	1	C, DC, N, OV, Z
	INC f, WREG	WREG = $f + 1$	1	1	C, DC, N, OV, Z
	INC Ws, Wd	Wd = Ws + 1	1	1	C, DC, N, OV, Z
INC2	INC2 f	$f = f + 2$	1	1	C, DC, N, OV, Z
	INC2 f, WREG	WREG = $f + 2$	1	1	C, DC, N, OV, Z
	INC2 Ws, Wd	Wd = Ws + 2	1	1	C, DC, N, OV, Z
IOR	IOR f	$f = f . \text{IOR. WREG}$	1	1	N, Z
	IOR f, WREG	WREG = $f . \text{IOR. WREG}$	1	1	N, Z
	IOR #lit10, Wn	Wd = lit10 .IOR. Wd	1	1	N, Z
	IOR Wb, Ws, Wd	Wd = Wb .IOR. Ws	1	1	N, Z
	IOR Wb, #lit5, Wd	Wd = Wb .IOR. lit5	1	1	N, Z
LNK	LNK #lit14	Link Frame Pointer	1	1	None
LSR	LSR f	$f = \text{Logical Right Shift } f$	1	1	C, N, OV, Z
	LSR f, WREG	WREG = Logical Right Shift f	1	1	C, N, OV, Z
	LSR Ws, Wd	Wd = Logical Right Shift Ws	1	1	C, N, OV, Z
	LSR Wb, Wns, Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N, Z
	LSR Wb, #lit5, Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N, Z
MOV	MOV f, Wn	Move f to Wn	1	1	None
	MOV [Wns+Slit10], Wnd	Move [Wns+Slit10] to Wnd	1	1	None
	MOV f	Move f to f	1	1	N, Z
	MOV f, WREG	Move f to WREG	1	1	N, Z
	MOV #lit16, Wn	Move 16-Bit Literal to Wn	1	1	None
	MOV.b #lit8, Wn	Move 8-Bit Literal to Wn	1	1	None
	MOV Wn, f	Move Wn to f	1	1	None
	MOV Wns, [Wns+Slit10]	Move Wns to [Wns+Slit10]	1	1	
	MOV Wso, Wdo	Move Ws to Wd	1	1	None
	MOV WREG, f	Move WREG to f	1	1	N, Z
	MOV.D Wns, Wd	Move Double from W(ns):W(ns+1) to Wd	1	2	None
	MOV.D Ws, Wnd	Move Double from Ws to W(nd+1):W(nd)	1	2	None
MUL	MUL.SS Wb, Ws, Wnd	{Wnd+1, Wnd} = Signed(Wb) * Signed(Ws)	1	1	None
	MUL.SU Wb, Ws, Wnd	{Wnd+1, Wnd} = Signed(Wb) * Unsigned(Ws)	1	1	None
	MUL.US Wb, Ws, Wnd	{Wnd+1, Wnd} = Unsigned(Wb) * Signed(Ws)	1	1	None
	MUL.UU Wb, Ws, Wnd	{Wnd+1, Wnd} = Unsigned(Wb) * Unsigned(Ws)	1	1	None
	MUL.SU Wb, #lit5, Wnd	{Wnd+1, Wnd} = Signed(Wb) * Unsigned(lit5)	1	1	None
	MUL.UU Wb, #lit5, Wnd	{Wnd+1, Wnd} = Unsigned(Wb) * Unsigned(lit5)	1	1	None
	MUL f	W3:W2 = $f * \text{WREG}$	1	1	None
NEG	NEG f	$f = \bar{f} + 1$	1	1	C, DC, N, OV, Z
	NEG f, WREG	WREG = $\bar{f} + 1$	1	1	C, DC, N, OV, Z
	NEG Ws, Wd	Wd = $\bar{Ws} + 1$	1	1	C, DC, N, OV, Z
NOP	NOP	No Operation	1	1	None
	NOPR	No Operation	1	1	None
POP	POP f	Pop f from Top-of-Stack (TOS)	1	1	None
	POP Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
	POP.D Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd+1)	1	2	None
	POP.S	Pop Shadow Registers	1	1	All
PUSH	PUSH f	Push f to Top-of-Stack (TOS)	1	1	None
	PUSH Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
	PUSH.D Wns	Push W(ns):W(ns+1) to Top-of-Stack (TOS)	1	2	None
	PUSH.S	Push Shadow Registers	1	1	None

PIC24FJ128GA010 FAMILY

27.2 AC Characteristics and Timing Parameters

The information contained in this section defines the PIC24FJ128GA010 AC characteristics and timing parameters.

TABLE 27-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial Operating voltage V_{DD} range as described in Section 27.1 “DC Characteristics” .
---------------------------	---

FIGURE 27-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

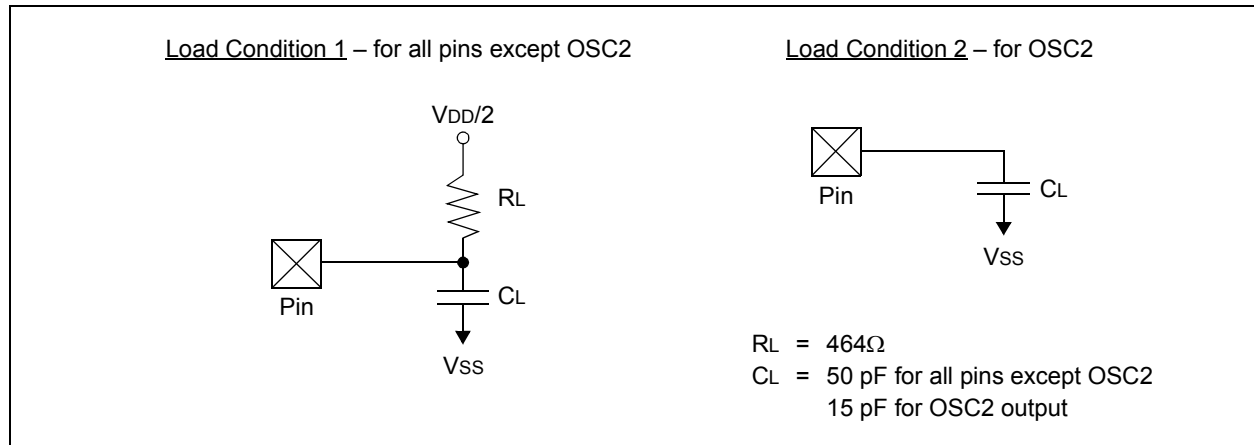


TABLE 27-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

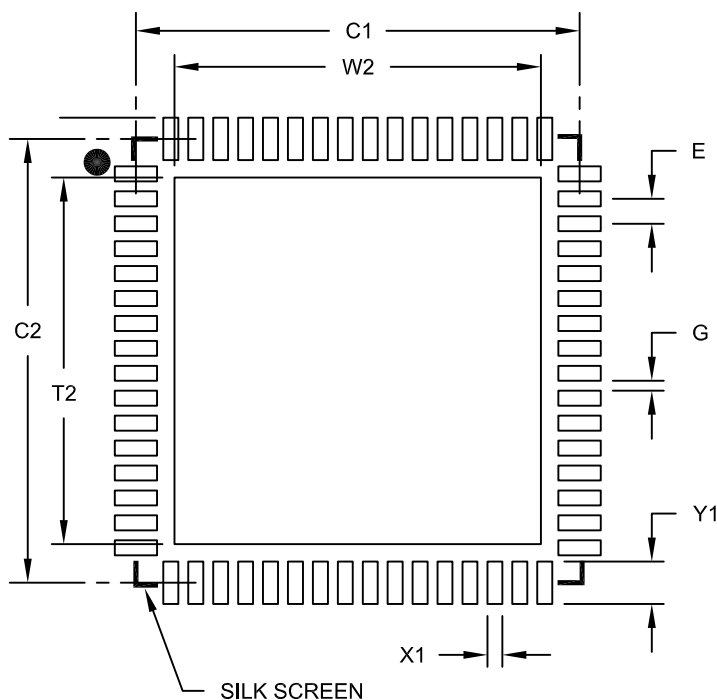
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DO50	Cosc2	OSC2/CLKO Pin	—	—	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	Cio	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I ² C™ mode

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

PIC24FJ128GA010 FAMILY

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

PIC24FJ128GA010 FAMILY

OSCTUN (FRC Oscillator Tune).....	102
PADCFG1 (Pad Configuration Control).....	166
PMADDR (Parallel Port Address).....	157
PMAEN (Parallel Port Enable).....	157
PMCON (Parallel Port Control).....	154
PMODE (Parallel Port Mode).....	156
PMSTAT (Parallel Port Status).....	158
RCFGCAL (RTCC Calibration and Configuration).....	165
RCON (Reset Control).....	58
SPIxCON1 (SPIx Control 1).....	132
SPIxCON2 (SPIx Control 2).....	133
SPIxSTAT (SPIx Status and Control).....	130
SR (CPU STATUS).....	28, 67
T1CON (Timer1 Control).....	112
TxCON (Timer2/4 Control).....	116
TyCON (Timer3/5 Control).....	117
UxMODE (UARTx Mode).....	148
UxSTA (UARTx Status and Control).....	150
WKDYHR (Weekday and Hours Value).....	169
YEAR (Year Value).....	168
Registers Map	
CPU Core.....	35
Reset Sequence.....	63
Resets.....	57
Clock Source Selection.....	59
Device Times.....	59
Revision History.....	247
RTCC	
Alarm.....	172
Configuring.....	172
Interrupt.....	172
ALRMVAL Register Mappings.....	170
Calibration.....	172
Control Registers.....	165
Module Registers.....	164
Mapping.....	164
RTCVAL Register Mapping.....	168
S	
Serial Peripheral Interface (SPI).....	127
Software Simulator (MPLAB SIM).....	215
Software Stack Pointer, Frame Pointer	
CALL Stack Frame.....	46
Special Features.....	195
Code Protection.....	195
Flexible Configuration.....	195
In-Circuit Emulation.....	195
In-Circuit Serial Programming (ICSP).....	195
JTAG Boundary Scan Interface.....	195
Watchdog Timer (WDT).....	195
Special Function Register Reset States.....	61
Symbols Used in Opcode Descriptions.....	206
T	
Table of Contents.....	5
Timer1 Module.....	111
Timer2/3 Module.....	113
Timer4/5 Module.....	113
Timing Diagrams	
CLKO and I/O.....	230
External Clock.....	228
Timing Requirements	
Capacitive Loading on Output Pin.....	227
CLKO and I/O.....	230
External Clock.....	228
Timing Specifications	
Internal RC Oscillator.....	229
Internal RC Oscillator Accuracy.....	229
PLL Clock.....	229
U	
UARTx	
Baud Rate Generator (BRG).....	146
Break and Sync Transmit Sequence.....	147
Infrared Support.....	147
IrDA	
Built-in Encoder and Decoder.....	147
External Support, Clock Output.....	147
Operation of UxCTS and UxRTS Control Pins.....	147
Receiving in	
8-Bit or 9-Bit Data Mode.....	147
Transmitting	
8-Bit Data Mode.....	147
Transmitting in	
9-Bit Data Mode.....	147
Universal Asynchronous Receiver Transmitter (UART) ...	145
V	
VDDCORE/VCAP Pin.....	201
W	
Watchdog Timer (WDT).....	202
Control Register.....	202
Programming Considerations.....	202
WWW Address.....	253
WWW, On-Line Support.....	6

Worldwide Sales and Service

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta

Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston

Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago

Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland

Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas

Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis

Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles

Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara

Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto

Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office

Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney

Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu

Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing

Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou

Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR

Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing

Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao

Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai

Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang

Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen

Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan

Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian

Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen

Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai

Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore

Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi

Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune

Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Osaka

Tel: 81-66-152-7160
Fax: 81-66-152-9310

Japan - Yokohama

Tel: 81-45-471-6166
Fax: 81-45-471-6122

Korea - Daegu

Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul

Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang

Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila

Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore

Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu

Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung

Tel: 886-7-536-4818
Fax: 886-7-330-9305

Taiwan - Taipei

Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok

Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels

Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen

Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris

Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich

Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan

Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen

Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid

Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham

Tel: 44-118-921-5869
Fax: 44-118-921-5820

11/29/11