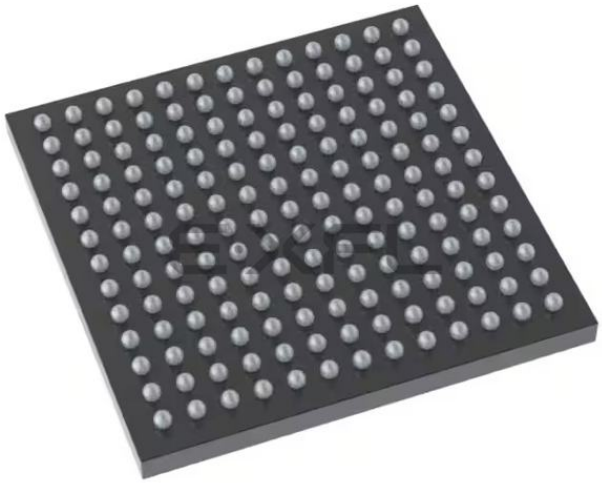

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	168-UFBGA, WLCSP
Supplier Device Package	168-WLCSP (4.89x5.69)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f469agy6tr

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The DSI Host main features:

- Compliant with MIPI® Alliance standards
- Interface with MIPI® D-PHY
- Supports all commands defined in the MIPI® Alliance specification for DCS:
  - Transmission of all Command mode packets through the APB interface
  - Transmission of commands in low-power and high-speed during Video Mode
- Supports up to two D-PHY data lanes
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports Ultra Low-Power mode with PLL disabled
- ECC and Checksum capabilities
- Support for End of Transmission Packet (EoTp)
- Fault recovery schemes
- 3D transmission support
- Configurable selection of system interfaces:
  - AMBA APB for control and optional support for Generic and DCS commands
  - Video Mode interface through LTDC
  - Adapted Command Mode interface through LTDC
- Independently programmable Virtual Channel ID in
  - Video Mode
  - Adapted Command Mode
  - APB Slave

Video Mode interfaces features:

- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB
- Programmable polarity of all LTDC interface signals
- Extended resolutions beyond the DPI standard maximum resolution of 800x480 pixels: maximum resolution is limited by available DSI physical link bandwidth:
  - Number of lanes: 2
  - Maximum speed per lane: 500Mbps

Adapted interface features:

- Support for sending large amounts of data through the *memory_write_start* (WMS) and *memory_write_continue* (WMC) DCS commands
- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB

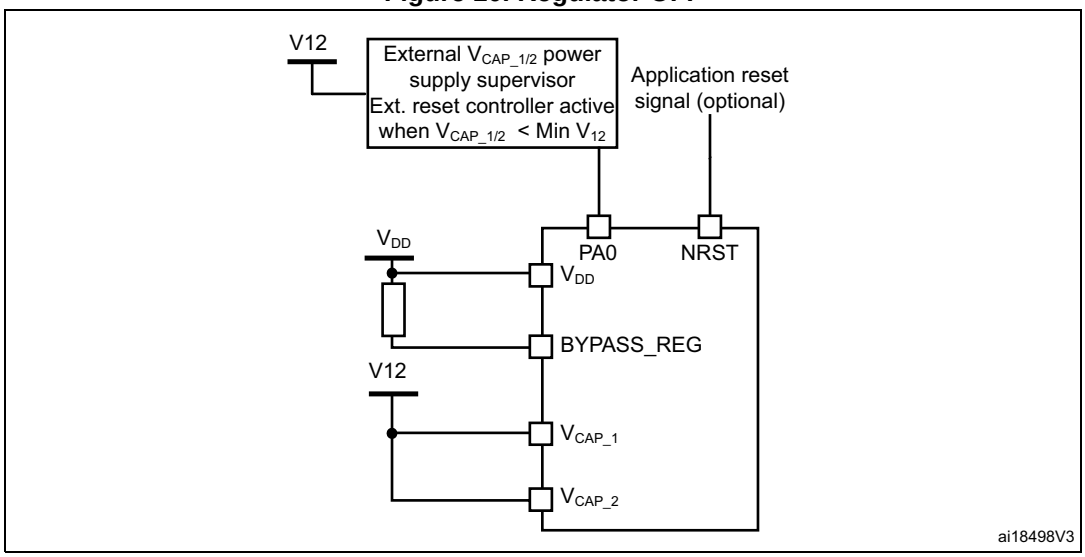
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. Refer to *Operating conditions*.The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to *Section 2.18*.

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

Figure 10. Regulator OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see *Figure 11*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 12*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application (see Operating conditions).

FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

2.35 Universal serial bus on-the-go full-speed (OTG_FS)

The device embeds an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1.28 KB with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- HNP/SNP/IP inside (no need for any external resistor)

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.36 Universal serial bus on-the-go high-speed (OTG_HS)

The device embeds a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

Table 10. STM32F469xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	J9	M4	-	-	100	P15	PH10	I/O	FT	-	TIM5_CH1, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	K9	N3	-	-	101	N15	PH11	I/O	FT	-	TIM5_CH2, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	-	H10	P2	-	-	102	M15	PH12	I/O	FT	-	TIM5_CH3, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	-	H7	-	-	-	K10	VSS	S	-	-	-	-
-	66	-	-	-	-	103	K11	VDD	S	-	-	-	-
46	67	N10	H5	P12	85	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT	-
47	68	N11	K4	P13	86	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT	OTG_HS_VBUS
48	69	N12	P1	R14	87	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, I2S2ext_SD, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT	-
49	70	N13	N2	R15	88	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT	-
50	71	L10	L4	P15	89	108	L15	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
51	72	M10	N1	P14	90	109	L14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
52	73	L11	M3	N15	91	110	K15	PD10	I/O	FT	-	USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
-	74	M11	J4	N14	92	111	N10	PD11	I/O	FT	-	USART3_CTS, QUADSPI_BK1_IO0, FMC_A16/FMC_CLE, EVENTOUT	-

Table 10. STM32F469xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
83	115	A9	C4	A12	141	163	A12	PC12	I/O	FT	-	TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDIO_CK, DCMI_D9, EVENTOUT	-
84	116	C9	E6	B12	142	164	B12	PD0	I/O	FT	-	CAN1_RX, FMC_D2, EVENTOUT	-
85	117	C7	A3	C12	143	165	C12	PD1	I/O	FT	-	CAN1_TX, FMC_D3, EVENTOUT	-
86	118	B8	C5	D12	144	166	D12	PD2	I/O	FT	-	TRACED2, TIM3_ETR, UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-
87	119	C8	D6	D11	145	167	C11	PD3	I/O	FT	-	SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
88	120	C6	B4	D10	146	168	D11	PD4	I/O	FT	-	USART2_RTS, FMC_NOE, EVENTOUT	-
89	121	B7	C6	C11	147	169	C10	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	122	F8	A4	D8	148	170	F8	VSS	S	-	-	-	-
-	123	F7	-	C8	149	171	E9	VDD	S	-	-	-	-
90	124	D7	E7	B11	150	172	B11	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-
91	-	A8	A5	A11	151	173	A11	PD7	I/O	FT	-	USART2_CK, FMC_NE1, EVENTOUT	-
-	-	-	-	-	-	174	B10	PJ12	I/O	FT	-	LCD_G3, LCD_B0, EVENTOUT	-
-	-	-	-	-	-	175	B9	PJ13	I/O	FT	-	LCD_G4, LCD_B1, EVENTOUT	-
-	-	-	-	-	-	176	C9	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
-	-	-	-	-	-	177	D10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-
-	125	E6	D7	C10	152	178	D9	PG9	I/O	FT	-	USART6_RX, QUADSPI_BK2_IO2, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT	-
-	126	E7	C7	B10	153	179	C8	PG10	I/O	FT	-	LCD_G3, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
-	127	B6	B6	B9	154	180	B8	PG11	I/O	FT	-	ETH_MII_TX_EN/ETH_RMII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT	-

Table 10. STM32F469xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
96	136	B4	A9	B5	165	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT	-
97	137	A5	F8	D6	166	197	E6	BOOT0	I	B	-	-	VPP
98	138	D4	B9	A5	167	198	A7	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDIO_D4, DCMI_D6, LCD_B6, EVENTOUT	-
99	139	C4	E9	B4	168	199	B4	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDIO_D5, DCMI_D7, LCD_B7, EVENTOUT	-
NC (2)	140	A4	A10	A4	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, UART8_Rx, FMC_NBL0, DCMI_D2, EVENTOUT	-
NC (2)	141	A3	C9	A3	170	201	A5	PE1	I/O	FT	-	UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	E3	B10	D5	-	202	F6	VSS	S	-	-	-	-
-	142	C3	D9	C6	171	203	E5	PDR_ON	S	-	-	-	-
100	143	D3	A11	C5	172	204	E7	VDD	S	-	-	-	-
-	-	B3	D10	D4	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	A2	C10	C4	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	A1	B11	C3	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	B1	A12	C2	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

1. **Function availability depends on the chosen device.**
2. NC (not-connected) pins are not bonded. They must be configured by software to output push-pull and forced to “0” in the output data register to avoid extra current consumption in low power modes.
3. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
4. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F4xx reference manual, available from the STMicroelectronics website: www.st.com.
5. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

Table 12. Alternate function (continued)

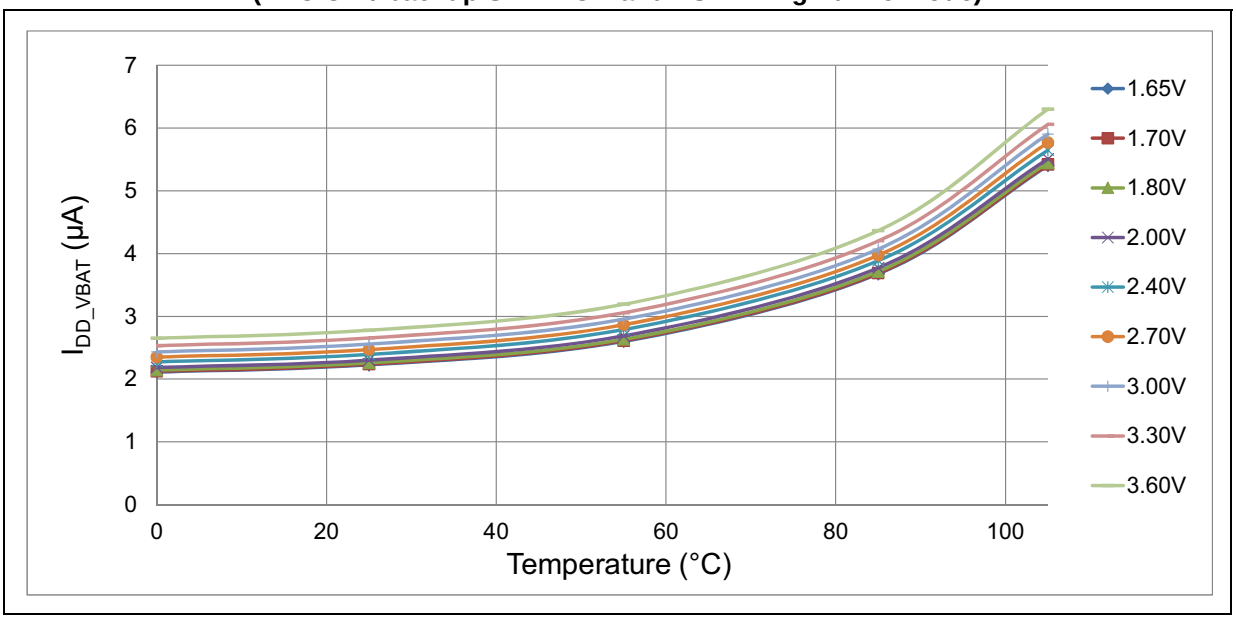
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI HOST	LCD	SYS
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FMC_A0	-	-	EVENT OUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FMC_A1	-	-	EVENT OUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FMC_A2	-	-	EVENT OUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	EVENT OUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	EVENT OUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVENT OUT
	PF6	-	-	-	TIM10_CH1	-	SPI5_NSS	SAI1_SD_B	-	UART7_Rx	QUADSPI_BK1_IO3	-	-	-	-	-	EVENT OUT
	PF7	-	-	-	TIM11_CH1	-	SPI5_SCK	SAI1_MCLK_B	-	UART7_Tx	QUADSPI_BK1_IO2	-	-	-	-	-	EVENT OUT
	PF8	-	-	-	-	-	SPI5_MISO	SAI1_SCK_B	-	-	TIM13_CH1	QUADSPI_BK1_IO0	-	-	-	-	EVENT OUT
	PF9	-	-	-	-	-	SPI5_MOSI	SAI1_FS_B	-	-	TIM14_CH1	QUADSPI_BK1_IO1	-	-	-	-	EVENT OUT
	PF10	-	-	-	-	-	-	-	-	-	QUADSPI_CLK		-	-	DCMI_D11	LCD_DE	EVENT OUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	-	-	-	FMC_SDNRAS	DCMI_D12	-	EVENT OUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENT OUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A7	-	-	EVENT OUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A8	-	-	EVENT OUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A9	-	-	EVENT 'OUT

Table 25. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in RUN mode	All Peripherals enabled(2)(3)	168	97	102	128	154	mA
			150	87	92	118	143	
			144	80	84	108	131	
			120	65	68	88	108	
			90	51	54	73	93	
			60	37	41	59	79	
			30	21	23	42	62	
			25	18	20	39	59	
		All Peripherals disabled	168	49	55	79	105	
			150	44	49	44	100	
			144	40	45	68	92	
			120	36	39	58	78	
			90	29	32	51	71	
			60	22	25	44	64	
			30	13	15	34	54	
			25	11	13	32	52	

1. Guaranteed based on test during characterization.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

Figure 28. Typical V_{BAT} current consumption (RTC ON / backup SRAM ON and LSE in High drive mode)



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 58: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 33*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the informations given in this paragraph are based on characterization results obtained with typical external components specified in *Table 38*.

In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 38. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	MΩ
I_{DD}	LSE current consumption	Low power mode(2)	-	-	1	µA
		High drive mode(2)	-	-	3	
ACC_{LSE}(3)	LSE accuracy	-	− 500	-	500	ppm
G_m_crit_max	Maximum critical crystal g_m	Low power mode(2)	-	-	0.56	µA/V
		High drive mode(2)	-	-	1.5	
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. LSE mode cannot be changed “on the fly” otherwise, a glitch can be generated on OSCIN pin.
3. This parameter depends on the crystal used in the application. Refer to application note AN2867.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is based on characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from www.st.com.

Figure 32. Typical application with a 32.768 kHz crystal

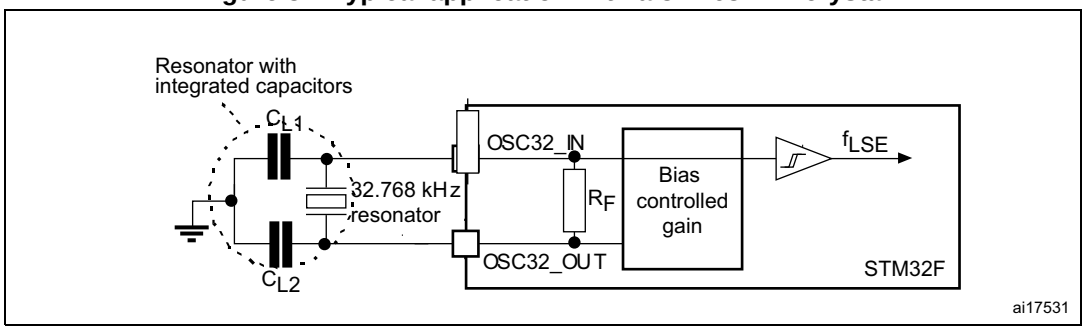


Figure 37. MIPI D-PHY HS/LP clock lane transition timing diagram

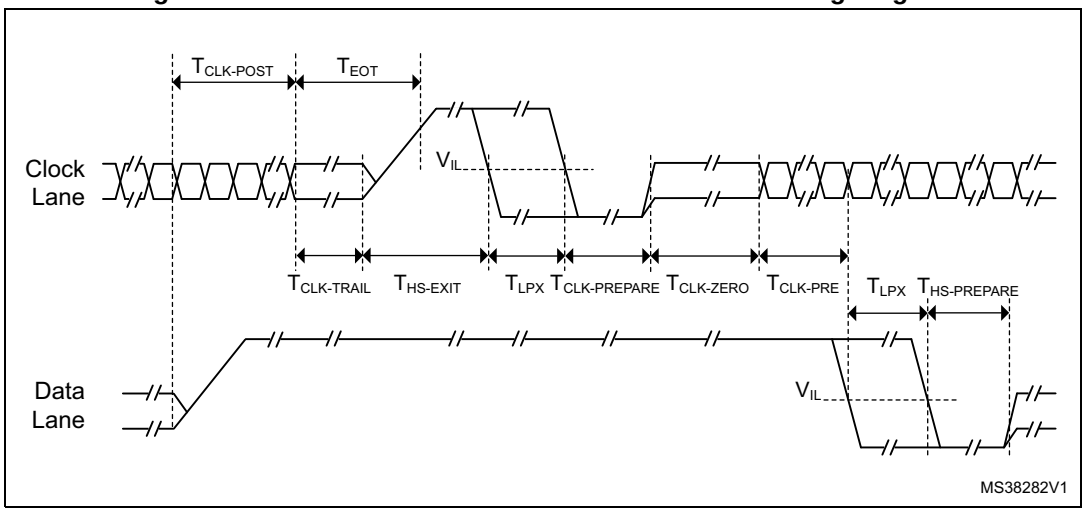
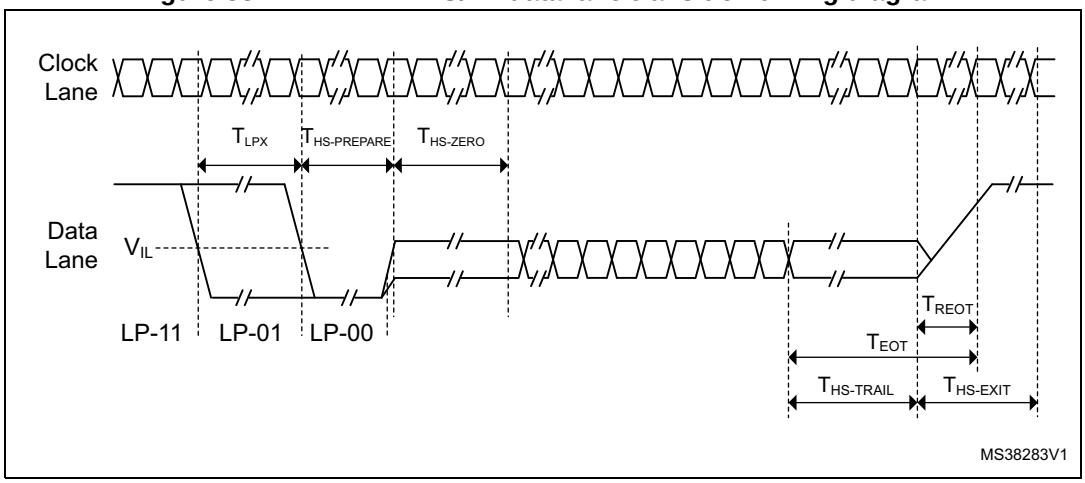


Figure 38. MIPI D-PHY HS/LP data lane transition timing diagram



5.3.14 MIPI D-PHY PLL characteristics

The parameters given in *Table 47* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 47. DSI-PLL characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	4	-	100	MHz
f_{PLL_INFIN}	PFD input clock	-	4	-	25	
f_{PLL_OUT}	PLL multiplier output clock	-	31.25	-	500	
f_{VCO_OUT}	PLL VCO output	-	500	-	1000	
t_{LOCK}	PLL lock time	-	-	-	200	µs

Table 55. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD S5.3.1, LQFP100, LQFP144, LQFP176, LQFP208, UFBGA169, UFBGA176, TFBGA216 and WLCSP148 packages	C3	250	

1. Guaranteed based on test during characterization.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 56. Electrical sensitivities(1)

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

1. MSV on PA4 and PA5 is 5 V, versus 5.4 V on all IOs.

5.3.19 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 57*.

5.3.25 Temperature sensor characteristics

Table 82. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	

1. Based on test during characterization.
2. Guaranteed by design.

Table 83. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

5.3.26 V_{BAT} monitoring characteristics

Table 84. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

5.3.27 Reference voltage

The parameters given in *Table 85* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 85. internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S_vrefint}$(1)	ADC sampling time when reading the internal reference voltage		10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV

Table 92. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK} - 1$	$3T_{HCLK}+0.5$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK} - 0.5$	$2T_{HCLK}$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{HCLK} - 1$	$T_{HCLK}+1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	1	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	2	
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK}+0.5$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high)	0	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$T_{HCLK} - 0.5$	-	
$t_{h(BL_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK}+1.5$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	$T_{HCLK}+1$	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Based on test during characterization.

Table 93. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}+0.5$	$8T_{HCLK}+2$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1$	$5T_{HCLK} +1.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK} +1.5$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$	-	

1. Based on test during characterization.

Figure 62. Asynchronous multiplexed PSRAM/NOR write waveforms

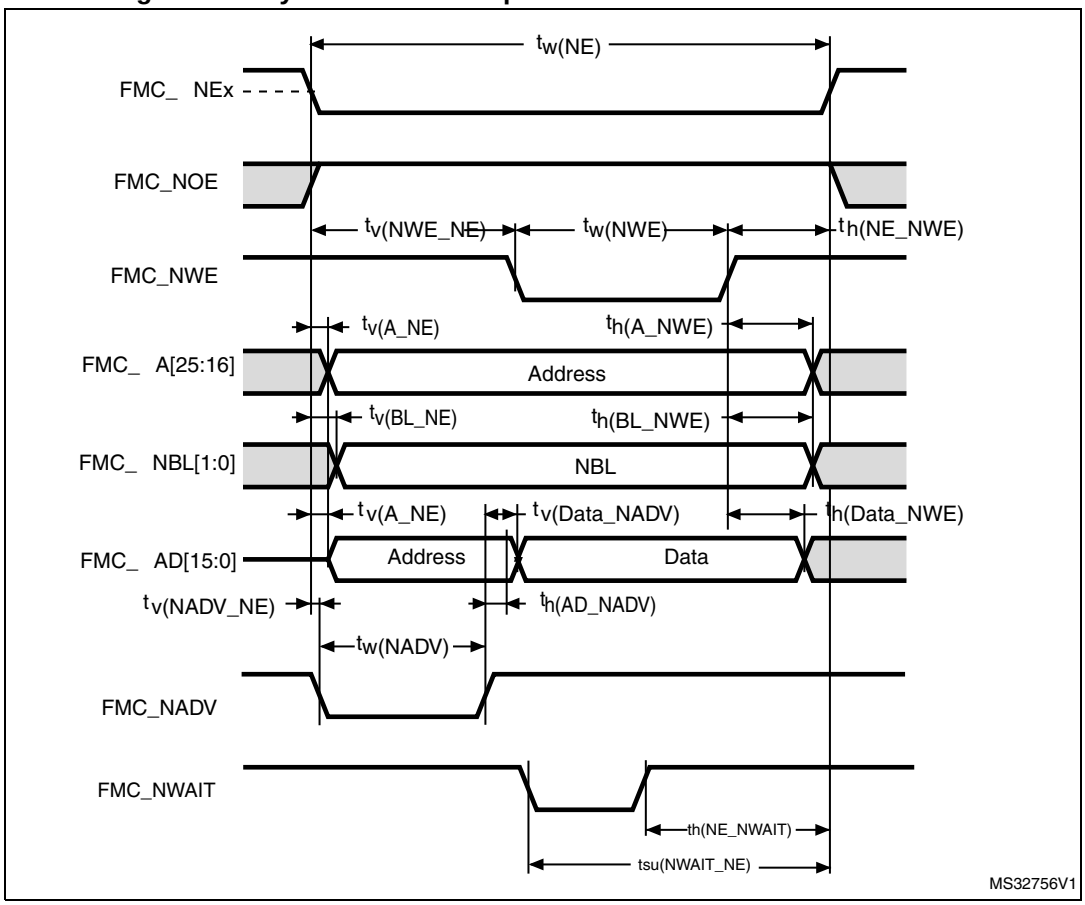


Table 94. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$	$4T_{HCLK}$+0.5	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK} − 1	T_{HCLK}+0.5	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{HCLK}$	$2T_{HCLK}$+0.5	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0.5	1	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK} − 0.5	T_{HCLK}+ 0.5	
$t_{h(AD_NADV)}$	FMC_AD (address) valid hold time after FMC_NADV high	T_{HCLK} − 2	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	T_{HCLK} − 2	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	T_{HCLK} +1.5	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	T_{HCLK} +0.5	-	

1. Based on test during characterization.

Table 103. LPSDR SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	2.5	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	1	-	
$t_{d(SDCLKL_SDNRAS}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	1	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	1	-	

1. Guaranteed based on test during characterization.

Figure 72. SDRAM write access waveforms

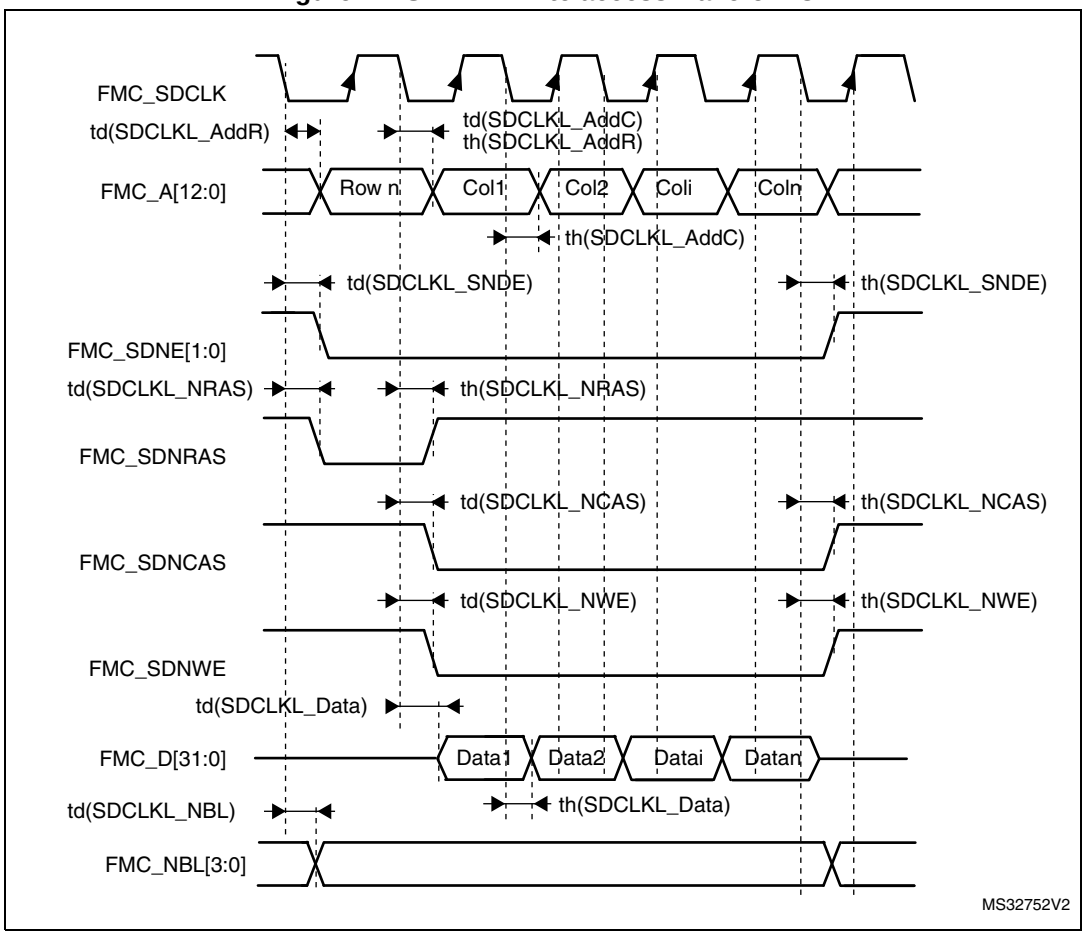
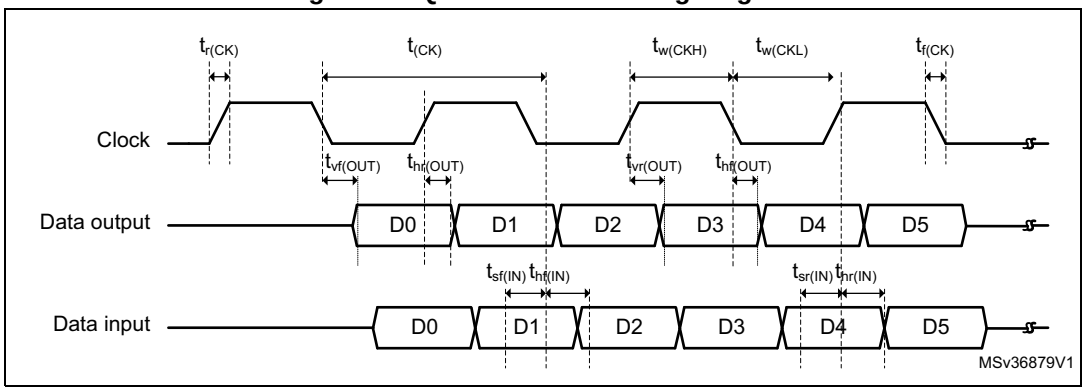


Table 107. Quad-SPI characteristics in DDR mode(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{ck} $1/t_{(CK)}$	Quad-SPI clock frequency	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF	-	-	80	MHz
		1.71 V ≤ V_{DD} ≤ 3.6 V, C_L = 15 pF	-	-	70	
$t_{w(CKH)}$	Quad-SPI clock high time	-	$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$	Quad-SPI clock low time	-	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	
$t_{sr(IN)}$ $t_{sf(IN)}$	Data input set-up time	2.7 V ≤ V_{DD} ≤ 3.6 V	2	-	-	
		1.71 V ≤ V_{DD} ≤ 3.6 V	0.5	-	-	
$t_{hr(IN)}$ $t_{hf(IN)}$	Data input hold time	2.7 V ≤ V_{DD} ≤ 3.6 V	3	-	-	
		1.71 V ≤ V_{DD} ≤ 3.6 V	4.5	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	DHHC=0	-	8	10.5	
		DHHC=1 Pres=1,2…	-	$T_{hclk}/2+2$	$T_{hclk}/2+2.5$	
$t_{h(OUT)}$ $t_{f(OUT)}$	Data output hold time	DHHC=0	7	-	-	
		DHHC=1 Pres=1,2…	$T_{hclk}/2+0.5$	-	-	

1. Guaranteed based on test during characterization.

Figure 74. Quad-SPI DDR timing diagram



5.3.31 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 108* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}