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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 180MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 114 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 384K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 169-UFBGA |
| Supplier Device Package | 169-UFBGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f469aih6 |

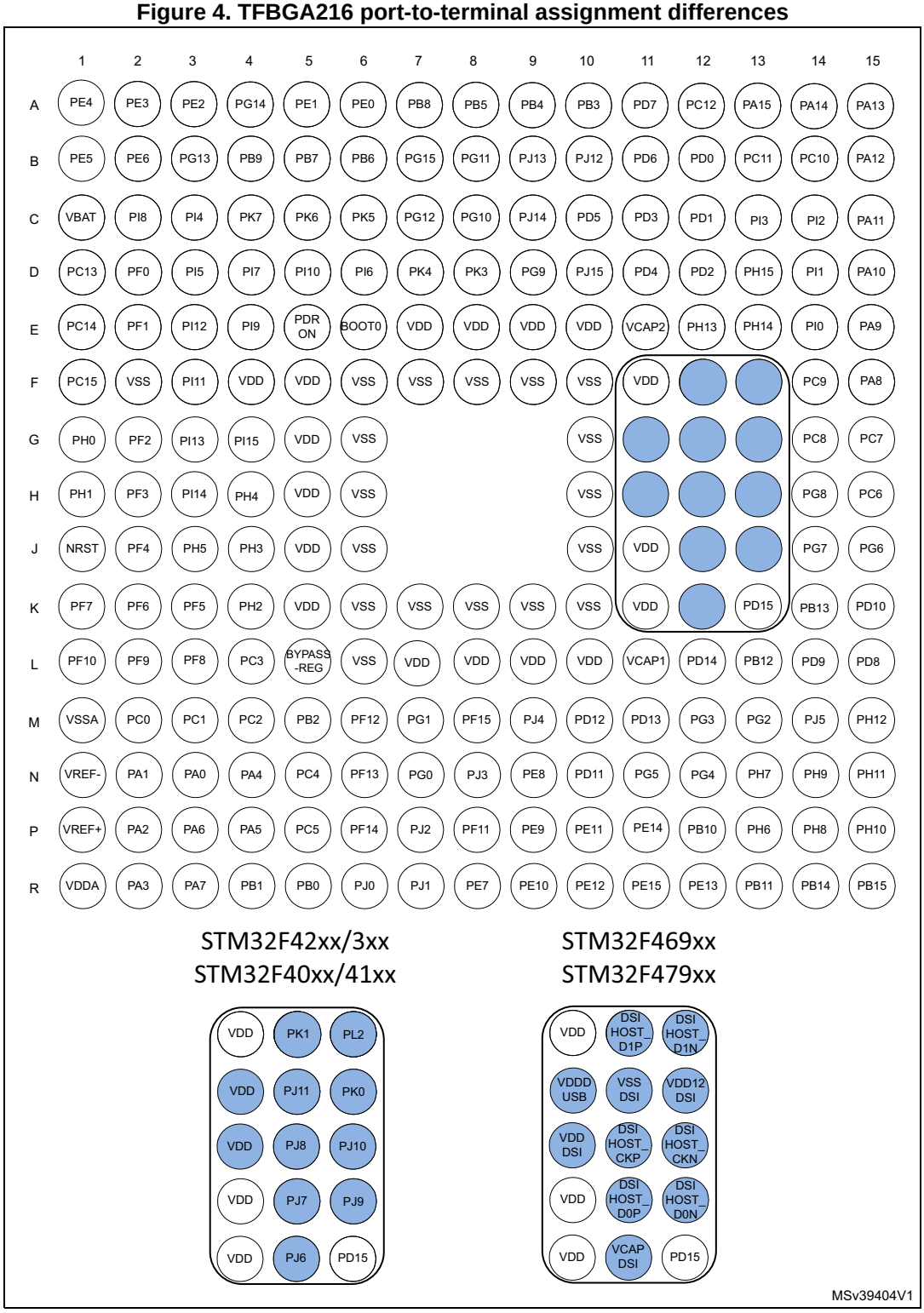
**Table 2. STM32F469xx features and peripheral counts (continued)**

| Peripherals | STM32F469Vx | STM32F469Zx | STM32F469Ax | STM32F469Ix | STM32F469Bx | STM32F469Nx |
|---|---|---|---|---|---|---|
| MIPI-DSI Host | Yes | | | | | |
| LCD-TFT | Yes | | | | | |
| Chrom-ART Accelerator™ (DMA2D) | Yes | | | | | |
| GPIOs | 71 | 106 | 114 | 131 | 161 | 161 |
| 12-bit ADC<br>Number of channels | 3 | | | | | |
| | 14 | 20 | 24 | 16 | 24 | 24 |
| 12-bit DAC<br>Number of channels | Yes<br>2 | | | | | |
| Maximum CPU frequency | 180 MHz | | | | | |
| Operating voltage | 1.7 to 3.6V(2) | | | | | |
| Operating temperatures | Ambient operating temperature: −40 to 85 °C / −40 to 105 °C<br>Junction temperature: −40 to 105 °C / −40 to 125 °C | | | | | |
| Package | LQFP100 | LQPF144 | UFBGA169<br>WLCSP168 | LQFP176<br>UFBGA176 | LQFP208 | TFBGA216 |

1. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
2. VDD/VDDA minimum value of 1.7 V is obtained when the internal reset is OFF (refer to *Section 2.19.2*).

### 1.1.4 TFBGA216 package

**Figure 4. TFBGA216 port-to-terminal assignment differences**




1. The highlighted pins are substituted with dedicated DSI IO pins on STM32F469xx/479xx devices.

## 2.4 Embedded Flash memory

The devices embed a Flash memory of up to 2 Mbytes available for storing programs and data.

## 2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 2.6 Embedded SRAM

All devices embed:

- Up to 384Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM

  RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM

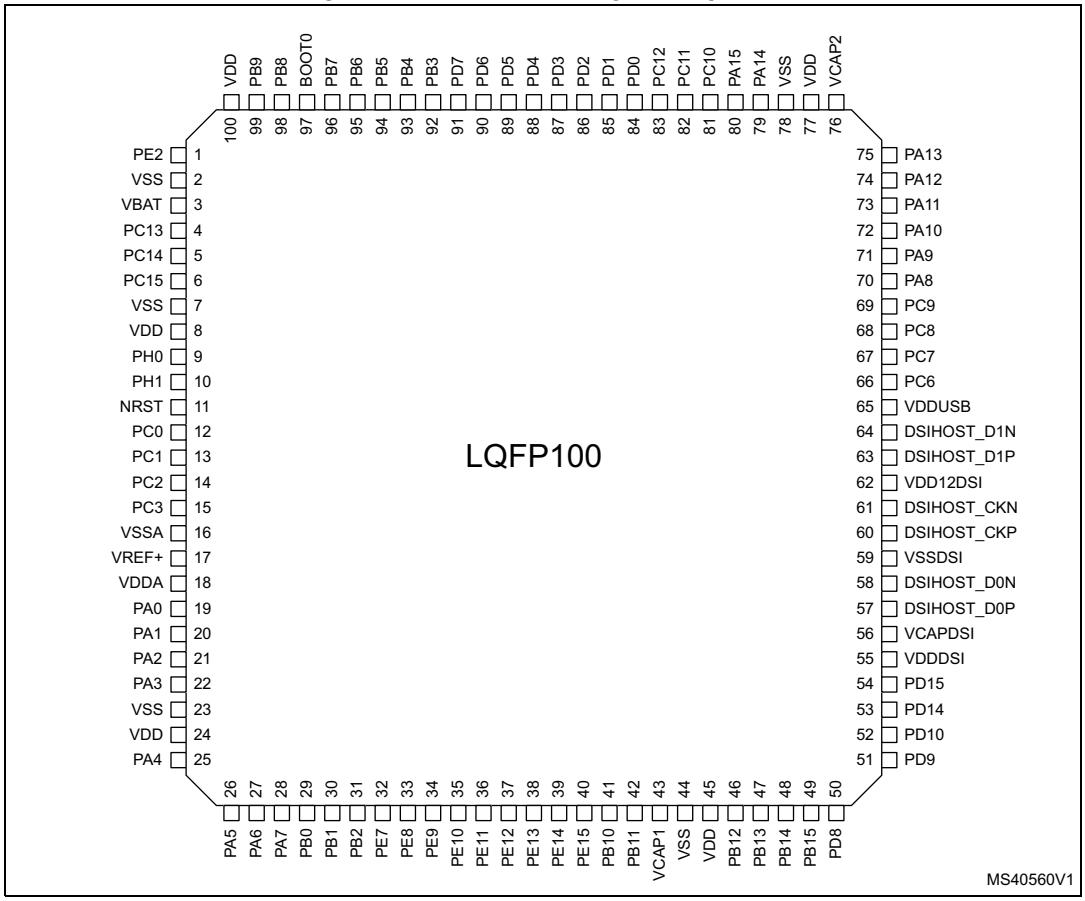
  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or $V_{BAT}$ mode.

## 2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, QUADSPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

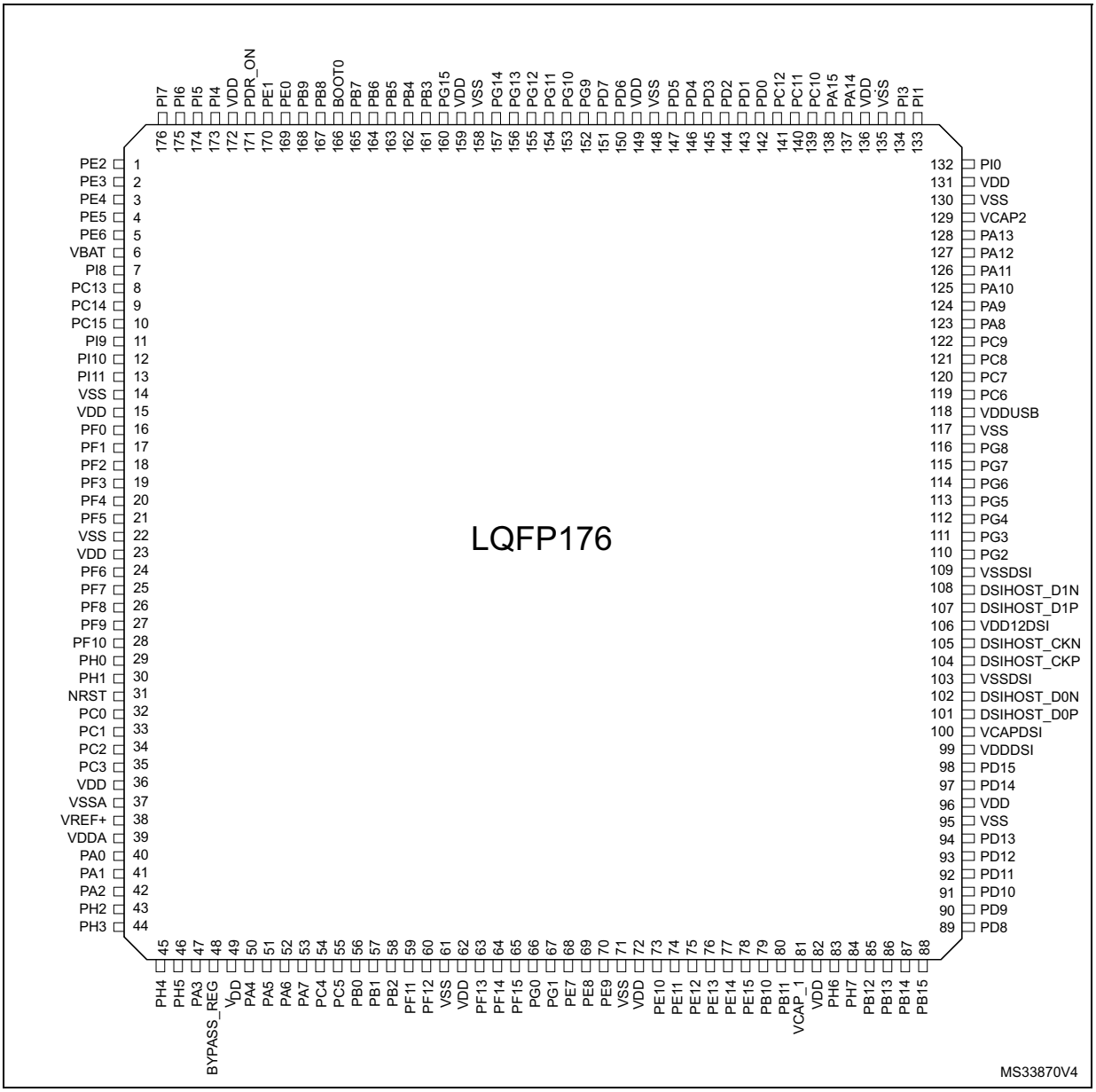
# 3 Pinouts and pin description

**Figure 13. STM32F46x LQFP100 pinout**




1. The above figure shows the package top view.

**Figure 18. STM32F46x LQFP176 pinout**




1. The above figure shows the package top view.

**Table 12. Alternate function (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/2/3 | SPI1/2/3/4/5/6 | SPI2/3/SAI1 | SPI2/3/USART1/2/3 | USART6/UART4/5/7/8 | CAN1/2/TIM12/13/14/QUADSPI/LCD | QUADSPI/OTG2_HS/OTG1_FS | ETH | FMC/SDIO/OTG2_FS | DCMI/DSIHOST | LCD | SYS |
| Port J | PJ0 | - | - | - | - | - | - | - | - | - | LCD_R7 | - | - | - | - | LCD_R1 | EVENTOUT |
| | PJ1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R2 | EVENTOUT |
| | PJ2 | - | - | - | - | - | - | - | - | - | - | - | - | - | DSIHOST_TE | LCD_R3 | EVENTOUT |
| | PJ3 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R4 | EVENTOUT |
| | PJ4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R5 | EVENTOUT |
| | PJ5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R6 | EVENTOUT |
| | PJ12 | - | - | - | - | - | - | - | - | - | LCD_G3 | - | - | - | - | LCD_B0 | EVENTOUT |
| | PJ13 | - | - | - | - | - | - | - | - | - | LCD_G4 | - | - | - | - | LCD_B1 | EVENTOUT |
| | PJ14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B2 | EVENTOUT |
| | PJ15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B3 | EVENTOUT |
| Port K | PK3 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B4 | EVENTOUT |
| | PK4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B5 | EVENTOUT |
| | PK5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B6 | EVENTOUT |
| | PK6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B7 | EVENTOUT |
| | PK7 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DE | EVENTOUT |

**Table 15. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ | Total current into sum of all $V_{DD\_x}$ power lines (source)(1) | 290 | mA |
| $\Sigma I_{VSS}$ | Total current out of sum of all $V_{SS\_x}$ ground lines (sink)(1) | − 290 | |
| $\Sigma I_{VDDUSB}$ | Total current into $V_{DDUSB}$ power line (source) | 25 | |
| $I_{VDD}$ | Maximum current into each $V_{DD\_x}$ power line (source)(1) | 100 | |
| $I_{VSS}$ | Maximum current out of each $V_{SS\_x}$ ground line (sink)(1) | − 100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current sourced by any I/Os and control pin | − 25 | |
| $\Sigma I_{IO}$ | Total output current sunk by sum of all I/O and control pins (2) | 120 | |
| | Total output current sunk by sum of all USB I/Os | 25 | |
| | Total output current sourced by sum of all I/Os and control pins(2) | − 120 | |
| $I_{INJ(PIN)}$ (3) | Injected current on FT pins (4) | − 5/+0 | |
| | Injected current on NRST and BOOT0 pins (4) | | |
| | Injected current on TTa pins(5) | ±5 | |
| $\Sigma I_{INJ(PIN)}$(5) | Total injected current (sum of all I/O and control pins)(6) | ±25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.24*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 14* for the values of the maximum allowed input voltage.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 16. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | − 65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 125 | °C |

## 5.3 Operating conditions

### 5.3.1 General operating conditions

**Table 17. General operating conditions**

| Symbol | Parameter | Conditions[1] | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF | | 0 | - | 120 | MHz |
| | | Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON | Over-drive OFF | 0 | - | 144 | |
| | | | Over-drive ON | | - | 168 | |
| | | Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON | Over-drive OFF | 0 | - | 168 | |
| | | | Over-drive ON | | - | 180 | |
| $f_{PCLK1}$ | Internal APB1 clock frequency | Over-drive OFF | | 0 | - | 42 | |
| | | Over-drive ON | | 0 | - | 45 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | Over-drive OFF | | 0 | - | 84 | |
| | | Over-drive ON | | 0 | - | 90 | |
| $V_{DD}$ | Standard operating voltage | - | | 1.7[2] | - | 3.6 | V |
| $V_{DDA}$[3][4] | Analog operating voltage (ADC limited to 1.2 M samples) | Must be the same potential as $V_{DD}$[5] | | 1.7[2] | - | 2.4 | |
| | Analog operating voltage (ADC limited to 2.4 M samples) | | | 2.4 | - | 3.6 | |
| $V_{DDUSB}$ | USB supply voltage (supply voltage for PA11, PA12, PB14 and PB15 pins) | USB not used | | 1.7 | 3.3 | 3.6 | |
| | | USB used | | 3.0 | - | 3.6 | |
| $V_{DDDSI}$ | DSI system operating voltage | - | | 1.7[2] | - | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | - | | 1.65 | - | 3.6 | |

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to $f_{HCLK}$ frequency and $V_{DD}$ range (see *Table 18: Limitations depending on the operating power supply range*).
- When the regulator is OFF, the $V_{12}$ is provided externally, as described in *Table 17: General operating conditions*.
- The voltage scaling and over-drive mode are adjusted to $f_{HCLK}$ frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 120$ MHz
  - Scale 2 for 120 MHz < $f_{HCLK} \leq 144$ MHz
  - Scale 1 for 144 MHz < $f_{HCLK} \leq 180$ MHz. The over-drive is only ON at 180 MHz.
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 25 MHz and PLL is ON when $f_{HCLK}$ is higher than 25 MHz.
- The typical current consumption values are obtained for 1.7 V ≤ $V_{DD}$ ≤ 3.6 V voltage range and for ambient temperature $T_A$= 25 °C unless otherwise specified.
- The maximum values are obtained for 1.7 V ≤ $V_{DD}$ ≤ 3.6 V voltage range and a maximum ambient temperature ($T_A$), unless otherwise specified.
- For the voltage range 1.7 V ≤ $V_{DD}$ ≤ 2.1 V the maximum frequency is 168 MHz.

**Table 30. Typical and maximum current consumption in Standby mode**

| Symbol | Parameter | Conditions | Typ(1) | | | Max(2) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| | | | $V_{DD}$ = 1.7 V | $V_{DD}$= 2.4 V | $V_{DD}$ = 3.3 V | $V_{DD}$ = 3.3 V | | | |
| $I_{DD\_STBY}$ | Supply current in Standby mode | Backup SRAM ON, RTC and LSE oscillator OFF | 1.7 | 2.5 | 2.9 | 6(3) | 18 | 35(3) | µA |
| | | Backup SRAM OFF, RTC and LSE oscillator OFF | 1.0 | 1.8 | 2.20 | 5(3) | 15 | 30(3) | |
| | | Backup SRAM OFF, RTC ON and LSE oscillator in Power Drive mode | 1.7 | 2.7 | 3.2 | 7 | 20 | 39 | |
| | | Backup SRAM ON, RTC ON and LSE oscillator in Power Drive mode | 2.4 | 3.4 | 4.0 | 8 | 25 | 48 | |
| | | Backup SRAM ON, RTC ON and LSE oscillator in High Drive mode | 3.2 | 4.2 | 4.8 | 10 | 29 | 57 | |
| | | Backup SRAM OFF, RTC ON and LSE oscillator in High Drive mode | 2.5 | 3.5 | 4.1 | 8 | 25 | 48 | |

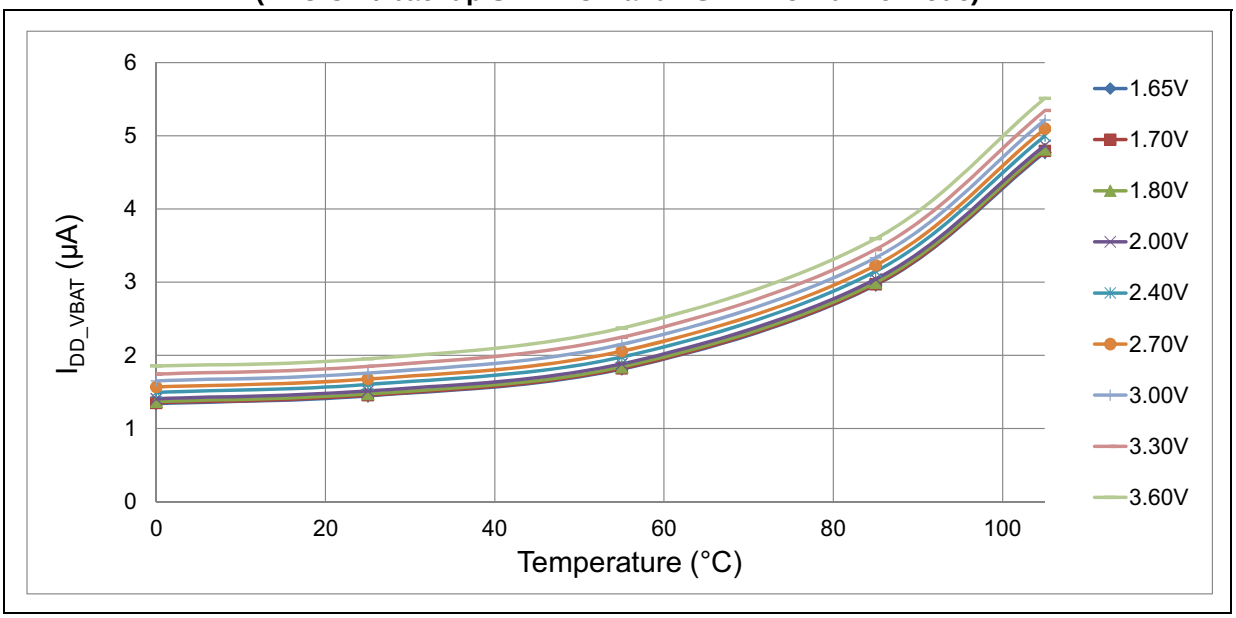
1. PDR is off for $V_{DD}$=1.7 V. When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

**Table 31. Typical and maximum current consumption in $V_{BAT}$ mode**

| Symbol | Parameter | Conditions[1] | Typ | | | Max[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| | | | $V_{BAT}$ = 1.7 V | $V_{BAT}$= 2.4 V | $V_{BAT}$ = 3.3 V | $V_{BAT}$ = 3.3 V | | | |
| $I_{DD\_VBAT}$ | Backup domain supply current | Backup SRAM ON, RTC ON and LSE oscillator in Low Power mode | 1.431 | 1.577 | 1.825 | 1.9 | 12.0 | 24.0 | µA |
| | | Backup SRAM OFF, RTC ON and LSE oscillator in Low Power mode | 0.720 | 0.849 | 1.060 | 1.1 | 7.0 | 13.9 | |
| | | Backup SRAM ON, RTC ON and LSE oscillator in High Drive mode | 2.212 | 2.368 | 2.630 | 2.80 | 17.3 | 34.6 | |
| | | Backup SRAM OFF, RTC ON and LSE oscillator in High Drive mode | 1.499 | 1.637 | 1.862 | 2.0 | 12.3 | 24.5 | |
| | | Backup SRAM ON, RTC and LSE OFF | 0.710 | 0.720 | 0.760 | 0.8[3] | 5.0 | 10.0[3] | |
| | | Backup SRAM OFF, RTC and LSE OFF | 0.018 | 0.020 | 0.024 | 0.2[3] | 2.0 | 4.0[3] | |

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a $C_L$ of 6 pF for typical values.
2. Based on characterization, tested in production.
3. Based on test during characterization.

**Figure 27. Typical $V_{BAT}$ current consumption (RTC ON / backup SRAM ON and LSE in Low drive mode)**



### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the informations given in this paragraph are based on characterization results obtained with typical external components specified in *Table 38*.

In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

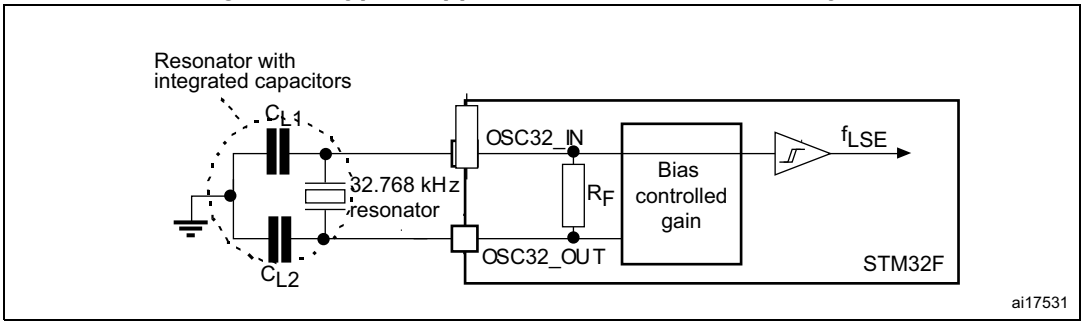
**Table 38. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor | - | - | 18.4 | - | MΩ |
| $I_{DD}$ | LSE current consumption | Low power mode(2) | - | - | 1 | µA |
| | | High drive mode(2) | - | - | 3 | |
| $ACC_{LSE}$(3) | LSE accuracy | - | − 500 | - | 500 | ppm |
| $G_m$_crit_max | Maximum critical crystal $g_m$ | Low power mode(2) | - | - | 0.56 | µA/V |
| | | High drive mode(2) | - | - | 1.5 | |
| $t_{SU(LSE)}$(4) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Guaranteed by design.
2. LSE mode cannot be changed “on the fly” otherwise, a glitch can be generated on OSCIN pin.
3. This parameter depends on the crystal used in the application. Refer to application note AN2867.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is based on characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

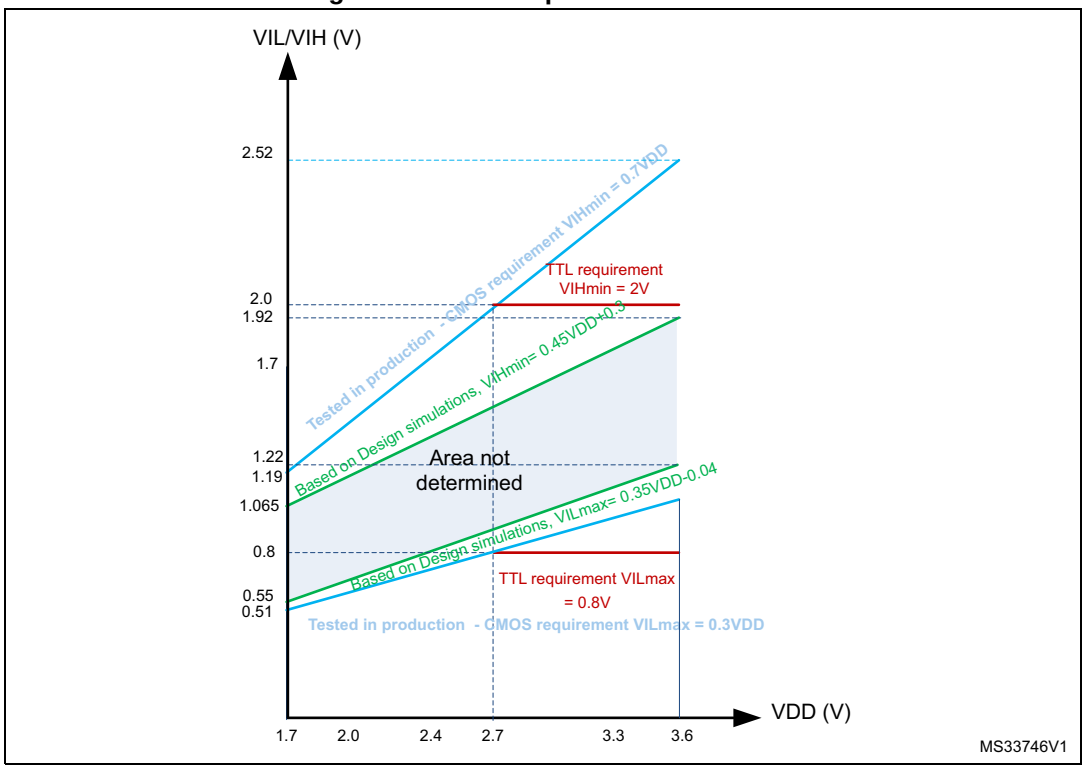
*Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from www.st.com.*

**Figure 32. Typical application with a 32.768 kHz crystal**



All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 39*.

**Figure 39. FT I/O input characteristics**




## Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed $V_{OL}/V_{OH}$) except PC13, PC14, PC15 and PI8 which can sink or source up to ±3mA. When using the PC13 to PC15 and PI8 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 15*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 15*).

### 5.3.21 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 58*).

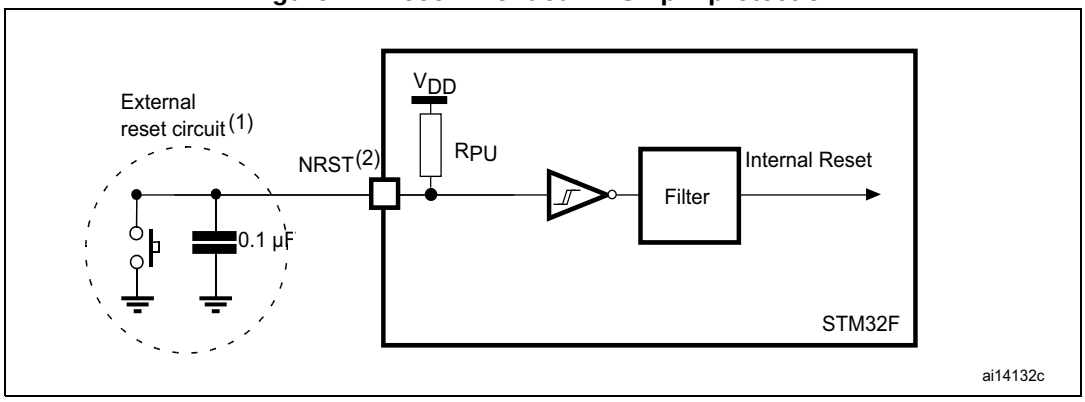
Unless otherwise specified, the parameters given in *Table 61* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

**Table 61. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Weak pull-up equivalent resistor(1) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$(2) | NRST Input filtered pulse | - | - | - | 100 | ns |
| $V_{NF(NRST)}$(2) | NRST Input not filtered pulse | $V_{DD} > 2.7$ V | 300 | - | - | |
| $T_{NRST\_OUT}$ | Generated reset pulse duration | Internal Reset source | 20 | - | - | µs |

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

**Figure 41. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 61*. Otherwise the reset is not taken into account by the device.

**Table 76. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 30 MHz 12-bit resolution | 0.50 | - | 16.40 | µs |
| | | $f_{ADC}$ = 30 MHz 10-bit resolution | 0.43 | - | 16.34 | |
| | | $f_{ADC}$ = 30 MHz 8-bit resolution | 0.37 | - | 16.27 | |
| | | $f_{ADC}$ = 30 MHz 6-bit resolution | 0.30 | - | 16.20 | |
| | | 9 to 492 ($t_S$ for sampling +n-bit resolution for successive approximation) | | | | $1/f_{ADC}$ |
| $f_S$(2) | Sampling rate ($f_{ADC}$ = 30 MHz, and $t_S$ = 3 ADC cycles) | 12-bit resolution Single ADC | - | - | 2 | Msps |
| | | 12-bit resolution Interleave Dual ADC mode | - | - | 3.75 | |
| | | 12-bit resolution Interleave Triple ADC mode | - | - | 6 | |
| $I_{VREF+}$(2) | ADC $V_{REF}$ DC current consumption in conversion mode | - | - | 300 | 500 | µA |
| $I_{VDDA}$(2) | ADC $V_{DDA}$ DC current consumption in conversion mode | - | - | 1.6 | 1.8 | mA |

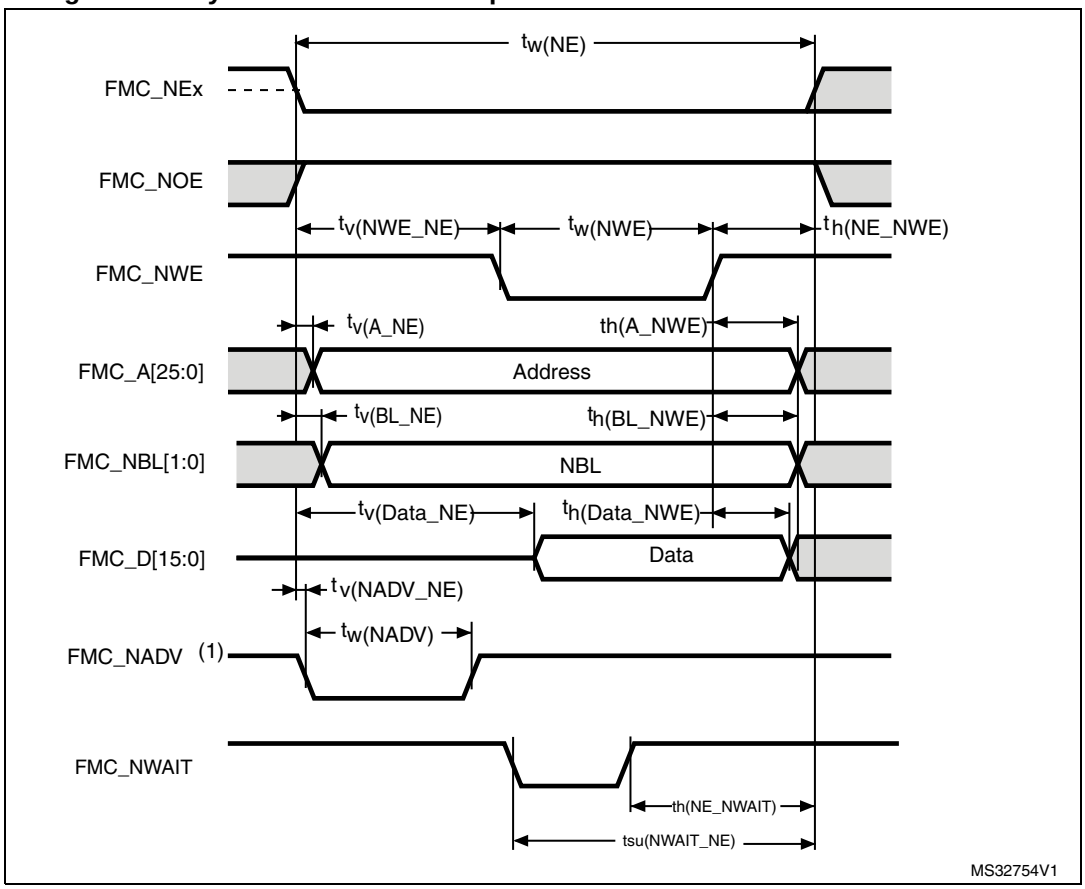
1. $V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.19.2*).
2. Based on test during characterization.
3. $V_{REF+}$ is internally connected to $V_{DDA}$ and $V_{REF-}$ is internally connected to $V_{SSA}$.
4. $R_{ADC}$ maximum value is given for $V_{DD}$=1.7 V, and minimum value for $V_{DD}$=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 76*.

**Equation 1: $R_{AIN}$ max formula**

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

**Figure 60. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms**




1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

**Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $3T_{HCLK}$ | $3T_{HCLK}+1$ | ns |
| $t_{v(NWE\_NE)}$ | FMC_NEx low to FMC_NWE low | $T_{HCLK} - 0.5$ | $T_{HCLK}+ 0.5$ | |
| $t_{w(NWE)}$ | FMC_NWE low time | $T_{HCLK}$ | $T_{HCLK}+ 0.5$ | |
| $t_{h(NE\_NWE)}$ | FMC_NWE high to FMC_NE high hold time | $T_{HCLK}$ +1.5 | - | |
| $t_{v(A\_NE)}$ | FMC_NEx low to FMC_A valid | - | 0 | |
| $t_{h(A\_NWE)}$ | Address hold time after FMC_NWE high | $T_{HCLK}$+0.5 | - | |
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 1.5 | |
| $t_{h(BL\_NWE)}$ | FMC_BL hold time after FMC_NWE high | $T_{HCLK}$+0.5 | - | |
| $t_{v(Data\_NE)}$ | Data to FMC_NEx low to Data valid | - | $T_{HCLK}+ 2$ | |
| $t_{h(Data\_NWE)}$ | Data hold time after FMC_NWE high | $T_{HCLK}$+0.5 | - | |
| $t_{v(NADV\_NE)}$ | FMC_NEx low to FMC_NADV low | - | 0.5 | |
| $t_{w(NADV)}$ | FMC_NADV low time | - | $T_{HCLK}+ 0.5$ | |

1. Based on test during characterization.

**Table 91. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $8T_{HCLK}+1$ | $8T_{HCLK}+2$ | ns |
| $t_{w(NWE)}$ | FMC_NWE low time | $6T_{HCLK}-1$ | $6T_{HCLK}+2$ | |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $6T_{HCLK}+1.5$ | - | |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK}+1$ | - | |

1. Based on test during characterization.

**Figure 61. Asynchronous multiplexed PSRAM/NOR read waveforms**

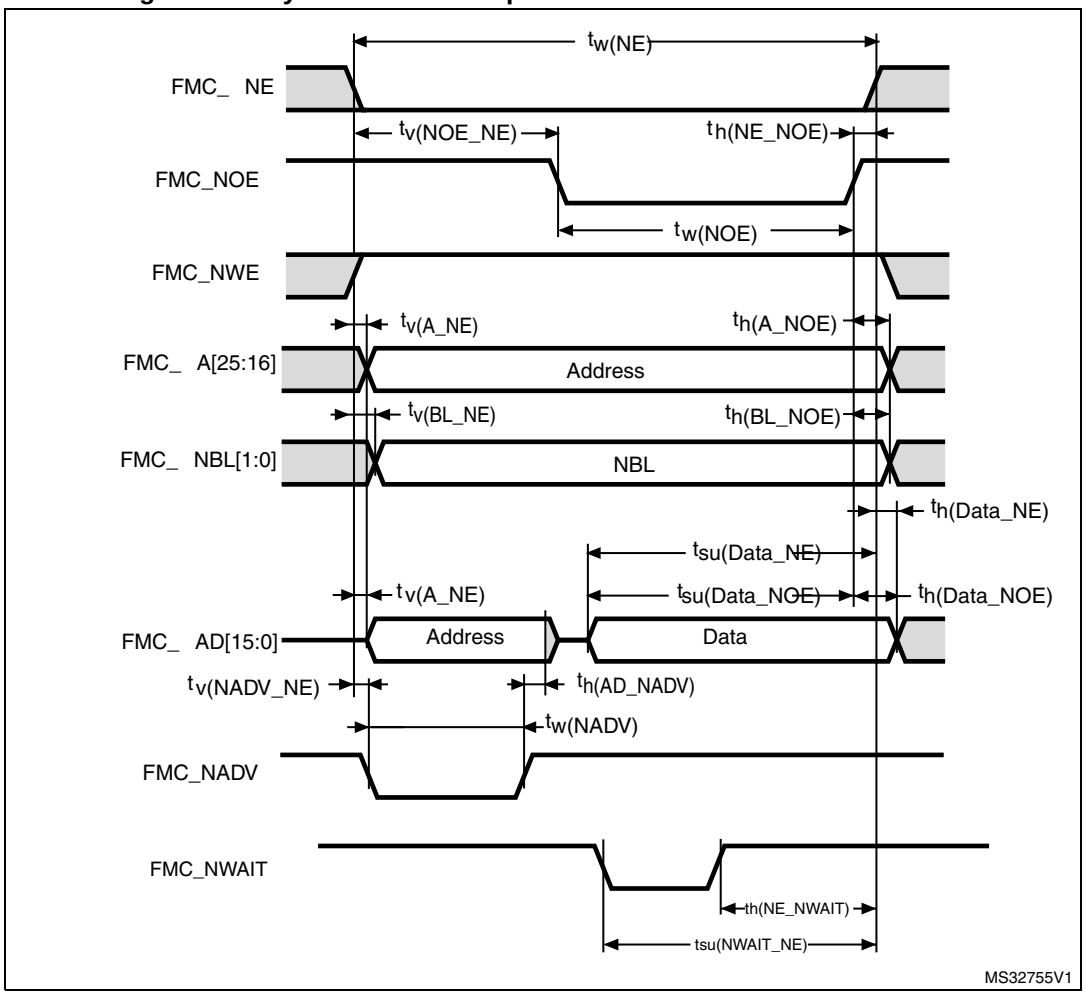


**Figure 68. NAND controller waveforms for write access**

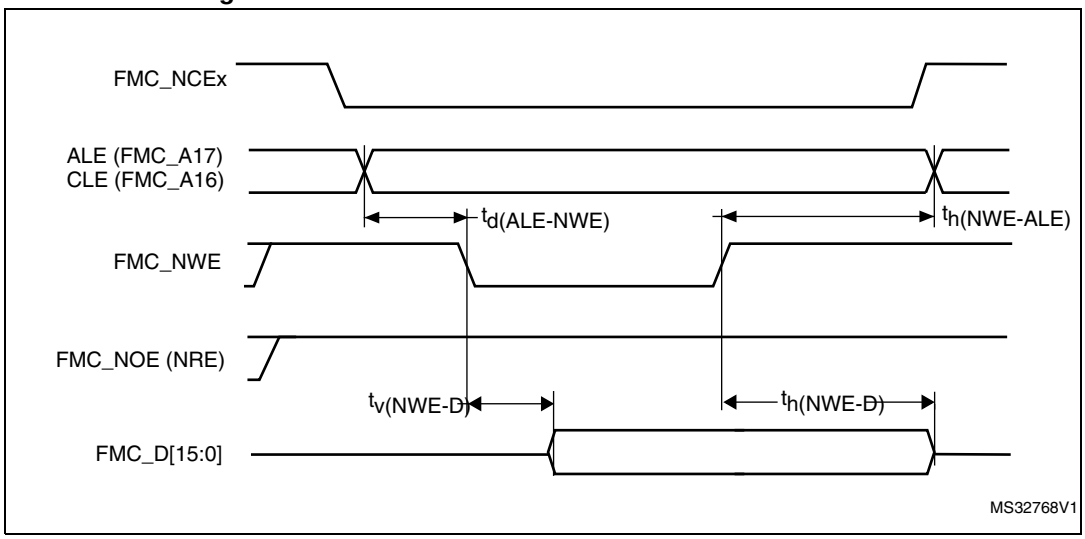
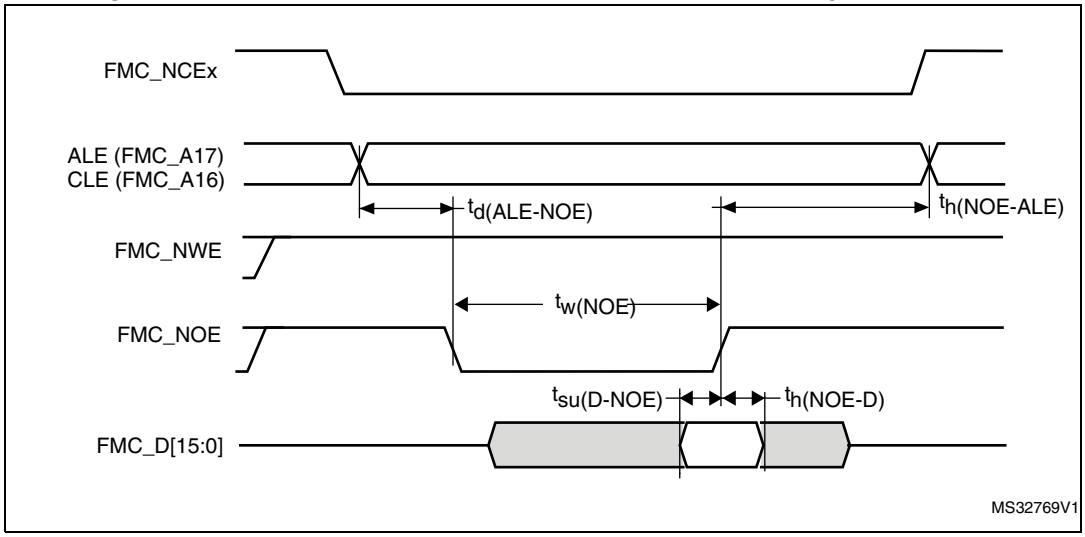



**Figure 69. NAND controller waveforms for common memory read access**

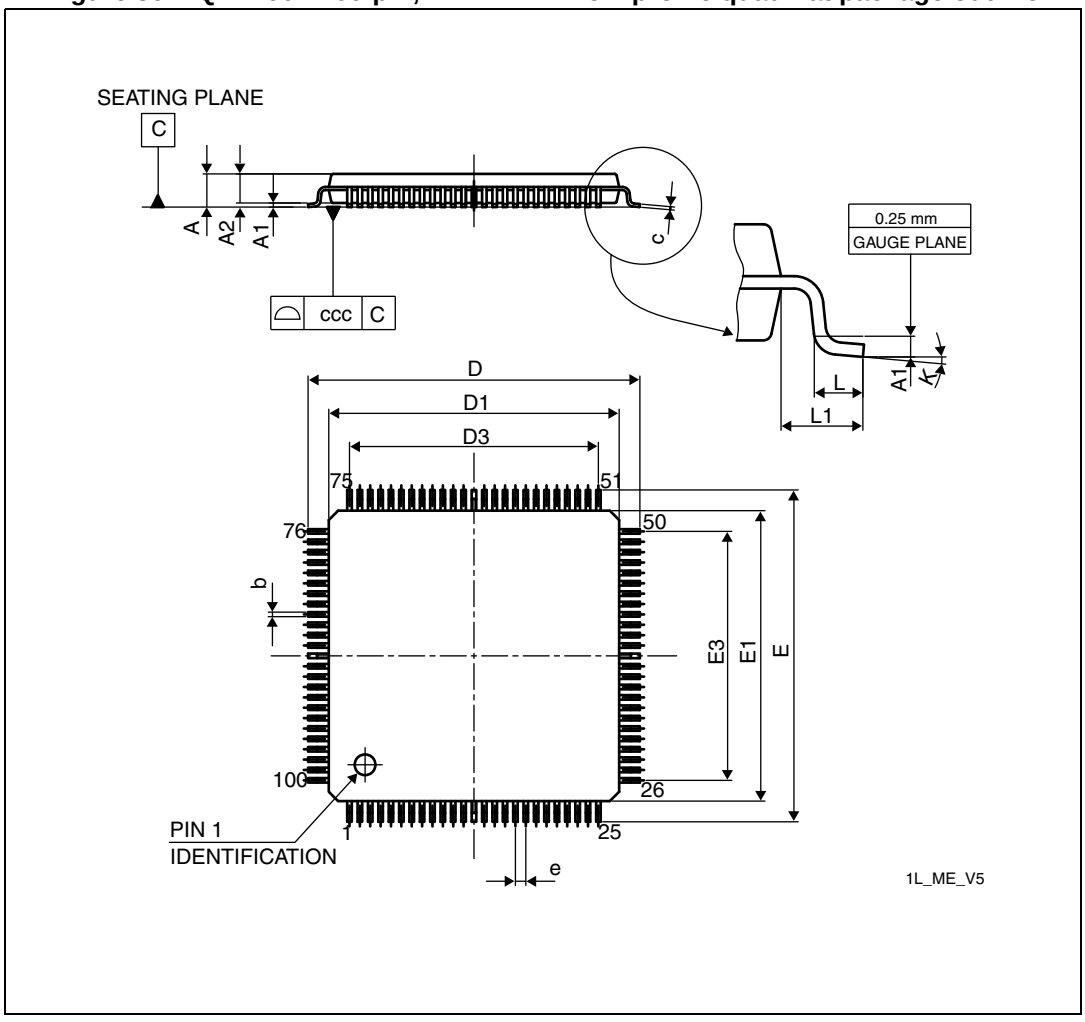


# 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

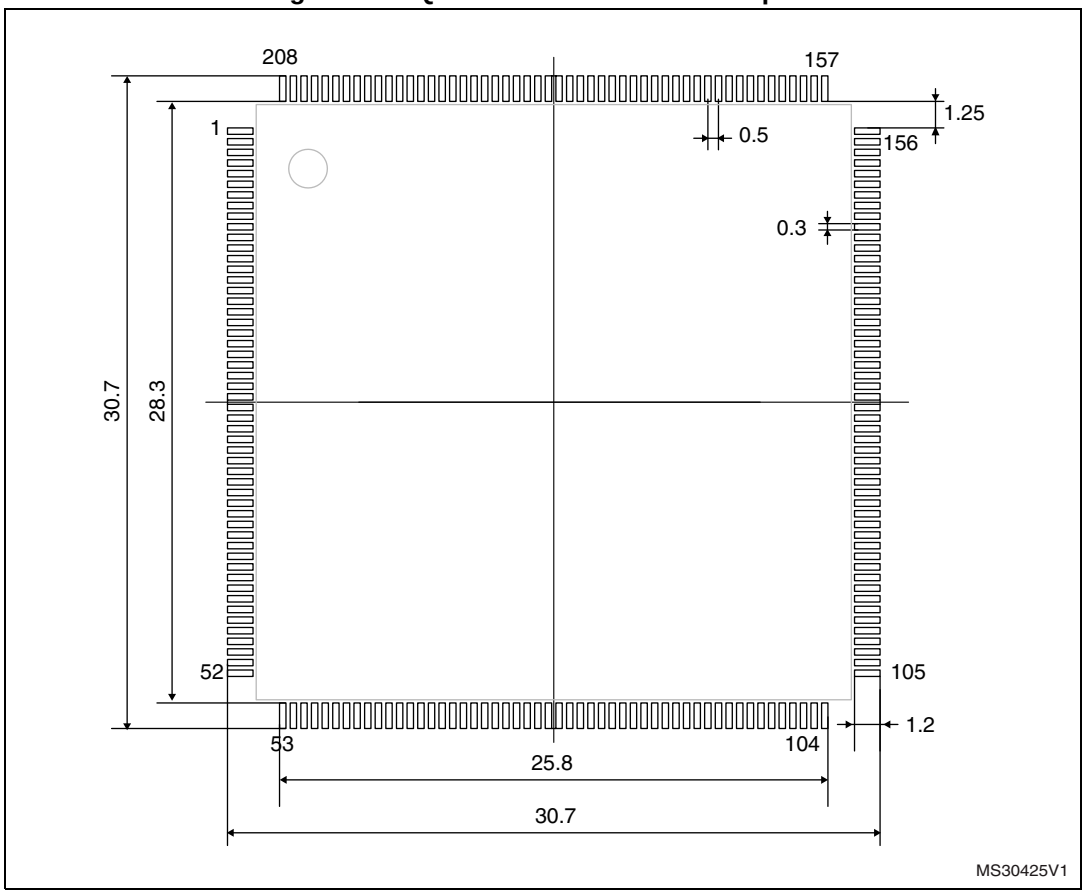
## 6.1 LQFP100 package information

**Figure 80. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline**




1. Drawing is not to scale.

**Figure 95. LQFP208 recommended footprint**




1. Dimensions are expressed in millimeters.