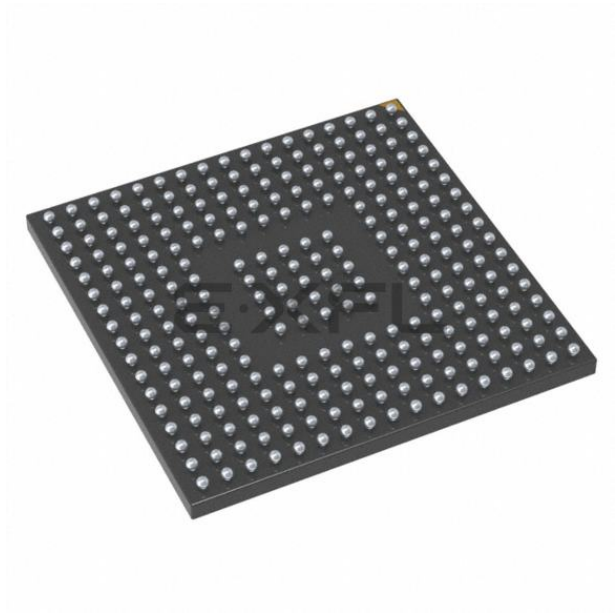

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f469ieh6

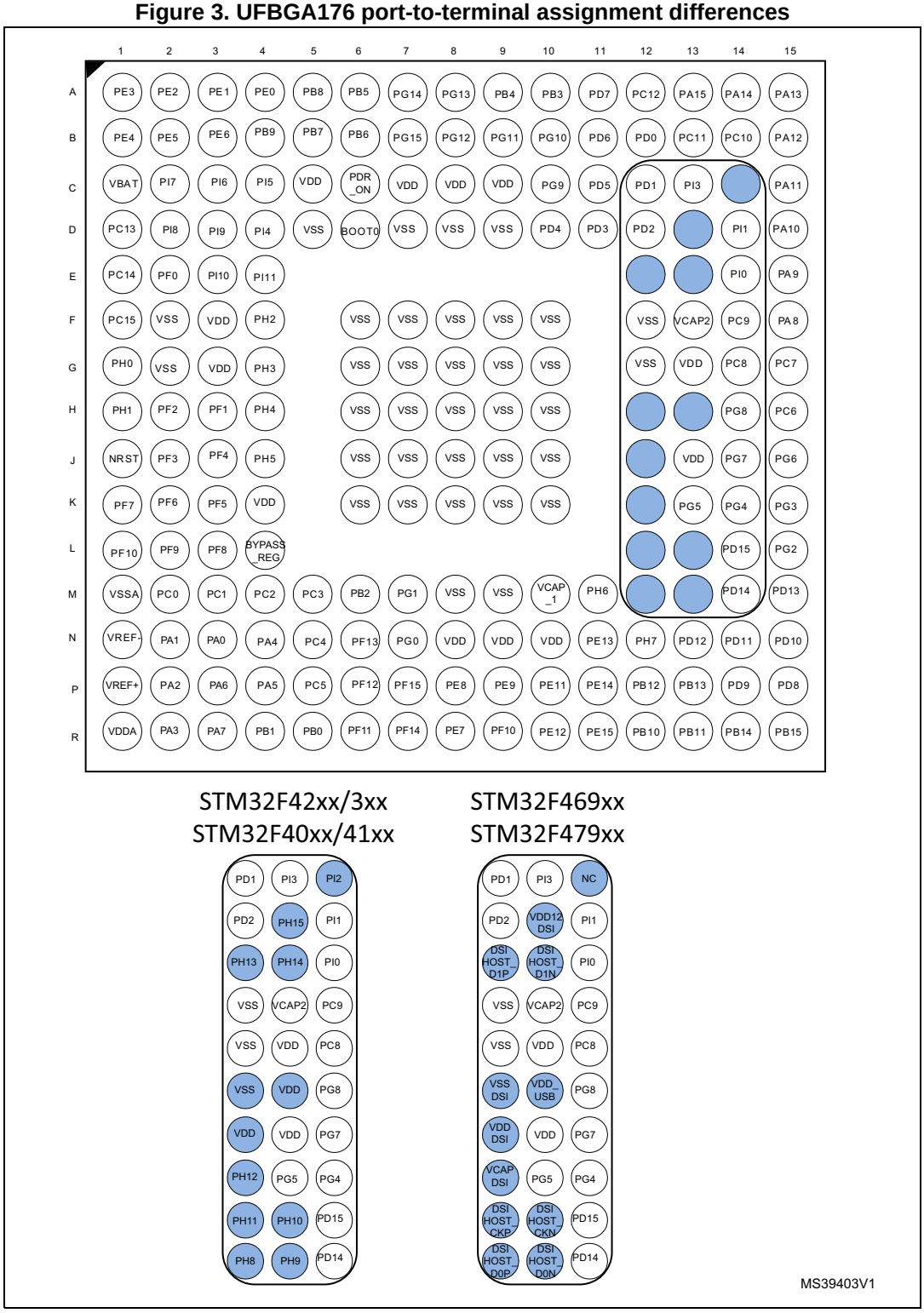
Table 2. STM32F469xx features and peripheral counts (continued)

Peripherals	STM32F469Vx	STM32F469Zx	STM32F469Ax	STM32F469Ix	STM32F469Bx	STM32F469Nx
MIPI-DSI Host	Yes					
LCD-TFT	Yes					
Chrom-ART Accelerator™ (DMA2D)	Yes					
GPIOs	71	106	114	131	161	161
12-bit ADC Number of channels	3					
	14	20	24	16	24	24
12-bit DAC Number of channels	Yes 2					
Maximum CPU frequency	180 MHz					
Operating voltage	1.7 to 3.6V(2)					
Operating temperatures	Ambient operating temperature: −40 to 85 °C / −40 to 105 °C Junction temperature: −40 to 105 °C / −40 to 125 °C					
Package	LQFP100	LQPF144	UFBGA169 WLCSP168	LQFP176 UFBGA176	LQFP208	TFBGA216

1. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
2. VDD/VDDA minimum value of 1.7 V is obtained when the internal reset is OFF (refer to *Section 2.19.2*).

1.1.3 UFBGA176 package

Figure 3. UFBGA176 port-to-terminal assignment differences



1. The highlighted pins are substituted with dedicated DSI IO pins on STM32F469xx/479xx devices.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep mode

    The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.
  - In Stop modes

    The MR can be configured in two ways during stop mode:

    MR operates in normal mode (default mode of MR in stop mode)

    MR operates in under-drive mode (reduced leakage mode).
- LPR is used in the Stop modes:

  The LP regulator mode is configured by software when entering Stop mode.

  Like the MR mode, the LPR can be configured in two ways during stop mode:
  - LPR operates in normal mode (default mode when LPR is ON)
  - LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to *Table 3* for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin. Refer to *Section 2.18* and *Table 124*.

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode(1)

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode(2)	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

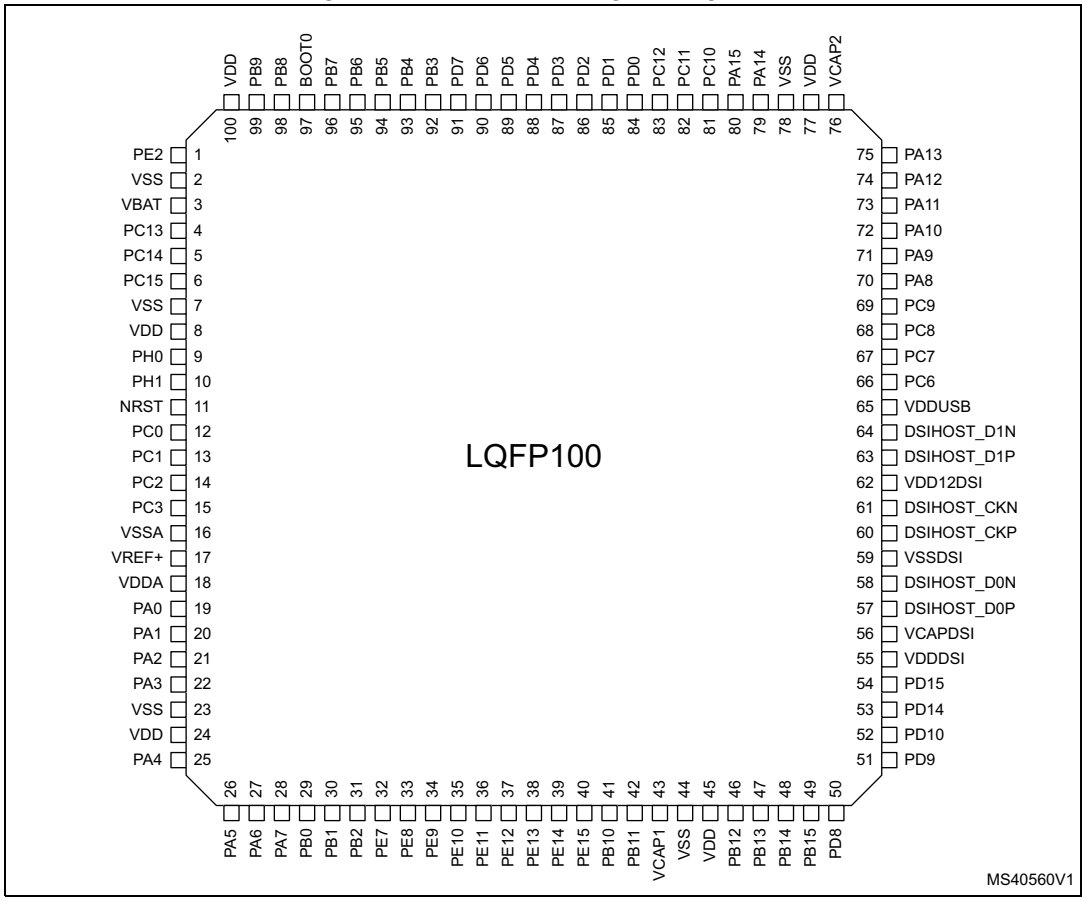
1. '-' means that the corresponding configuration is not available.
2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

2.20.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

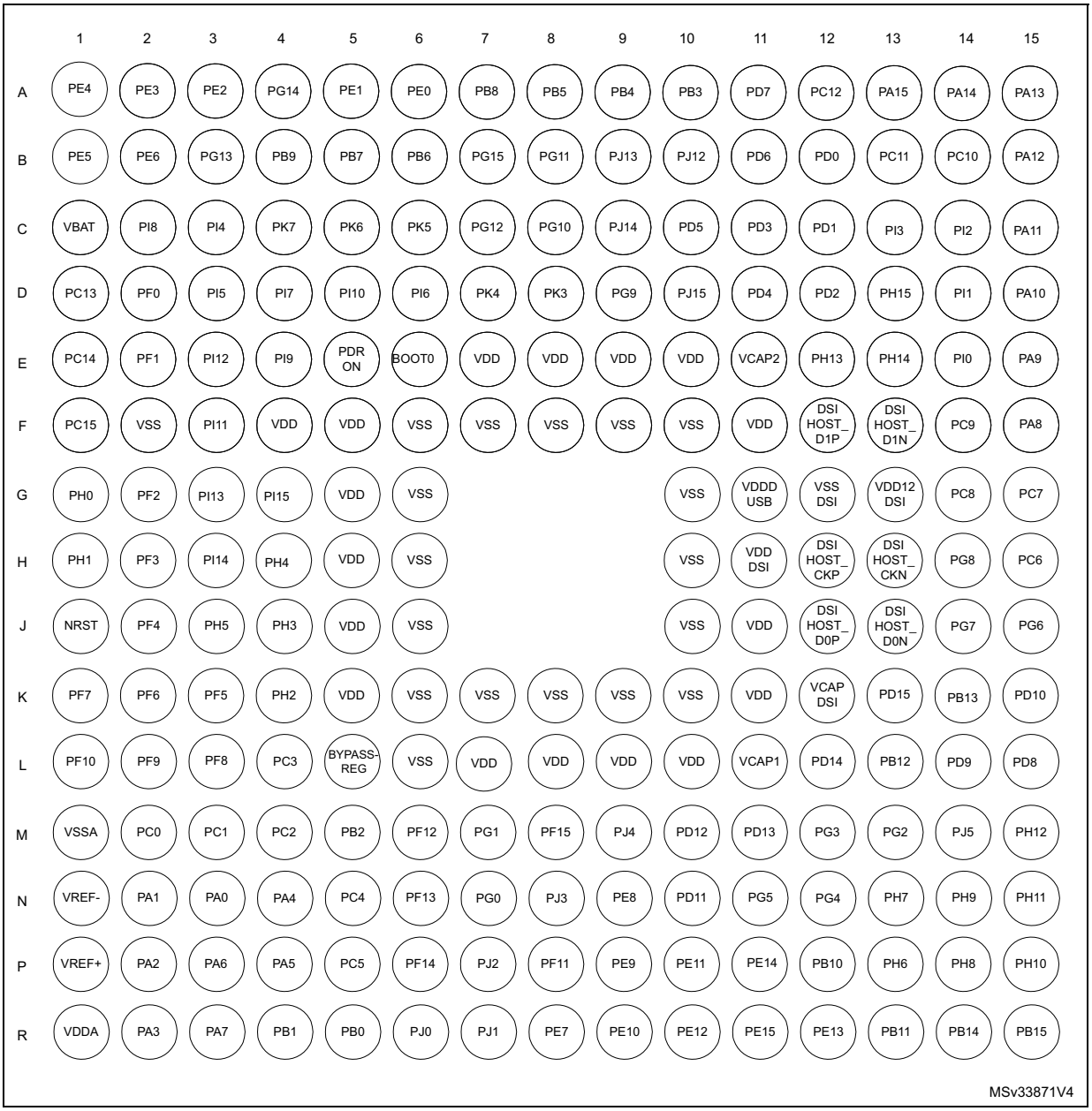
3 Pinouts and pin description

Figure 13. STM32F46x LQFP100 pinout



1. The above figure shows the package top view.

Figure 20. STM32F46x TFBGA216 ballout



1. The above figure shows the package top view.

Table 10. STM32F469xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	96	D13	G6	H14	116	135	H14	PG8	I/O	FT	-	SPI6_NSS, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	-	G9	F2	G12	117	136	G10	VSS	S	-	-	-	-
65	97	G11	F1	H13	118	137	G11	VDDUSB	S	-	-	-	-
66	98	F9	F3	H15	119	138	H15	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDIO_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
67	99	F10	G7	G15	120	139	G15	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDIO_D7, DCMI_D1, LCD_G6, EVENTOUT	-
68	100	E10	F4	G14	121	140	G14	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, USART6_CK, SDIO_D0, DCMI_D2, EVENTOUT	-
69	101	G10	F5	F14	122	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, QUADSPI_BK1_IO0, SDIO_D1, DCMI_D3, EVENTOUT	-
70	102	D8	E1	F15	123	142	F15	PA8	I/O	FT	-	MCO1, TIM1_CH1, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT	-
71	103	E8	E2	E15	124	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, EVENTOUT	OTG_FS_ VBUS
72	104	E9	E3	D15	125	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT	-
73	105	A13	F7	C15	126	145	C15	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-
74	106	A12	F6	B15	127	146	B15	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
75	107	A11	D1	A15	128	147	A15	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
76	108	D12	D2	F13	129	148	E11	VCAP2	S	-	-	-	-
-	109	D11	C1	F12	130	149	F10	VSS	S	-	-	-	-

Table 10. STM32F469xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
96	136	B4	A9	B5	165	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT	-
97	137	A5	F8	D6	166	197	E6	BOOT0	I	B	-	-	VPP
98	138	D4	B9	A5	167	198	A7	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDIO_D4, DCMI_D6, LCD_B6, EVENTOUT	-
99	139	C4	E9	B4	168	199	B4	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDIO_D5, DCMI_D7, LCD_B7, EVENTOUT	-
NC (2)	140	A4	A10	A4	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, UART8_Rx, FMC_NBL0, DCMI_D2, EVENTOUT	-
NC (2)	141	A3	C9	A3	170	201	A5	PE1	I/O	FT	-	UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	E3	B10	D5	-	202	F6	VSS	S	-	-	-	-
-	142	C3	D9	C6	171	203	E5	PDR_ON	S	-	-	-	-
100	143	D3	A11	C5	172	204	E7	VDD	S	-	-	-	-
-	-	B3	D10	D4	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	A2	C10	C4	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	A1	B11	C3	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	B1	A12	C2	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

1. **Function availability depends on the chosen device.**
2. NC (not-connected) pins are not bonded. They must be configured by software to output push-pull and forced to “0” in the output data register to avoid extra current consumption in low power modes.
3. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
4. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F4xx reference manual, available from the STMicroelectronics website: www.st.com.
5. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

Table 12. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSIHOST	LCD	SYS
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENTOUT
	PI1	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	FMC_D25	DCMI_D8	LCD_G6	EVENTOUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENTOUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	FMC_D27	DCMI_D10		EVENTOUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	-	FMC_NBL2	DCMI_D5	LCD_B4	EVENTOUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	-	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENTOUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	-	FMC_D28	DCMI_D6	LCD_B6	EVENTOUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	-	-	FMC_D29	DCMI_D7	LCD_B7	EVENTOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-		EVENTOUT
	PI9	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_D30	-	LCD_VSYNC	EVENTOUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RX_ER	FMC_D31	-	LCD_HSYNC	EVENTOUT
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-	-	-	-	EVENTOUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	EVENTOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENTOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENTOUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENT‘OUT

Table 36. Low-speed external user clock characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 29. High-speed external clock source AC timing diagram

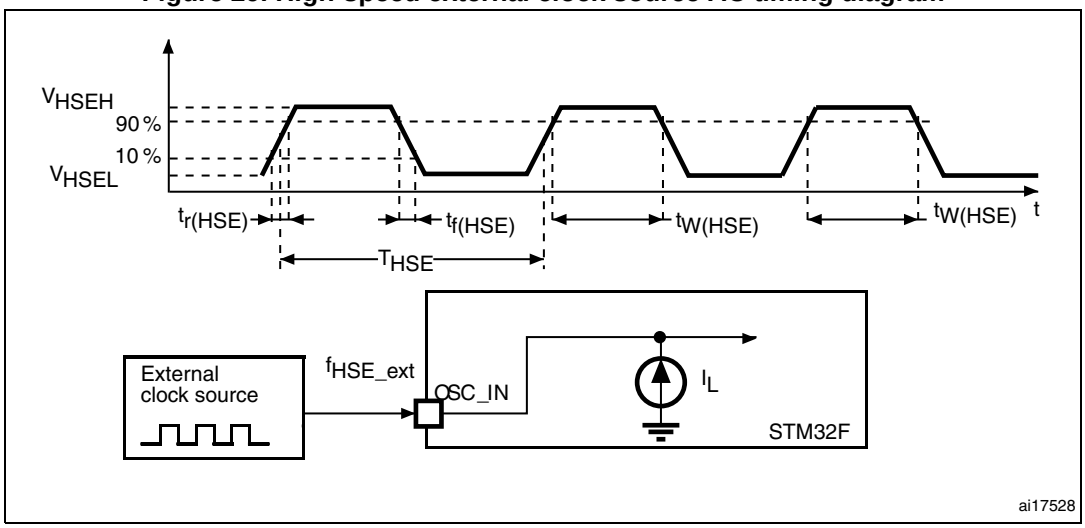
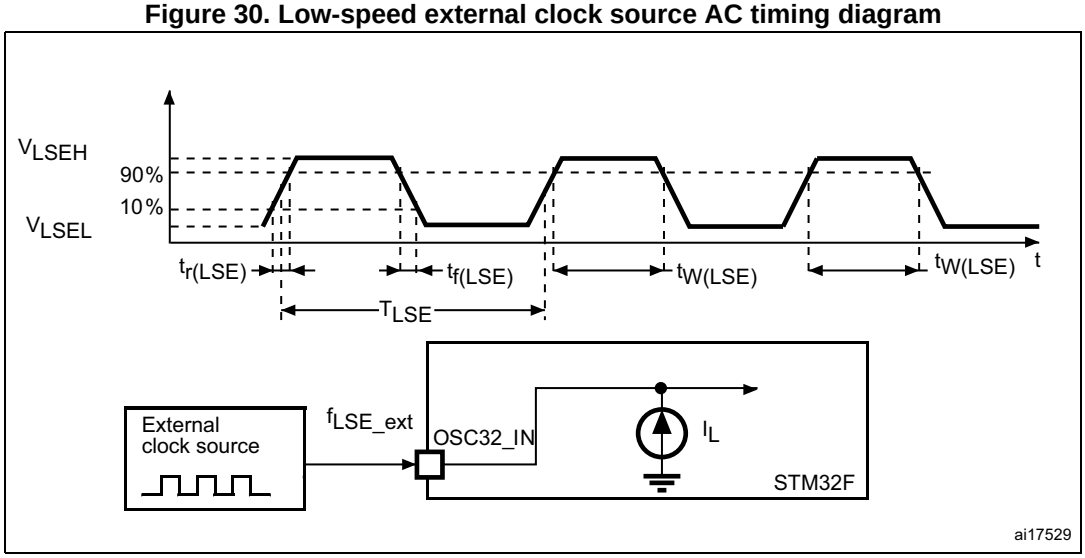


Figure 30. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

Figure 42. SPI timing diagram - slave mode and CPHA = 0

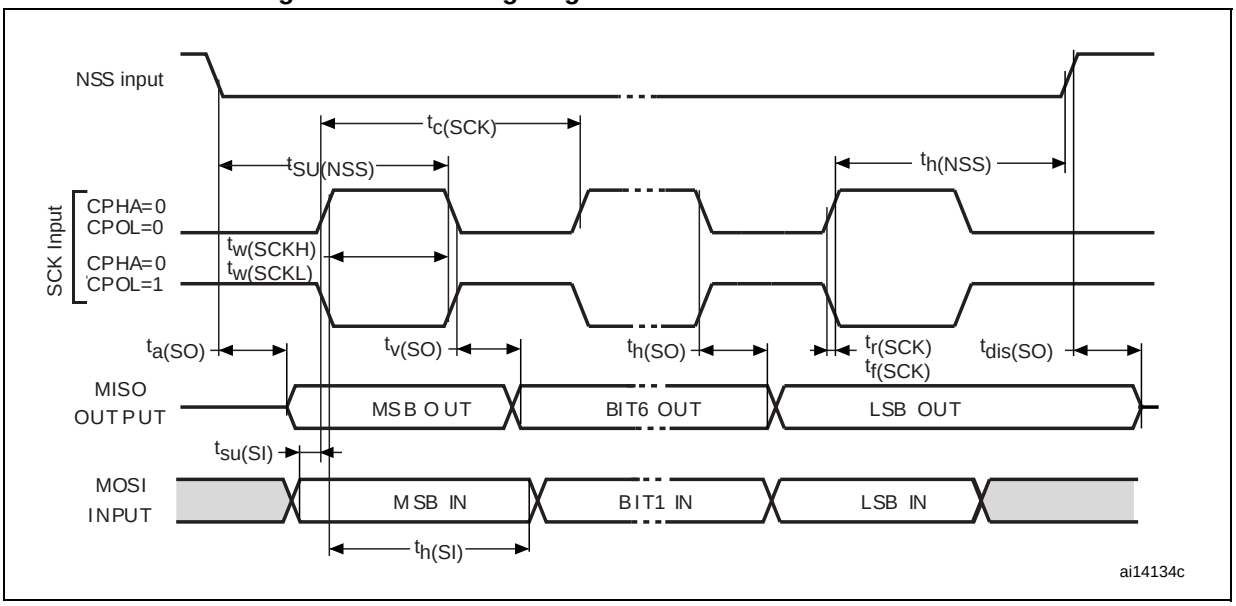


Figure 43. SPI timing diagram - slave mode and CPHA = 1(1)

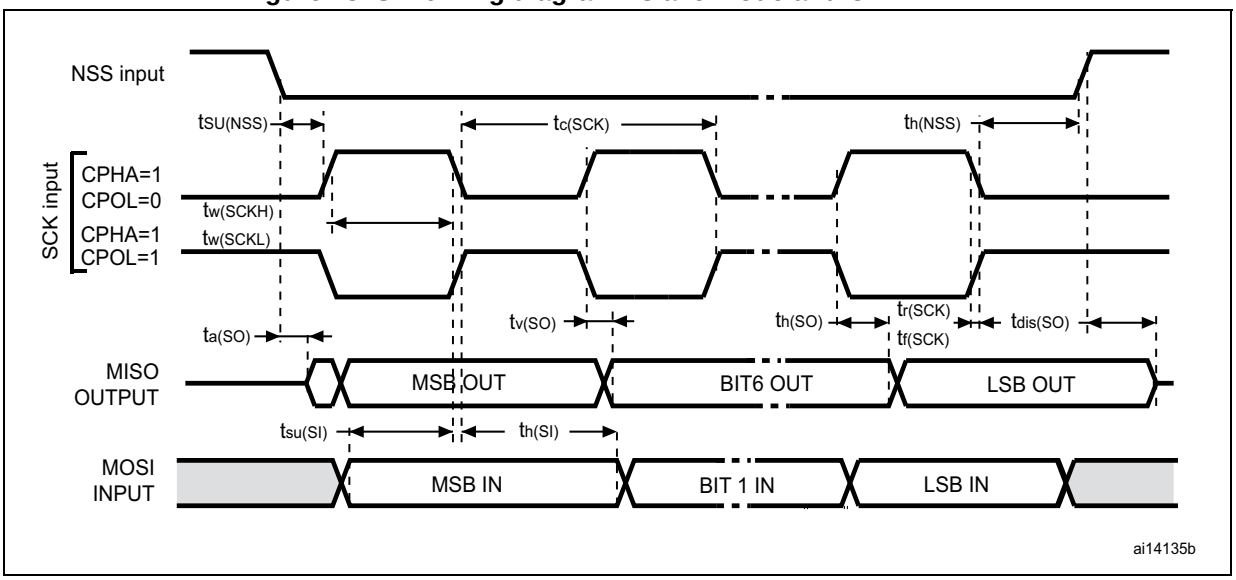


Table 77. ADC static accuracy at f_{ADC} = 18 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V V_{DDA} –V_{REF} < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Based on test during characterization.

Table 78. ADC static accuracy at f_{ADC} = 30 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V, V_{DDA} –V_{REF} < 1.2 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Based on test during characterization.

Table 79. ADC static accuracy at f_{ADC} = 36 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V V_{DDA} –V_{REF} < 1.2 V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

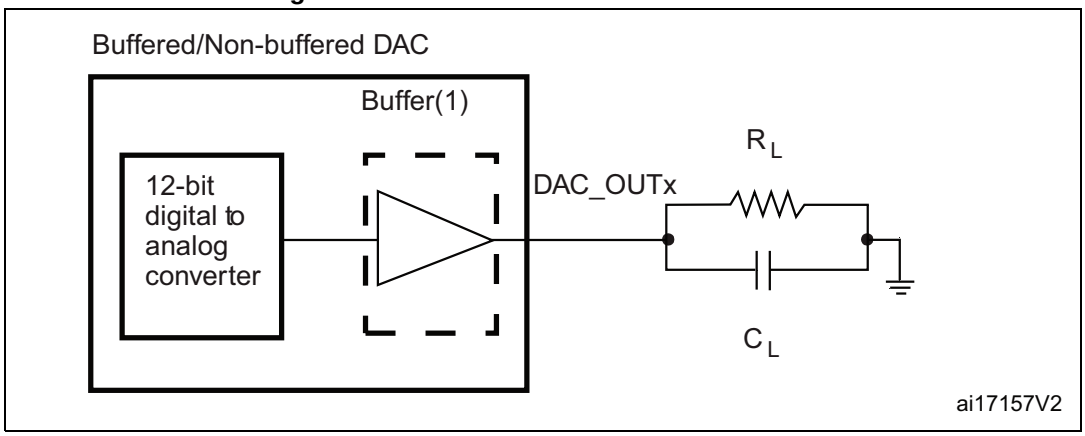
1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Based on test during characterization.

Table 87. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
I_{DDA}(4)	DAC DC VDDA current consumption in quiescent mode(3)	-	280	380	µA	With no load, middle code (0x800) on the inputs
		-	475	625	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(4)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(4)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset(4)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(4)	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(4)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB	-	3	6	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
THD(4)	Total Harmonic Distortion Buffer ON	-	-	-	dB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.19.2*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed based on test during characterization.

Figure 58. 12-bit buffered/non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.29 FMC characteristics

Unless otherwise specified, the parameters given in Tables *88* through *101* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.20* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figures *59* through *62* represent asynchronous waveforms, and Tables *88* through *95* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK} - 0.5$	$2\ T_{HCLK}+0.5$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK}$	$2T_{HCLK}+ 0.5$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} + 2.5$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	$T_{HCLK} +2$	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK} +1$	

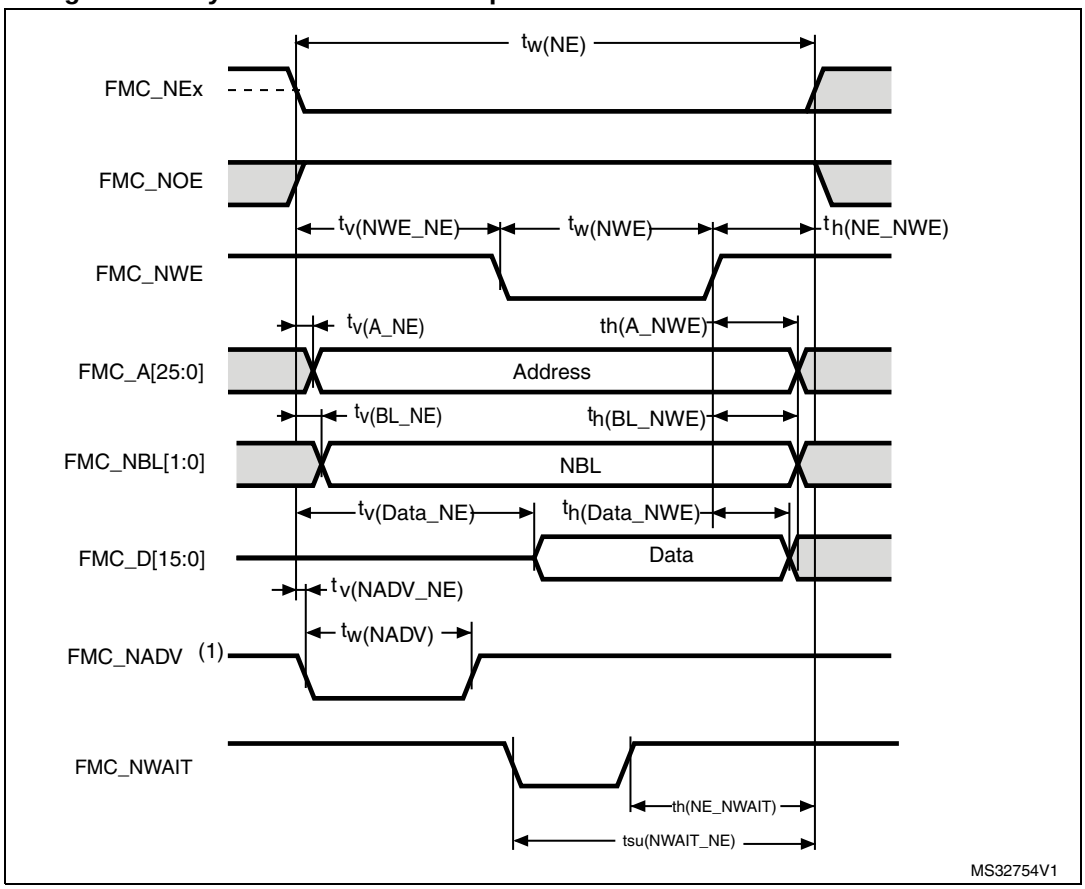
1. Based on test during characterization.

Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{HCLK}+0.5$	$7T_{HCLK}+1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1.5$	$5T_{HCLK} +2$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}+1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$	-	

1. Based on test during characterization.

Figure 60. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+1$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK}+ 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}	$T_{HCLK}+ 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK} +1.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}+0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	T_{HCLK}+0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{HCLK}+ 2$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	T_{HCLK}+0.5	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK}+ 0.5$	

1. Based on test during characterization.

Table 92. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK} - 1$	$3T_{HCLK}+0.5$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK} - 0.5$	$2T_{HCLK}$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{HCLK} - 1$	$T_{HCLK}+1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	1	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	2	
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK}+0.5$	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high)	0	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$T_{HCLK} - 0.5$	-	
$t_{h(BL\_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK}+1.5$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	$T_{HCLK}+1$	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Based on test during characterization.

Table 93. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}+0.5$	$8T_{HCLK}+2$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1$	$5T_{HCLK} +1.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK} +1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$	-	

1. Based on test during characterization.

NAND controller waveforms and timings

Figures *67* through *70* represent synchronous waveforms, and *Table 100* and *Table 101* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;
- Capacitive load C_L = 30 pF.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 67. NAND controller waveforms for read access

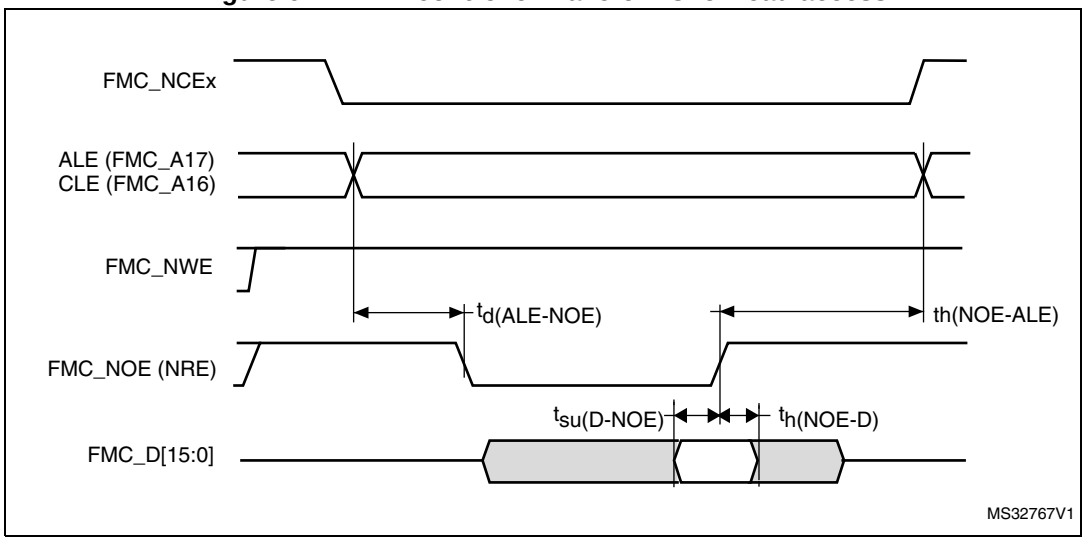


Figure 70. NAND controller waveforms for common memory write access

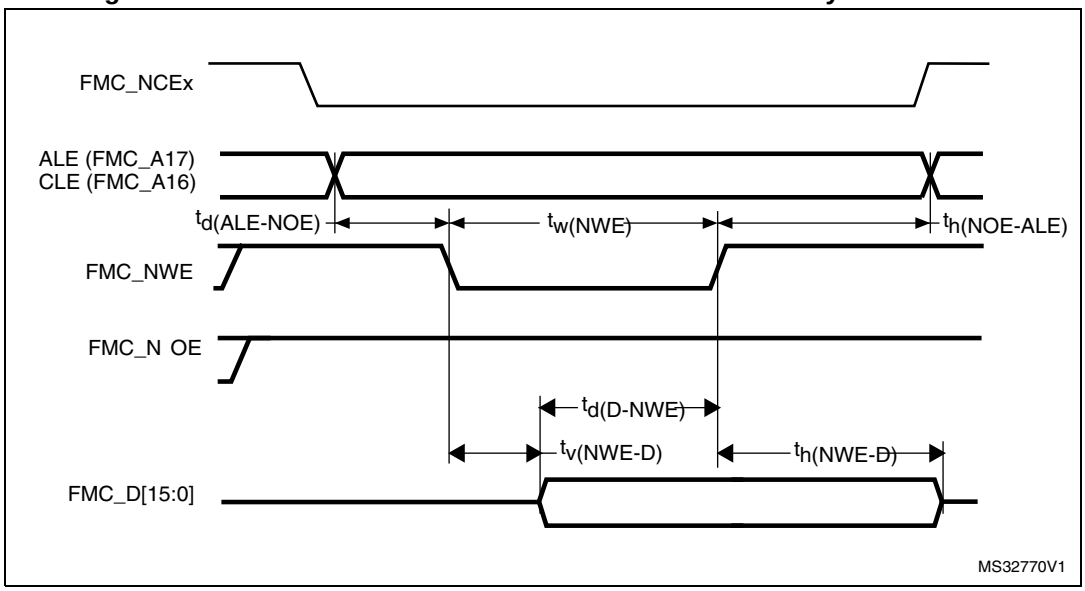


Table 100. Switching characteristics for NAND Flash read cycles

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK} - 0.5$	$4T_{HCLK}+0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	9	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{HCLK} - 0.5$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{HCLK} - 2$	-	

Table 101. Switching characteristics for NAND Flash write cycles

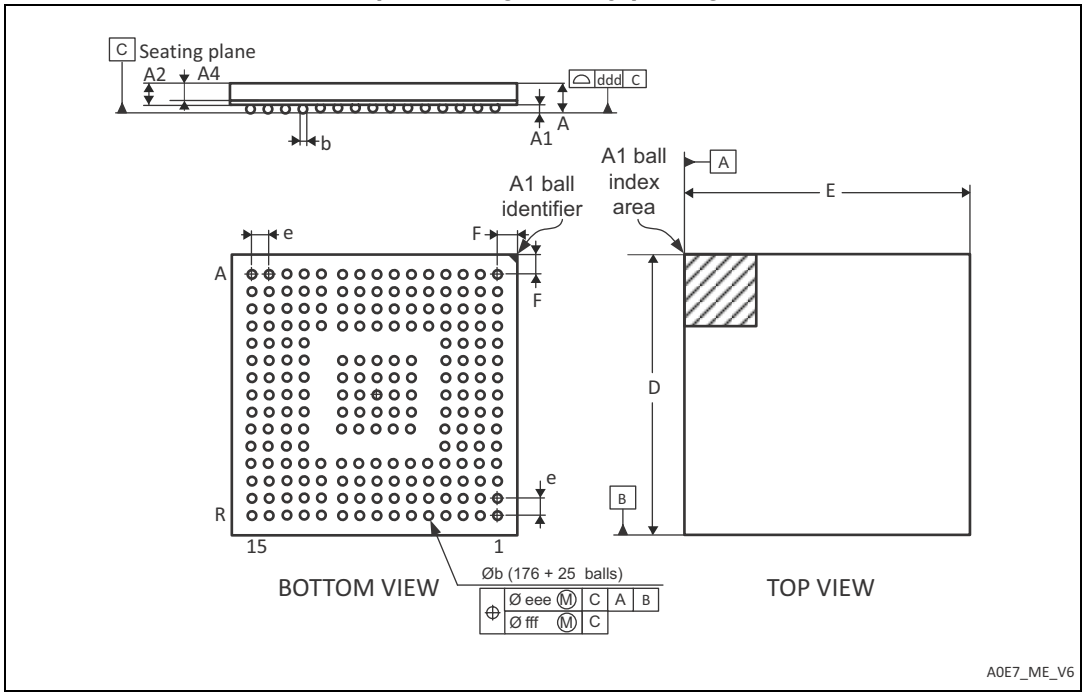
Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{HCLK}$	$4T_{HCLK}+1$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$3T_{HCLK} - 1$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK} - 3$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{HCLK}-0.5$	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{HCLK} - 1$	-	

SDRAM waveforms and timings

- C_L = 30 pF on data and address lines.
- C_L = 10 pF on FMC_SDCLK unless otherwise specified.

6.6 UFBGA176+25 package information

Figure 92. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 118. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3917	0.3937	0.3957
E	9.950	10.000	10.050	0.3917	0.3937	0.3957
e	-	0.650	-	-	0.0256	-
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.