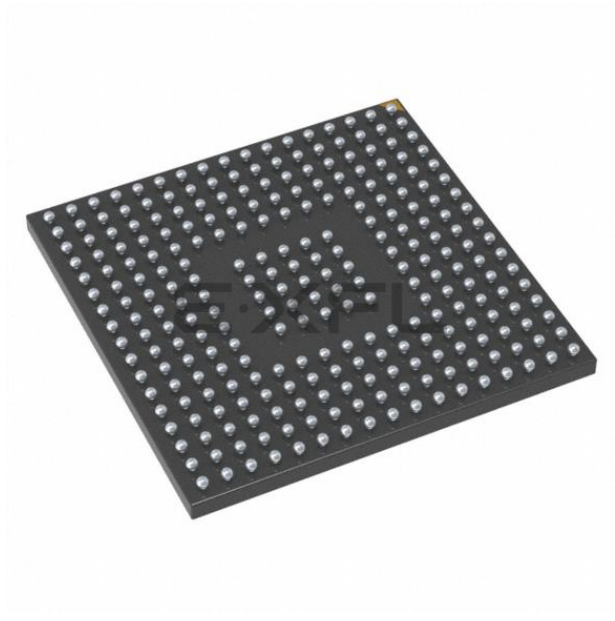

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 180MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 114 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 384K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 201-UFBGA |
| Supplier Device Package | 176+25UFBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f469igh6 |

# 1 Description

The STM32F469xx devices are based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 180 MHz. The Cortex®-M4 core features a Floating point unit (FPU) single precision which supports all ARM® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F469xx devices incorporate high-speed embedded memories (Flash memory up to 2 Mbytes, up to 384 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, and a true random number generator (RNG). They also feature standard and advanced communication interfaces:

- Up to three $I^2C$s
- Six SPIs, two $I^2S$s full duplex. To achieve audio class accuracy, the $I^2S$ peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- One SAI serial audio interface
- An SDMMC host interface
- Ethernet and camera interface
- LCD-TFT display controller
- Chrom-ART Accelerator™
- DSI Host.

Advanced peripherals include an SDMMC interface, a flexible memory control (FMC) interface, a Quad-SPI Flash memory, and camera interface for CMOS sensors. Refer to *Table 2* for the list of peripherals available on each part number.

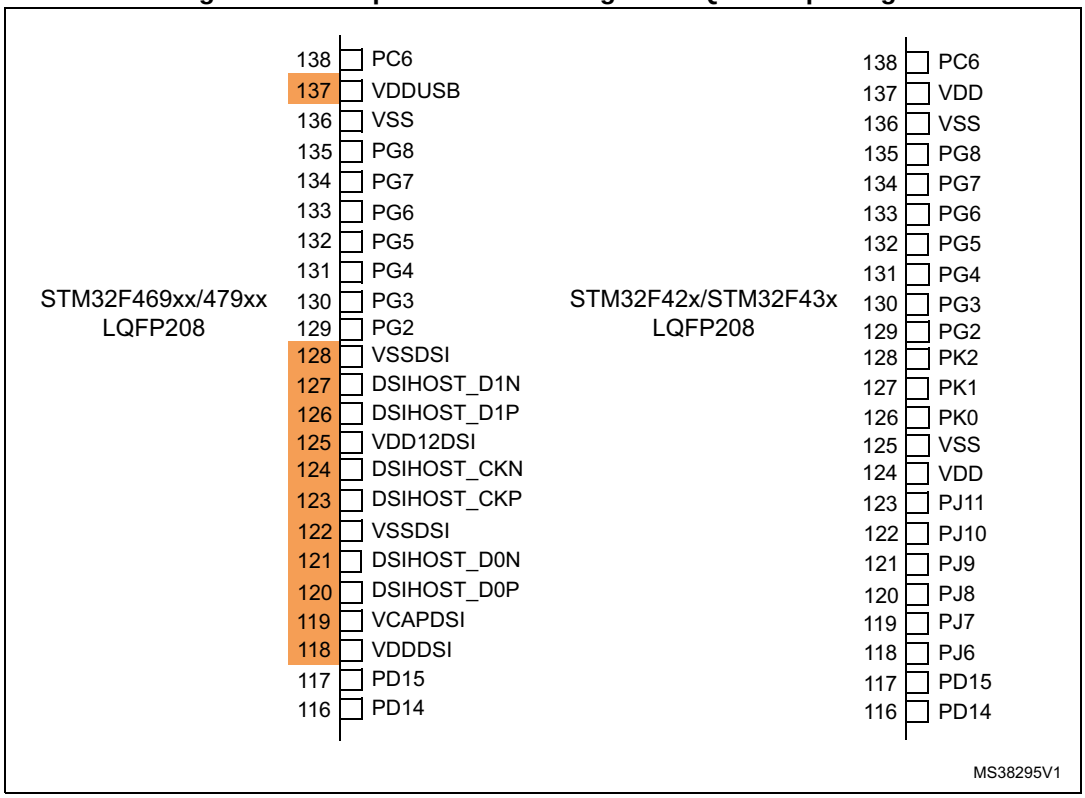
The STM32F469xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. A dedicated supply input for USB (OTG_FS and OTG_HS) only in full speed mode, is available on all packages.

The supply voltage can drop to 1.7 V (refer to *Section 2.19.2*). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F469xx devices are offered in eight packages, ranging from 100 to 216 pins. The set of included peripherals changes with the device chosen, according to *Table 2*.

### 1.1.2 LQFP208 package

**Figure 2. Incompatible board design for LQFP208 package**




1. Pins from 118 to 128 and pin 137 are not compatible

The major features are:

- Combined Rx and Tx FIFO size of 4 KB with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

## 2.37 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image black & white.

## 2.38 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

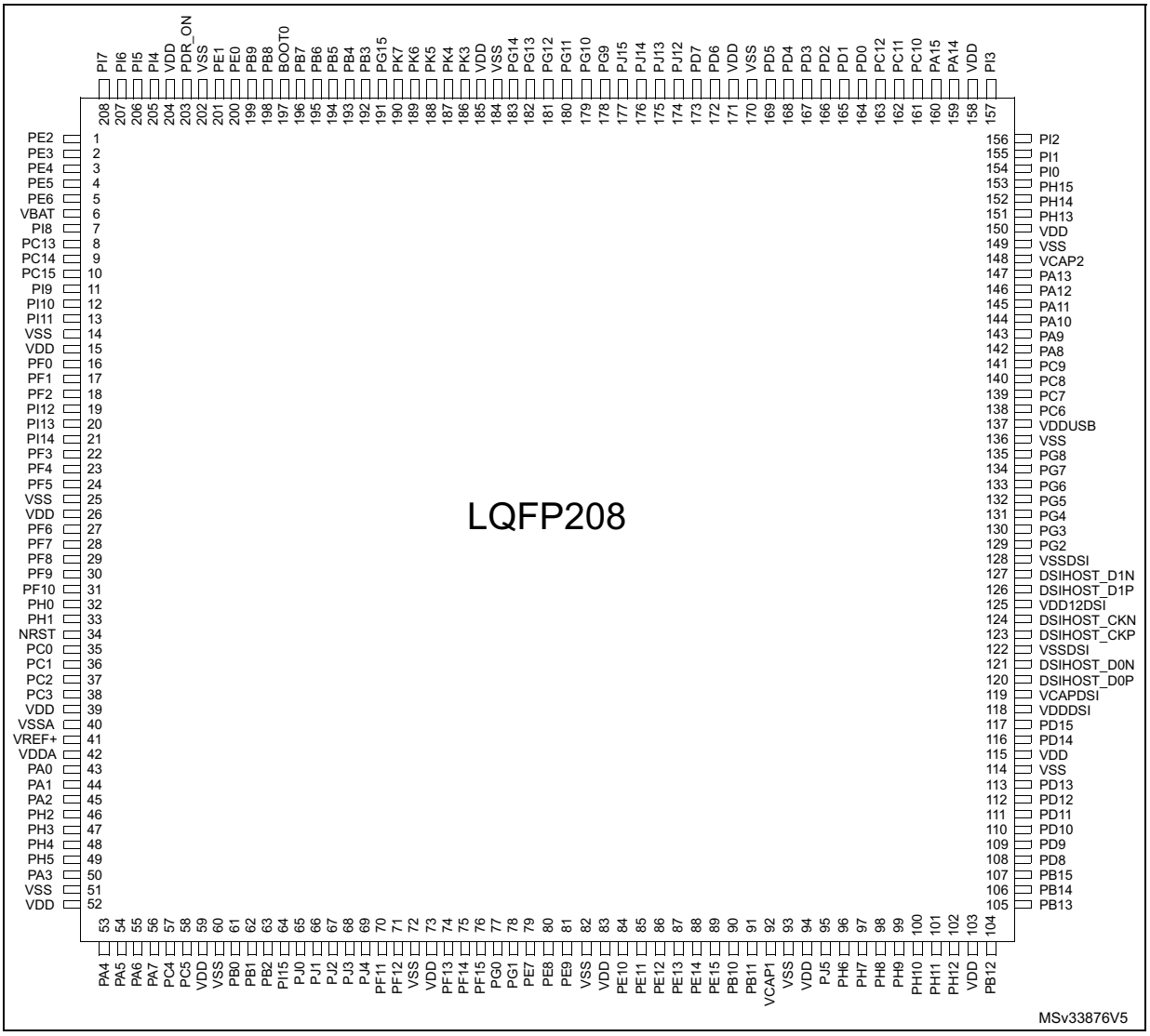
## 2.39 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 90 MHz.

**Figure 19. STM32F46x LQFP208 pinout**




1. The above figure shows the package top view.

**Table 10. STM32F469xx pin and ball definitions**

| Pin number | | | | | | | | Pin name (function after reset)[1] | Pin types | I/O structures | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP144 | UFBGA169 | WLCSP168 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| 1 | 144 | B2 | F9 | A2 | 1 | 1 | A3 | PE2 | I/O | FT | - | TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT | - |
| NC (2) | 1 | C1 | E10 | A1 | 2 | 2 | A2 | PE3 | I/O | FT | - | TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT | - |
| NC (2) | 2 | C2 | C11 | B1 | 3 | 3 | A1 | PE4 | I/O | FT | - | TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT | - |
| NC (2) | 3 | D1 | B12 | B2 | 4 | 4 | B1 | PE5 | I/O | FT | - | TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT | - |
| NC (2) | 4 | D2 | D11 | B3 | 5 | 5 | B2 | PE6 | I/O | FT | - | TRACED3, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT | - |
| 2 | - | - | - | - | - | - | G6 | VSS | S | - | - | - | - |
| - | - | - | - | - | - | - | F5 | VDD | S | - | - | - | - |
| 3 | 5 | E5 | C12 | C1 | 6 | 6 | C1 | VBAT | S | - | - | - | - |
| - | - | - | - | D2 | 7 | 7 | C2 | PI8 | I/O | FT | (3) (4) | EVENTOUT | RTC_TAMP1/ RTC_TAMP2/ RTC_TS |
| 4 | 6 | G4 | D12 | D1 | 8 | 8 | D1 | PC13 | I/O | FT | (3) (4) | EVENTOUT | RTC_TAMP1/ RTC_TS/ RTC_OUT |
| 5 | 7 | E1 | E11 | E1 | 9 | 9 | E1 | PC14-OSC32_IN (PC14) | I/O | FT | (3) (4) | EVENTOUT | OSC32_IN |
| 6 | 8 | F1 | E12 | F1 | 10 | 10 | F1 | PC15-OSC32_OUT (PC15) | I/O | FT | (3) (4) | EVENTOUT | OSC32_OUT |
| - | - | - | - | - | - | - | G5 | VDD | S | - | - | - | - |
| - | - | E2 | G9 | D3 | 11 | 11 | E4 | PI9 | I/O | FT | | CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT | - |
| - | - | E4 | F10 | E3 | 12 | 12 | D5 | PI10 | I/O | FT | | ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT | - |
| - | - | F2 | F11 | E4 | 13 | 13 | F3 | PI11 | I/O | FT | | LCD_G6, OTG_HS_ULPI_DIR, EVENTOUT | - |
| - | - | F5 | F12 | F2 | 14 | 14 | F2 | VSS | S | - | - | - | - |
| - | - | F4 | G11 | F3 | 15 | 15 | F4 | VDD | S | - | - | - | - |

Table 10. STM32F469xx pin and ball definitions (continued)

| Pin number | | | | | | | | Pin name (function after reset)(1) | Pin types | I/O structures | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP144 | UFBGA169 | WLCSP168 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | 9 | F3 | G10 | E2 | 16 | 16 | D2 | PF0 | I/O | FT | | I2C2_SDA, FMC_A0, EVENTOUT | - |
| - | 10 | G3 | H10 | H3 | 17 | 17 | E2 | PF1 | I/O | FT | | I2C2_SCL, FMC_A1, EVENTOUT | - |
| - | 11 | G5 | G12 | H2 | 18 | 18 | G2 | PF2 | I/O | FT | | I2C2_SMBA, FMC_A2, EVENTOUT | - |
| - | - | - | - | - | - | 19 | E3 | PI12 | I/O | FT | | LCD_HSYNC, EVENTOUT | - |
| - | - | - | - | - | - | 20 | G3 | PI13 | I/O | FT | | LCD_VSYNC, EVENTOUT | - |
| - | - | - | - | - | - | 21 | H3 | PI14 | I/O | FT | | LCD_CLK, EVENTOUT | - |
| - | 12 | H4 | H11 | J2 | 19 | 22 | H2 | PF3 | I/O | FT | (5) | FMC_A3, EVENTOUT | ADC3_IN9 |
| - | 13 | L4 | J10 | J3 | 20 | 23 | J2 | PF4 | I/O | FT | (5) | FMC_A4, EVENTOUT | ADC3_IN14 |
| - | 14 | H3 | H12 | K3 | 21 | 24 | K3 | PF5 | I/O | FT | (5) | FMC_A5, EVENTOUT | ADC3_IN15 |
| 7 | 15 | G7 | J11 | G2 | 22 | 25 | H6 | VSS | S | - | - | - | - |
| 8 | 16 | G8 | J12 | G3 | 23 | 26 | H5 | VDD | S | - | - | - | - |
| - | - | - | - | K2 | 24 | 27 | K2 | PF6 | I/O | FT | (5) | TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_Rx, QUADSPI_BK1_IO3, EVENTOUT | ADC3_IN4 |
| - | - | - | - | K1 | 25 | 28 | K1 | PF7 | I/O | FT | (5) | TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_Tx, QUADSPI_BK1_IO2, EVENTOUT | ADC3_IN5 |
| - | - | - | - | L3 | 26 | 29 | L3 | PF8 | I/O | FT | (5) | SPI5_MISO, SAI1_SCK_B, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT | ADC3_IN6 |
| - | - | - | - | L2 | 27 | 30 | L2 | PF9 | I/O | FT | (5) | SPI5_MOSI, SAI1_FS_B, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT | ADC3_IN7 |
| - | 17 | H1 | K10 | L1 | 28 | 31 | L1 | PF10 | I/O | FT | (5) | QUADSPI_CLK, DCMI_D11, LCD_DE, EVENTOUT | ADC3_IN8 |
| 9 | 18 | G2 | K11 | G1 | 29 | 32 | G1 | PH0-OSC_IN (PH0) | I/O | FT | - | EVENTOUT | OSC_IN |
| 10 | 19 | G1 | K12 | H1 | 30 | 33 | H1 | PH1-OSC_OUT (PH1) | I/O | FT | - | EVENTOUT | OSC_OUT |
| 11 | 20 | H2 | H9 | J1 | 31 | 34 | J1 | NRST | I/O | RST | - | | |
| 12 | 21 | M1 | J9 | M2 | 32 | 35 | M2 | PC0 | I/O | FT | (5) | OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT | ADC123_ IN10 |

**Table 10. STM32F469xx pin and ball definitions (continued)**

| Pin number | | | | | | | | Pin name (function after reset)(1) | Pin types | I/O structures | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP144 | UFBGA169 | WLCSP168 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | 96 | D13 | G6 | H14 | 116 | 135 | H14 | PG8 | I/O | FT | - | SPI6_NSS, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT | - |
| - | - | G9 | F2 | G12 | 117 | 136 | G10 | VSS | S | - | - | - | - |
| 65 | 97 | G11 | F1 | H13 | 118 | 137 | G11 | VDDUSB | S | - | - | - | - |
| 66 | 98 | F9 | F3 | H15 | 119 | 138 | H15 | PC6 | I/O | FT | - | TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDIO_D6, DCMI_D0, LCD_HSYNC, EVENTOUT | - |
| 67 | 99 | F10 | G7 | G15 | 120 | 139 | G15 | PC7 | I/O | FT | - | TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDIO_D7, DCMI_D1, LCD_G6, EVENTOUT | - |
| 68 | 100 | E10 | F4 | G14 | 121 | 140 | G14 | PC8 | I/O | FT | - | TRACED1, TIM3_CH3, TIM8_CH3, USART6_CK, SDIO_D0, DCMI_D2, EVENTOUT | - |
| 69 | 101 | G10 | F5 | F14 | 122 | 141 | F14 | PC9 | I/O | FT | - | MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, QUADSPI_BK1_IO0, SDIO_D1, DCMI_D3, EVENTOUT | - |
| 70 | 102 | D8 | E1 | F15 | 123 | 142 | F15 | PA8 | I/O | FT | - | MCO1, TIM1_CH1, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT | - |
| 71 | 103 | E8 | E2 | E15 | 124 | 143 | E15 | PA9 | I/O | FT | - | TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, EVENTOUT | OTG_FS_ VBUS |
| 72 | 104 | E9 | E3 | D15 | 125 | 144 | D15 | PA10 | I/O | FT | - | TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT | - |
| 73 | 105 | A13 | F7 | C15 | 126 | 145 | C15 | PA11 | I/O | FT | - | TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT | - |
| 74 | 106 | A12 | F6 | B15 | 127 | 146 | B15 | PA12 | I/O | FT | - | TIM1_ETR, USART1_RTS, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT | - |
| 75 | 107 | A11 | D1 | A15 | 128 | 147 | A15 | PA13(JTMS-SWDIO) | I/O | FT | - | JTMS-SWDIO, EVENTOUT | - |
| 76 | 108 | D12 | D2 | F13 | 129 | 148 | E11 | VCAP2 | S | - | - | - | - |
| - | 109 | D11 | C1 | F12 | 130 | 149 | F10 | VSS | S | - | - | - | - |

Table 11. FMC pin definition

| Pin name | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND16 | SDRAM |
|---|---|---|---|---|
| PF0 | A0 | - | - | A0 |
| PF1 | A1 | - | - | A1 |
| PF2 | A2 | - | - | A2 |
| PF3 | A3 | - | - | A3 |
| PF4 | A4 | - | - | A4 |
| PF5 | A5 | - | - | A5 |
| PF12 | A6 | - | - | A6 |
| PF13 | A7 | - | - | A7 |
| PF14 | A8 | - | - | A8 |
| PF15 | A9 | - | - | A9 |
| PG0 | A10 | - | - | A10 |
| PG1 | A11 | - | - | A11 |
| PG2 | A12 | - | - | A12 |
| PG3 | A13 | - | - | |
| PG4 | A14 | - | - | BA0 |
| PG5 | A15 | - | - | BA1 |
| PD11 | A16 | A16 | CLE | - |
| PD12 | A17 | A17 | ALE | - |
| PD13 | A18 | A18 | - | - |
| PE3 | A19 | A19 | - | - |
| PE4 | A20 | A20 | - | - |
| PE5 | A21 | A21 | - | - |
| PE6 | A22 | A22 | - | - |
| PE2 | A23 | A23 | - | - |
| PG13 | A24 | A24 | - | - |
| PG14 | A25 | A25 | - | - |
| PD14 | D0 | DA0 | D0 | D0 |
| PD15 | D1 | DA1 | D1 | D1 |
| PD0 | D2 | DA2 | D2 | D2 |
| PD1 | D3 | DA3 | D3 | D3 |
| PE7 | D4 | DA4 | D4 | D4 |
| PE8 | D5 | DA5 | D5 | D5 |
| PE9 | D6 | DA6 | D6 | D6 |
| PE10 | D7 | DA7 | D7 | D7 |
| PE11 | D8 | DA8 | D8 | D8 |

**Table 12. Alternate function (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/2/3 | SPI1/2/3/4/5/6 | SPI2/3/SAI1 | SPI2/3/USART1/2/3 | USART6/UART4/5/7/8 | CAN1/2/TIM12/13/14/QUADSPI/LCD | QUADSPI/OTG2_HS/OTG1_FS | ETH | FMC/SDIO/OTG2_FS | DCMI/DSI HOST | LCD | SYS |
| Port D | PD0 | - | - | - | - | - | - | - | - | - | CAN1_RX | - | - | FMC_D2 | - | - | EVENTOUT |
| | PD1 | - | - | - | - | - | - | - | - | - | CAN1_TX | - | - | FMC_D3 | - | - | EVENTOUT |
| | PD2 | TRACED2 | - | TIM3_ETR | - | - | - | - | - | UART5_RX | - | - | - | SDIO_CMD | DCMI_D11 | - | EVENTOUT |
| | PD3 | - | - | - | - | - | SPI2_SCK/I2S2_CK | - | USART2_CTS | - | - | - | - | FMC_CLK | DCMI_D5 | LCD_G7 | EVENTOUT |
| | PD4 | - | - | - | - | - | - | - | USART2_RTS | - | - | - | - | FMC_NOE | - | - | EVENTOUT |
| | PD5 | - | - | - | - | - | - | - | USART2_TX | - | - | - | - | FMC_NWE | - | - | EVENTOUT |
| | PD6 | - | - | - | - | - | SPI3_MOSI/I2S3_SD | SAI1_SD_A | USART2_RX | - | - | - | - | FMC_NWAIT | DCMI_D10 | LCD_B2 | EVENTOUT |
| | PD7 | - | - | - | - | - | - | - | USART2_CK | - | - | - | - | FMC_NE1 | - | - | EVENTOUT |
| | PD8 | - | - | - | - | - | - | - | USART3_TX | - | - | - | - | FMC_D13 | - | - | EVENTOUT |
| | PD9 | - | - | - | - | - | - | - | USART3_RX | - | - | - | - | FMC_D14 | - | - | EVENTOUT |
| | PD10 | - | - | - | - | - | - | - | USART3_CK | - | - | - | - | FMC_D15 | - | LCD_B3 | EVENTOUT |
| | PD11 | - | - | - | - | - | - | - | USART3_CTS | - | QUADSPI_BK1_IO0 | - | - | FMC_A16/FMC_CLE | - | - | EVENTOUT |
| | PD12 | - | - | TIM4_CH1 | - | - | - | - | USART3_RTS | - | QUADSPI_BK1_IO1 | - | - | FMC_A17/FMC_ALE | - | - | EVENTOUT |
| | PD13 | - | - | TIM4_CH2 | - | - | - | - | - | - | QUADSPI_BK1_IO3 | - | - | FMC_A18 | - | - | EVENTOUT |
| | PD14 | - | - | TIM4_CH3 | - | - | - | - | - | - | - | - | - | FMC_D0 | - | - | EVENTOUT |
| | PD15 | - | - | TIM4_CH4 | - | - | - | - | - | - | - | - | - | FMC_D1 | - | - | EVENT‘OUT |

**Table 15. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ | Total current into sum of all $V_{DD\_x}$ power lines (source)(1) | 290 | mA |
| $\Sigma I_{VSS}$ | Total current out of sum of all $V_{SS\_x}$ ground lines (sink)(1) | − 290 | |
| $\Sigma I_{VDDUSB}$ | Total current into $V_{DDUSB}$ power line (source) | 25 | |
| $I_{VDD}$ | Maximum current into each $V_{DD\_x}$ power line (source)(1) | 100 | |
| $I_{VSS}$ | Maximum current out of each $V_{SS\_x}$ ground line (sink)(1) | − 100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current sourced by any I/Os and control pin | − 25 | |
| $\Sigma I_{IO}$ | Total output current sunk by sum of all I/O and control pins (2) | 120 | |
| | Total output current sunk by sum of all USB I/Os | 25 | |
| | Total output current sourced by sum of all I/Os and control pins(2) | − 120 | |
| $I_{INJ(PIN)}$ (3) | Injected current on FT pins (4) | − 5/+0 | |
| | Injected current on NRST and BOOT0 pins (4) | | |
| | Injected current on TTa pins(5) | ±5 | |
| $\Sigma I_{INJ(PIN)}$(5) | Total injected current (sum of all I/O and control pins)(6) | ±25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.24*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 14* for the values of the maximum allowed input voltage.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 16. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | − 65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 125 | °C |

**Table 25. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled), regulator ON**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in RUN mode | All Peripherals enabled(2)(3) | 168 | 97 | 102 | 128 | 154 | mA |
| | | | 150 | 87 | 92 | 118 | 143 | |
| | | | 144 | 80 | 84 | 108 | 131 | |
| | | | 120 | 65 | 68 | 88 | 108 | |
| | | | 90 | 51 | 54 | 73 | 93 | |
| | | | 60 | 37 | 41 | 59 | 79 | |
| | | | 30 | 21 | 23 | 42 | 62 | |
| | | | 25 | 18 | 20 | 39 | 59 | |
| | | All Peripherals disabled | 168 | 49 | 55 | 79 | 105 | |
| | | | 150 | 44 | 49 | 44 | 100 | |
| | | | 144 | 40 | 45 | 68 | 92 | |
| | | | 120 | 36 | 39 | 58 | 78 | |
| | | | 90 | 29 | 32 | 51 | 71 | |
| | | | 60 | 22 | 25 | 44 | 64 | |
| | | | 30 | 13 | 15 | 34 | 54 | |
| | | | 25 | 11 | 13 | 32 | 52 | |

1. Guaranteed based on test during characterization.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

**Table 36. Low-speed external user clock characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | - | - | 5 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle | - | 30 | - | 70 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design.

**Figure 29. High-speed external clock source AC timing diagram**

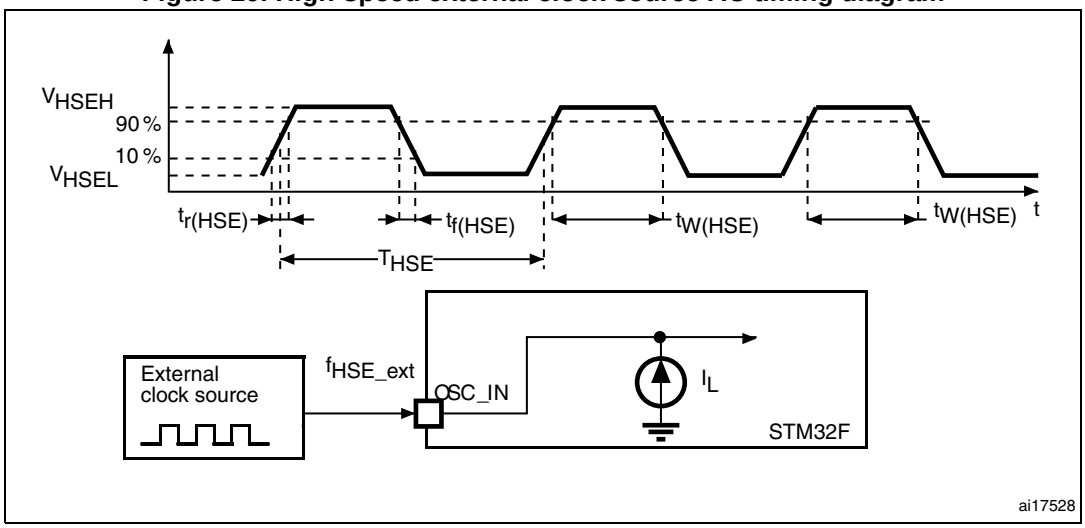
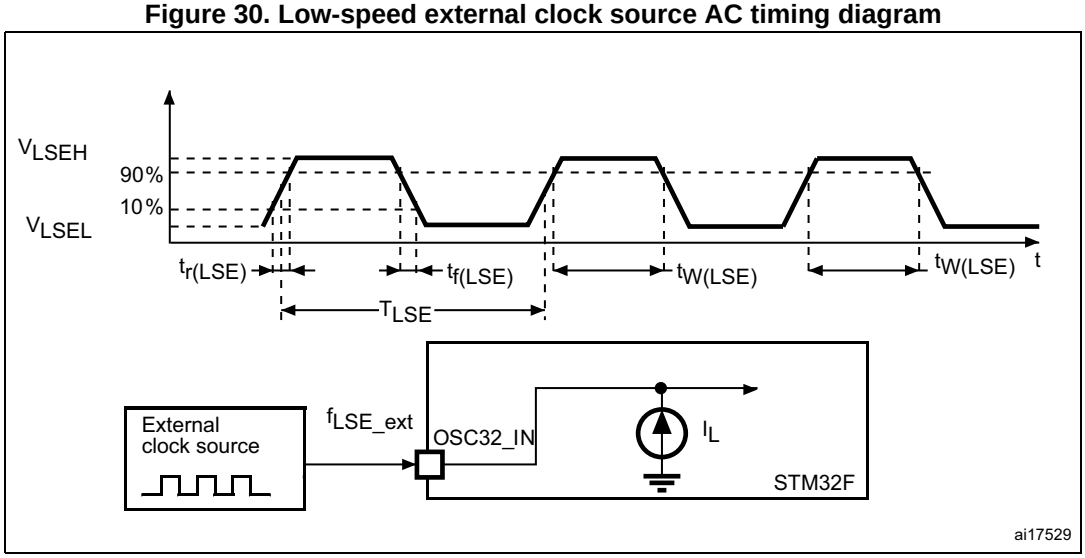



**Figure 30. Low-speed external clock source AC timing diagram**




## High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

**Table 58. I/O static characteristics (continued)**

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{HYS}$ | FT, TTa and NRST I/O input hysteresis | | 1.7 V≤$V_{DD}$≤3.6 V | 10%$V_{DD}$ (3) | - | - | V |
| | BOOT0 I/O input hysteresis | | 1.75 V≤$V_{DD}$ ≤3.6 V, –40 °C≤$T_A$ ≤105 °C | 0.1 | - | - | |
| | | | 1.7 V≤$V_{DD}$ ≤3.6 V, 0 °C≤$T_A$ ≤105 °C | | | | |
| $I_{lkg}$ | I/O input leakage current (4) | | $V_{SS}$ ≤$V_{IN}$ ≤$V_{DD}$ | - | - | ±1 | µA |
| | I/O FT input leakage current (5) | | $V_{IN}$ = 5 V | - | - | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistor(6) | All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID) | $V_{IN}$ = $V_{SS}$ | 30 | 40 | 50 | kΩ |
| | | PA10/PB12 (OTG_FS_ID, OTG_HS_ID) | | 7 | 10 | 14 | |
| $R_{PD}$ | Weak pull-down equivalent resistor(7) | All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID) | $V_{IN}$ = $V_{DD}$ | 30 | 40 | 50 | |
| | | PA10/PB12 (OTG_FS_ID, OTG_HS_ID) | | 7 | 10 | 14 | |
| $C_{IO}$(8) | I/O pin capacitance | | - | - | 5 | - | pF |

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 57*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 57*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Based on test during characterization.

**Table 71. USB HS clock timing parameters(1)**

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| - | $f_{HCLK}$ value to guarantee proper operation of USB HS interface | | 30 | - | - | MHz |
| $F_{START\_8BIT}$ | Frequency (first transition) | 8-bit ±10% | 54 | 60 | 66 | |
| $F_{STEADY}$ | Frequency (steady state) ±500 ppm | | 59.97 | 60 | 60.03 | |
| $D_{START\_8BIT}$ | Duty cycle (first transition) | 8-bit ±10% | 40 | 50 | 60 | % |
| $D_{STEADY}$ | Duty cycle (steady state) ±500 ppm | | 49.975 | 50 | 50.025 | |
| $t_{STEADY}$ | Time to reach the steady state frequency and duty cycle after the first transition | | - | - | 1.4 | ms |
| $t_{START\_DEV}$ | Clock startup time after the de-assertion of SuspendM | Peripheral | - | - | 5.6 | ms |
| $t_{START\_HOST}$ | | Host | - | - | - | |
| $t_{PREP}$ | PHY preparation time after the first transition of the input clock | | - | - | - | µs |

1. Guaranteed by design.

**Figure 50. ULPI timing diagram**

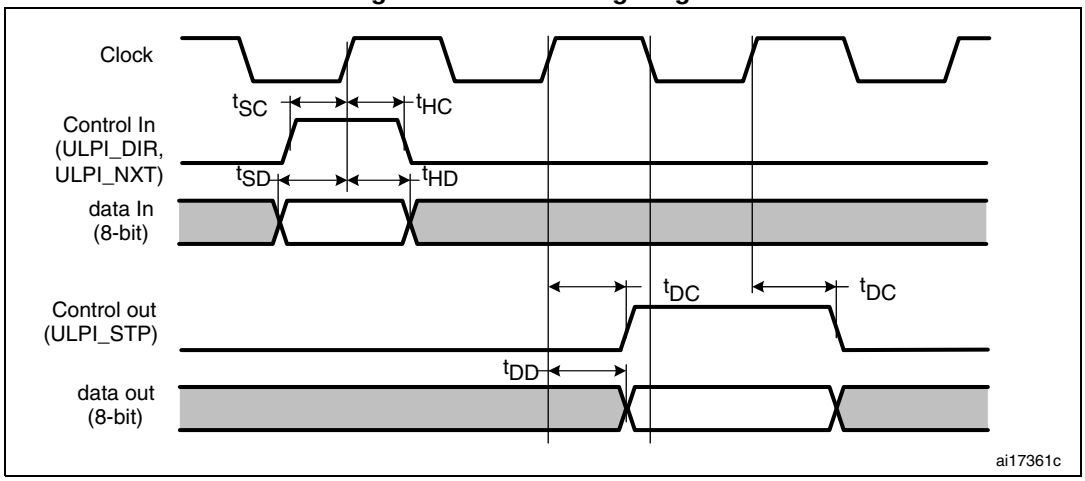


**Table 97. Synchronous multiplexed PSRAM write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FMC_CLK period, $V_{DD}$ range= 2.7 to 3.6 V | $2T_{HCLK} - 1$ | - | ns |
| $t_{d(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x=0…2) | - | 1.5 | |
| $t_{d(CLKH-NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | $T_{HCLK}$ | - | |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 0 | |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 0 | |
| $t_{d(CLKH-AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | $T_{HCLK}$ | - | |
| $t_{d(CLKL-NWEL)}$ | FMC_CLK low to FMC_NWE low | - | 0 | |
| $t_{(CLKH-NWEH)}$ | FMC_CLK high to FMC_NWE high | $T_{HCLK}-0.5$ | - | |
| $t_{d(CLKL-ADV)}$ | FMC_CLK low to FMC_AD[15:0] valid | - | 3 | |
| $t_{d(CLKL-ADIV)}$ | FMC_CLK low to FMC_AD[15:0] invalid | 0 | - | |
| $t_{d(CLKL-DATA)}$ | FMC_A/D[15:0] valid data after FMC_CLK low | - | 3 | |
| $t_{d(CLKL-NBLL)}$ | FMC_CLK low to FMC_NBL low | 0 | - | |
| $t_{d(CLKH-NBLH)}$ | FMC_CLK high to FMC_NBL high | $T_{HCLK}-0.5$ | - | |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 4 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 0 | - | |

1. Based on test during characterization.

**Figure 70. NAND controller waveforms for common memory write access**

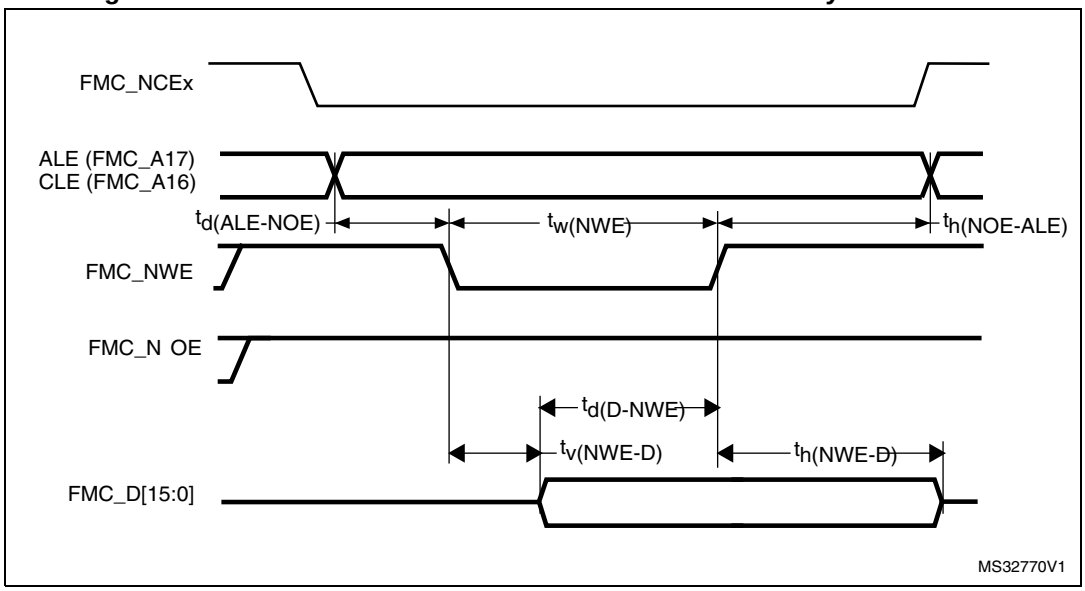



**Table 100. Switching characteristics for NAND Flash read cycles**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(N0E)}$ | FMC_NOE low width | $4T_{HCLK} - 0.5$ | $4T_{HCLK}+0.5$ | ns |
| $t_{su(D-NOE)}$ | FMC_D[15-0] valid data before FMC_NOE high | 9 | - | |
| $t_{h(NOE-D)}$ | FMC_D[15-0] valid data after FMC_NOE high | 0 | - | |
| $t_{d(ALE-NOE)}$ | FMC_ALE valid before FMC_NOE low | - | $3T_{HCLK} - 0.5$ | |
| $t_{h(NOE-ALE)}$ | FMC_NWE high to FMC_ALE invalid | $3T_{HCLK} - 2$ | - | |

**Table 101. Switching characteristics for NAND Flash write cycles**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NWE)}$ | FMC_NWE low width | $4T_{HCLK}$ | $4T_{HCLK}+1$ | ns |
| $t_{v(NWE-D)}$ | FMC_NWE low to FMC_D[15-0] valid | 0 | - | |
| $t_{h(NWE-D)}$ | FMC_NWE high to FMC_D[15-0] invalid | $3T_{HCLK} - 1$ | - | |
| $t_{d(D-NWE)}$ | FMC_D[15-0] valid before FMC_NWE high | $5T_{HCLK} - 3$ | - | |
| $t_{d(ALE-NWE)}$ | FMC_ALE valid before FMC_NWE low | - | $3T_{HCLK}-0.5$ | |
| $t_{h(NWE-ALE)}$ | FMC_NWE high to FMC_ALE invalid | $3T_{HCLK} - 1$ | - | |

## SDRAM waveforms and timings

- $C_L$ = 30 pF on data and address lines.
- $C_L$ = 10 pF on FMC_SDCLK unless otherwise specified.

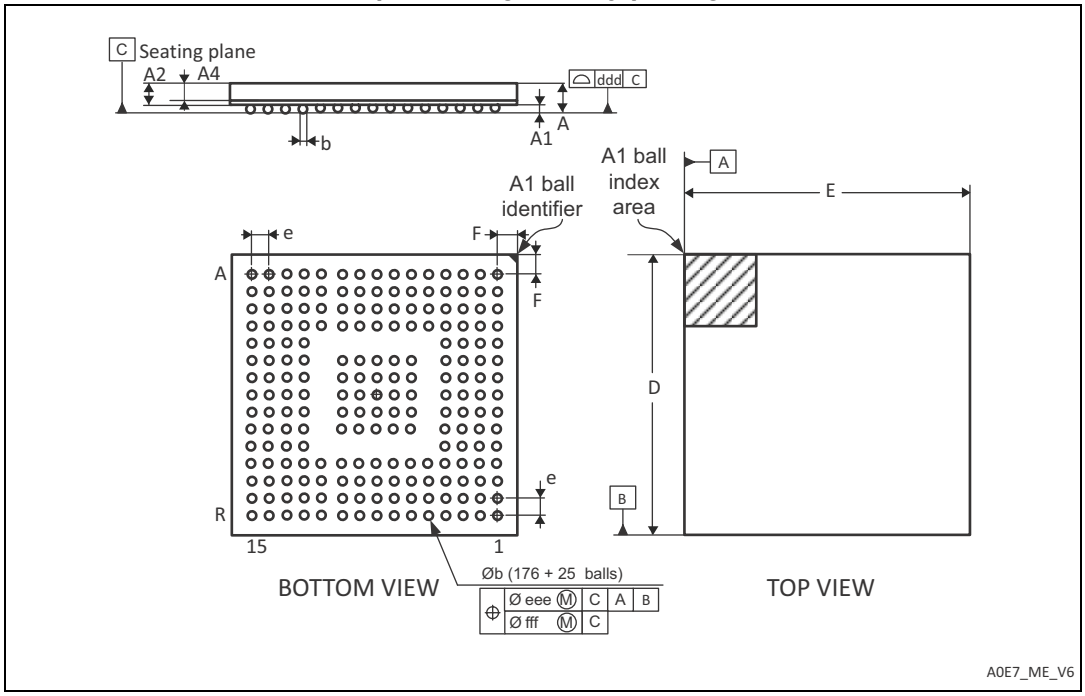
**Table 117. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| e | - | 0.500 | - | - | 0.0197 | - |
| HD | 25.900 | - | 26.100 | 1.0200 | - | 1.0276 |
| HE | 25.900 | - | 26.100 | 1.0200 | - | 1.0276 |
| L | 0.450 | - | 0.750 | 0.0177 | - | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ZD | - | 1.250 | - | - | 0.0492 | - |
| ZE | - | 1.250 | - | - | 0.0492 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |
| k | 0 ° | - | 7 ° | 0 ° | - | 7 ° |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 6.6 UFBGA176+25 package information

**Figure 92. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline**




1. Drawing is not to scale.

**Table 118. UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.0020 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A4 | 0.270 | 0.320 | 0.370 | 0.0106 | 0.0126 | 0.0146 |
| b | 0.230 | 0.280 | 0.330 | 0.0091 | 0.0110 | 0.0130 |
| D | 9.950 | 10.000 | 10.050 | 0.3917 | 0.3937 | 0.3957 |
| E | 9.950 | 10.000 | 10.050 | 0.3917 | 0.3937 | 0.3957 |
| e | - | 0.650 | - | - | 0.0256 | - |
| F | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| ddd | - | - | 0.080 | - | - | 0.0031 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.