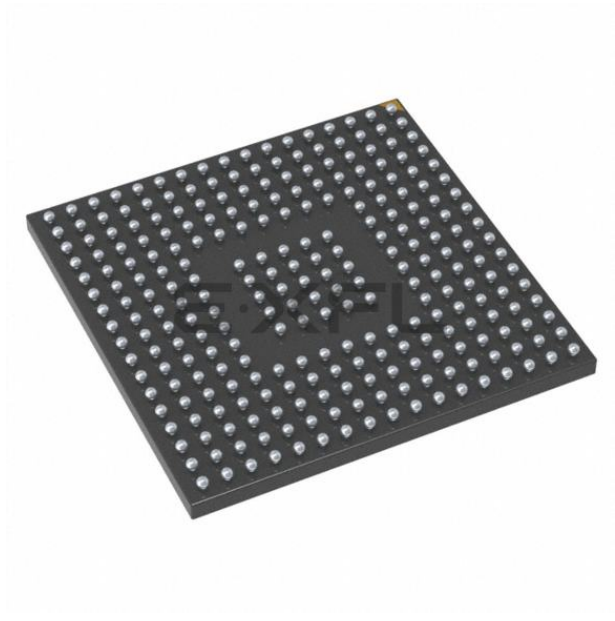

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f469igh6tr

1 Description

The STM32F469xx devices are based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 180 MHz. The Cortex®-M4 core features a Floating point unit (FPU) single precision which supports all ARM® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F469xx devices incorporate high-speed embedded memories (Flash memory up to 2 Mbytes, up to 384 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, and a true random number generator (RNG). They also feature standard and advanced communication interfaces:

- Up to three I^2Cs
- Six SPIs, two I^2Ss full duplex. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- One SAI serial audio interface
- An SDMMC host interface
- Ethernet and camera interface
- LCD-TFT display controller
- Chrom-ART Accelerator™
- DSI Host.

Advanced peripherals include an SDMMC interface, a flexible memory control (FMC) interface, a Quad-SPI Flash memory, and camera interface for CMOS sensors. Refer to *Table 2* for the list of peripherals available on each part number.

The STM32F469xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. A dedicated supply input for USB (OTG_FS and OTG_HS) only in full speed mode, is available on all packages.

The supply voltage can drop to 1.7 V (refer to *Section 2.19.2*). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F469xx devices are offered in eight packages, ranging from 100 to 216 pins. The set of included peripherals changes with the device chosen, according to *Table 2*.

1.1 Compatibility throughout the family

STM32F469xx devices are not compatible with other STM32F4xx devices.

Figure 1 and *Figure 2* show incompatible board designs, respectively, for LQFP176 and LQFP208 packages (highlighted pins).

The UFBGA176 and TFBGA216 ballouts are compatible with other STM32F4xx devices, only few IO port pins are substituted, as shown in *Figure 3* and *Figure 4*.

The LQFP100, LQFP144 and UFBGA169 packages are incompatible with other STM32F4xx devices.

2.4 Embedded Flash memory

The devices embed a Flash memory of up to 2 Mbytes available for storing programs and data.

2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.6 Embedded SRAM

All devices embed:

- Up to 384Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM

  RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

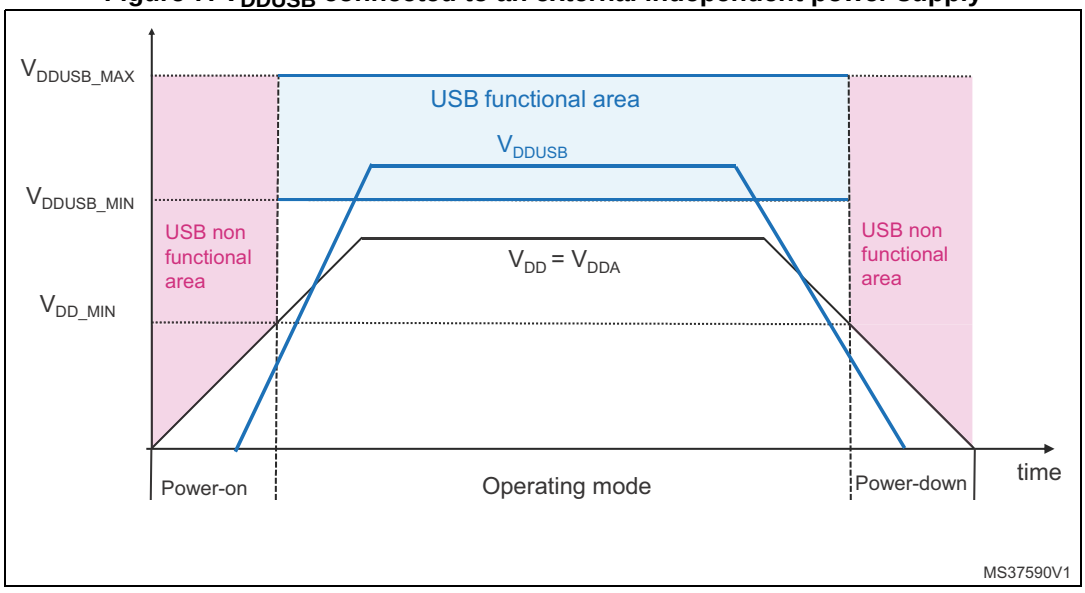
2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, QUADSPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

The following conditions must be respected:

- During power-on phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- During power-down phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- V_{DDUSB} rising and falling time rate specifications must be respected.
- In operating mode phase, V_{DDUSB} could be lower or higher than VDD:
  - If USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX}.The V_{DDUSB} supplies both USB transceivers (USB OTG_HS and USB OTG_FS).
  - If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by V_{DDUSB}.
  - If USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX}.

Figure 7. V_{DDUSB} connected to an external independent power supply



The DSI (Display Serial Interface) sub-system uses several power supply pins which are independent from the other supply pins:

- VDDDSI is an independent DSI power supply dedicated for DSI Regulator and MIPI D-PHY. This supply must be connected to global VDD.
- VCAPDSI pin is the output of DSI Regulator (1.2V) which must be connected externally to VDD12DSI.
- VDD12DSI pin is used to supply the MIPI D-PHY, and to supply clock and data lanes pins. An external capacitor of 2.2 uF must be connected on VDD12DSI pin.
- VSSDSI pin is an isolated supply ground used for DSI sub-system.
- If DSI functionality is not used at all, then:
  - VDDDSI pin must be connected to global VDD.
  - VCAPDSI pin must be connected externally to VDD12DSI but the external capacitor is no more needed.
  - VSSDSI pin must be grounded.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to analog parts
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 11. FMC pin definition (continued)

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF8	-	-	-	-
PF9	-	-	-	-
PF10	-	-	-	-
PG6	-	-	-	-
PG7	-	-	INT	-
PE0	NBL0	NBL0	-	NBL0
PE1	NBL1	NBL1	-	NBL1
PI4	NBL2	-	-	NBL2
PI5	NBL3	-	-	NBL3
PG8	-	-	-	SDCLK
PC0	-	-	-	SDNWE
PF11	-	-	-	SDNRAS
PG15	-	-	-	SDNCAS
PH2	-	-	-	SDCKE0
PH3	-	-	-	SDNE0
PH6	-	-	-	SDNE1
PH7	-	-	-	SDCKE1
PH5	-	-	-	SDNWE
PC2	-	-	-	SDNE0
PC3	-	-	-	SDCKE0
PB5	-	-	-	SDCKE1
PB6	-	-	-	SDNE1

Table 12. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI HOST	LCD	SYS
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENT OUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENT OUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	EVENT OUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	EVENT OUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/FMC_BA0	-	-	EVENT OUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/FMC_BA1	-	-	EVENT OUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-		DCMI_D12	LCD_R7	EVENT OUT
	PG7	-	-	-	-	-		SAI1_MCLK_A		USART6_CK	-	-	-	FMC_INT	DCMI_D13	LCD_CLK	EVENT OUT
	PG8	-	-	-	-	-	SPI6_NSS	-	-	USART6_RTS	-	-	ETH_PPS_OUT	FMC_SDCLK		LCD_G7	EVENT OUT
	PG9	-	-	-	-	-	-	-	-	USART6_RX	QUADSPI_BK2_IO2	-	-	FMC_NE2/FMC_NCE	DCMI_VSYNC		EVENT OUT
	PG10	-	-	-	-	-	-	-	-		LCD_G3	-	-	FMC_NE3	DCMI_D2	LCD_B2	EVENT OUT
	PG11	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_TX_EN / ETH_RMII_TX_EN	-	DCMI_D3	LCD_B3	EVENT OUT
	PG12	-	-	-	-	-	SPI6_MISO	-	-	USART6_RTS	LCD_B4	-	-	FMC_NE4	-	LCD_B1	EVENT OUT
	PG13	TRACED0	-	-	-	-	SPI6_SCK	-	-	USART6_CTS	-	-	ETH_MII_TXD0 / ETH_RMII_TXD0	FMC_A24	-	LCD_R0	EVENT OUT
	PG14	TRACED1	-	-	-	-	SPI6_MOSI	-	-	USART6_TX	QUADSPI_BK2_IO3	-	ETH_MII_TXD1 / ETH_RMII_TXD1	FMC_A25	-	LCD_B0	EVENT OUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	FMC_SDNCAS	DCMI_D13	-	EVENT ‘OUT

Table 12. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSIHOST	LCD	SYS
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENTOUT
	PI1	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	FMC_D25	DCMI_D8	LCD_G6	EVENTOUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENTOUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	FMC_D27	DCMI_D10		EVENTOUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	-	FMC_NBL2	DCMI_D5	LCD_B4	EVENTOUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	-	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENTOUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	-	FMC_D28	DCMI_D6	LCD_B6	EVENTOUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	-	-	FMC_D29	DCMI_D7	LCD_B7	EVENTOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-		EVENTOUT
	PI9	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_D30	-	LCD_VSYNC	EVENTOUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RX_ER	FMC_D31	-	LCD_HSYNC	EVENTOUT
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-	-	-	-	EVENTOUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	EVENTOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENTOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENTOUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENT‘OUT

Table 24. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM, regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in RUN mode	All Peripherals enabled(2)(3)	180	103	109(4)	142	175(4)	mA
			168	94	99	124	149	
			150	84	89	114	140	
			144	77	81	104	127	
			120	57	60	79	98	
			90	43	46	64	84	
			60	30	33	51	70	
			30	16	19	37	57	
			25	14	16	34	54	
			16	7	10	28	48	
			8	4	7	26	46	
			4	3	6	24	44	
			2	3	5	23	43	
		All Peripherals disabled(2)	180	50	56(4)	89	124(4)	
			168	45	51	75	102	
			150	41	46	70	97	
			144	37	42	63	88	
			120	28	31	49	69	
			90	21	24	42	63	
			60	15	17	36	56	
			30	9	11	29	49	
			25	7	10	28	48	
			16	4	7	25	45	
			8	3	6	22	44	
			4	3	5	23	43	
			2	2	5	23	43	

1. Guaranteed based on test during characterization.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. Guaranteed by test in production.

Table 28. Typical and maximum current consumption in Sleep mode, regulator OFF

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ		Max(1)						Unit
				I_{DD12}	I_{DD}	T_A = 25 °C		T_A = 85 °C		T_A = 105 °C		
						I_{DD12}	I_{DD}	I_{DD12}	I_{DD}	I_{DD12}	I_{DD}	
I_{DD12} / I_{DD}	Supply current in RUN mode from V_{12} and V_{DD} supply	All Peripherals enabled	168	70	1	75	1	100	1	126	1	mA
			150	63	1	70	1	93	1	118	1	
			144	57	1	61	1	84	1	108	1	
			120	42	1	45	1	64	1	84	1	
			90	32	1	36	1	53	1	73	1	
			60	22	1	24	1	43	1	63	1	
			30	12	1	14	1	33	1	53	1	
			25	10	1	12	1	31	1	51	1	
		All Peripherals disabled	168	20	1	24	1	49	1	75	1	
			150	18	1	22	1	47	1	73	1	
			144	16	1	19	1	42	1	66	1	
			120	12	1	14	1	33	1	53	1	
			90	10	1	12	1	30	1	50	1	
			60	7	1	9	1	27	1	47	1	
			30	4	1	6	1	24	1	44	1	
			25	4	1	6	1	24	1	44	1	

1. Guaranteed based on test during characterization.

Table 30. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions	Typ(1)			Max(2)			Unit
			T_A = 25 °C			T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.7 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.3 V			
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM ON, RTC and LSE oscillator OFF	1.7	2.5	2.9	6(3)	18	35(3)	µA
		Backup SRAM OFF, RTC and LSE oscillator OFF	1.0	1.8	2.20	5(3)	15	30(3)	
		Backup SRAM OFF, RTC ON and LSE oscillator in Power Drive mode	1.7	2.7	3.2	7	20	39	
		Backup SRAM ON, RTC ON and LSE oscillator in Power Drive mode	2.4	3.4	4.0	8	25	48	
		Backup SRAM ON, RTC ON and LSE oscillator in High Drive mode	3.2	4.2	4.8	10	29	57	
		Backup SRAM OFF, RTC ON and LSE oscillator in High Drive mode	2.5	3.5	4.1	8	25	48	

1. PDR is off for V_{DD}=1.7 V. When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

Figure 35 and *Figure 36* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 35. PLL output clock waveforms in center spread mode

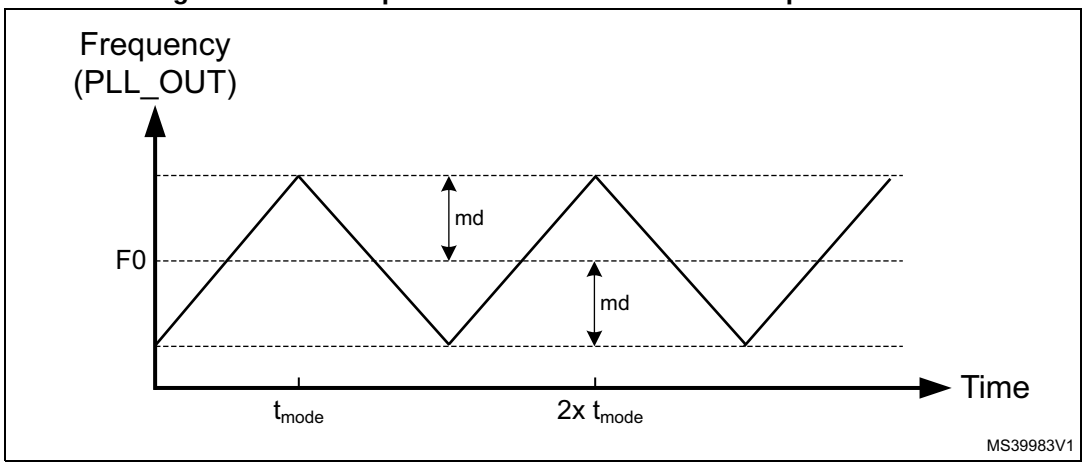
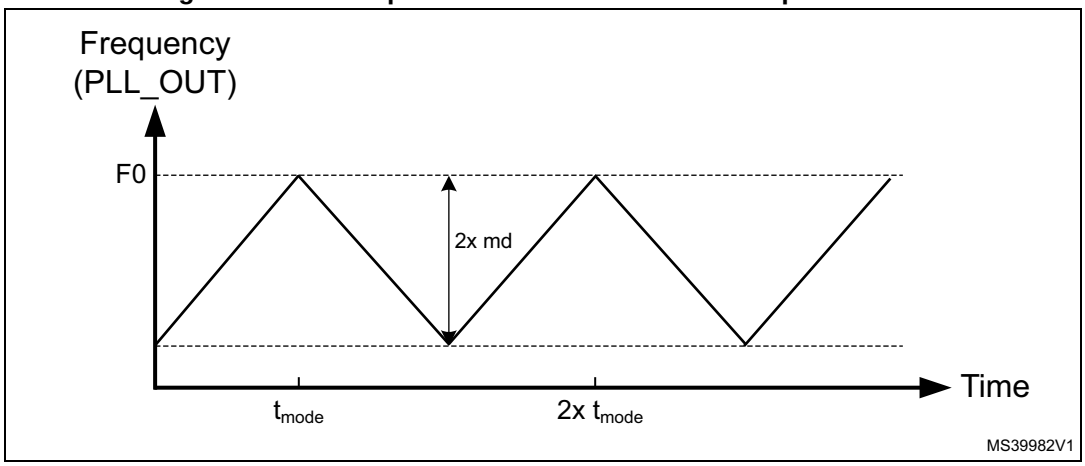


Figure 36. PLL output clock waveforms in down spread mode



5.3.13 MIPI D-PHY characteristics

The parameters given in *Table 45* and *Table 46* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 45. MIPI D-PHY characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Hi-Speed Input/Output Characteristics						
U_{INST}	UI instantaneous	-	2	-	12.5	ns

Table 60. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.7 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	2	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	8	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	4	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	3	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD}≥ 2.7 V	-	-	25	MHz
			C_L = 50 pF, V_{DD}≥ 1.8 V	-	-	12.5	
			C_L = 50 pF, V_{DD}≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	50	
			C_L = 10 pF, V_{DD}≥ 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	12.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} ≥ 2.7 V	-	-	10	ns
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	6	
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	20	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} ≥ 2.7 V	-	-	50(4)	MHz
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	100(4)	
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	25	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	50	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	42.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} ≥2.7 V	-	-	6	ns
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	4	
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	6	

5.3.22 TIM timer characteristics

The parameters given in *Table 62* are guaranteed by design. Refer to *Section 5.3.20* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 62. TIMx characteristics(1)(2)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 180 MHz	1	-	$t_{TIMxCLK}$
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 90 MHz	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 180 MHz	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 32-bit counter		-	65536 × 65536	$t_{TIMxCLK}$

1. TIMx is used as a general term to refer to the TIM1 to TIM12 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 180 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK = 4x PCLKx.

5.3.23 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0386 reference manual).

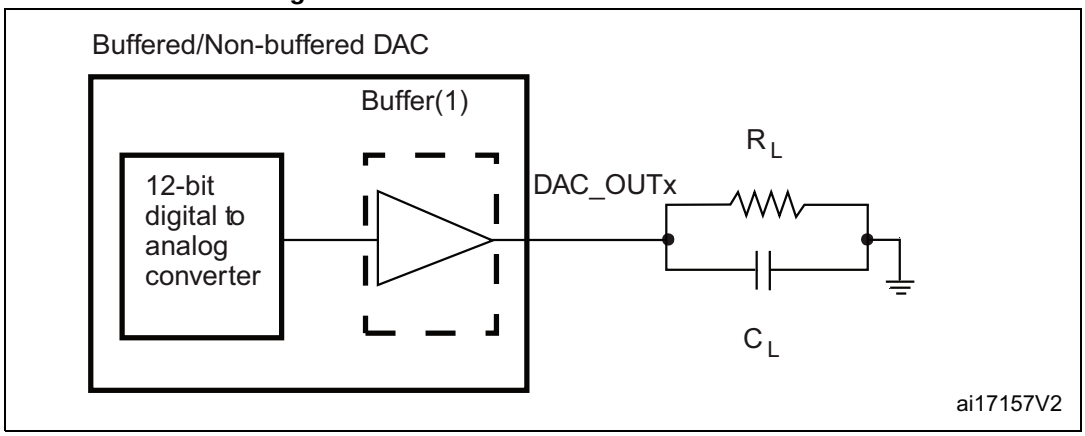
The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. Refer to *Section 5.3.20* for more details on the I²C I/O characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 63. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	150(3)	ns

Figure 58. 12-bit buffered/non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.29 FMC characteristics

Unless otherwise specified, the parameters given in Tables *88* through *101* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 V_{DD}

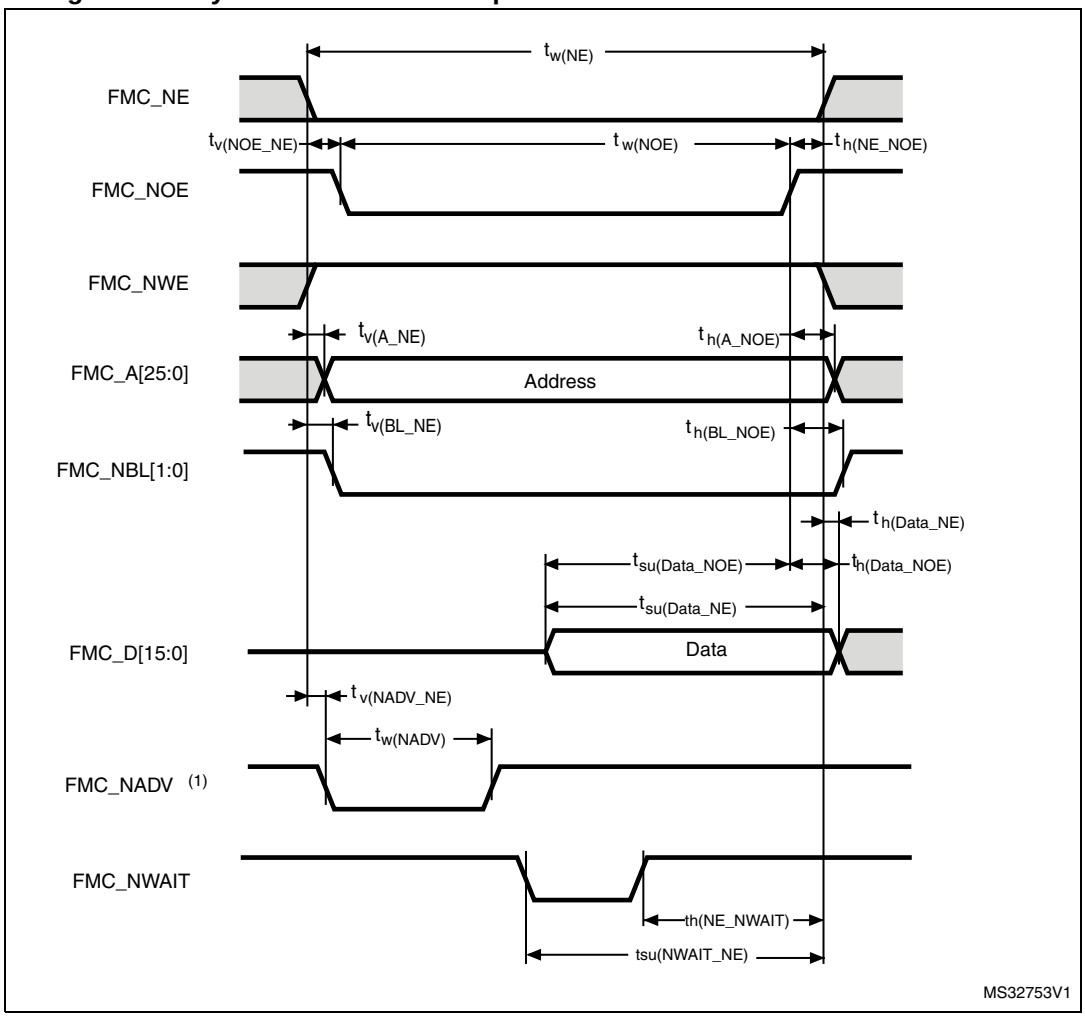
Refer to *Section 5.3.20* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figures *59* through *62* represent asynchronous waveforms, and Tables *88* through *95* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

Figure 59. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK} - 0.5$	$2\ T_{HCLK}+0.5$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK}$	$2T_{HCLK}+ 0.5$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} + 2.5$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	$T_{HCLK} +2$	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK} +1$	

1. Based on test during characterization.

Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{HCLK}+0.5$	$7T_{HCLK}+1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1.5$	$5T_{HCLK} +2$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}+1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$	-	

1. Based on test during characterization.

Figure 79. SD default mode

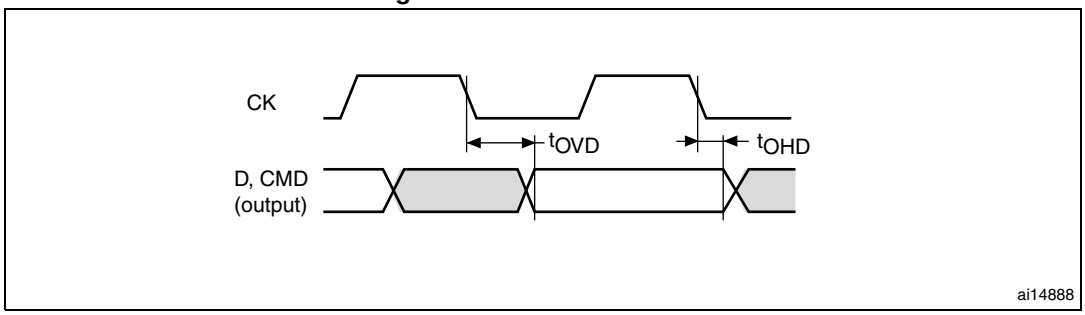


Table 110. Dynamic characteristics: SD / MMC characteristics, V_{DD} = 2.7 to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{pp} =50 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	f_{pp} =50 MHz	2.0	-	-	ns
t_{IH}	Input hold time HS		2.0	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	f_{pp} =50 MHz	-	13	13.5	ns
t_{OH}	Output hold time HS		12.5	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{pp} =25 MHz	2.0	-	-	ns
t_{IHD}	Input hold time SD		2.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{pp} =25 MHz	-	1.5	2.0	ns
t_{OHD}	Output hold default time SD		1.0	-	-	

1. Guaranteed based on test during characterization.

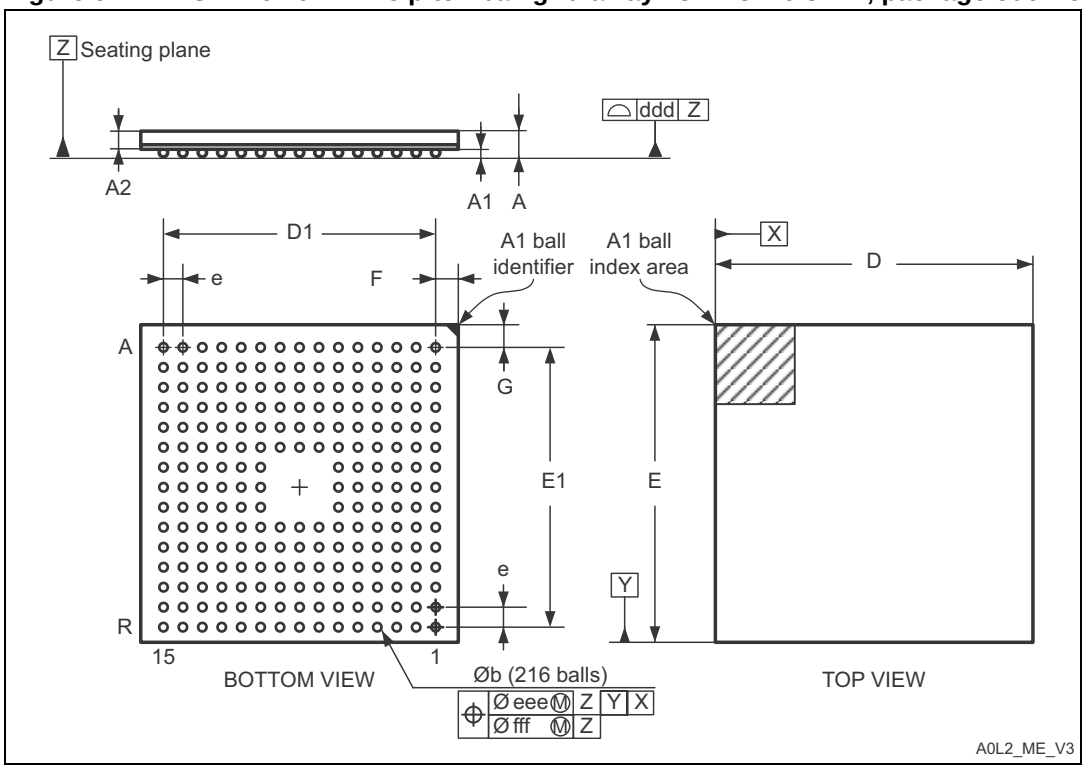
Table 114. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.8 TFBGA216 package information

Figure 97. TFBGA216 - thin fine pitch ball grid array 13 × 13 × 0.8mm, package outline



1. Drawing is not to scale.

Table 121. TFBGA216 - thin fine pitch ball grid array 13 × 13 × 0.8mm package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
A4	-	0.210	-	-	0.0083	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	12.850	13.000	13.150	0.5118	0.5118	0.5177
D1	-	11.200	-	-	0.4409	-
E	12.850	13.000	13.150	0.5118	0.5118	0.5177
E1	-	11.200	-	-	0.4409	-
e	-	0.800	-	-	0.0315	-
F	-	0.900	-	-	0.0354	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.