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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	131
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f469iit6

These features make the STM32F469xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 5 shows the general block diagram of the device family.

Table 2. STM32F469xx features and peripheral counts

Peripherals		STM32F469Vx	STM32F469Zx	STM32F469Ax	STM32F469Ix	STM32F469Bx	STM32F469Nx
Flash memory in Kbytes		512 1024 2048	512 1024 2048	512 1024 2048	512 1024 2048	512 1024 2048	512 1024 2048
SRAM in Kbytes	System	384 (160+32+128+64)					
	Backup	4					
FMC memory controller		Yes					
Quad-SPI		Yes					
Ethernet		No			Yes		
Timers	General-purpose	10					
	Advanced-control	2					
	Basic	2					
Random number generator		Yes					
Communication interfaces	SPI / I^2S	4/2(full duplex)(1)		6/2(full duplex)(1)			
	I^2C	3					
	USART/UART	4/3		4/4			
	USB OTG FS	Yes					
	USB OTG HS	Yes					
	CAN	2					
	SAI	1					
	SDIO	Yes					
Camera interface		Yes					

1.1 Compatibility throughout the family

STM32F469xx devices are not compatible with other STM32F4xx devices.

Figure 1 and *Figure 2* show incompatible board designs, respectively, for LQFP176 and LQFP208 packages (highlighted pins).

The UFBGA176 and TFBGA216 ballouts are compatible with other STM32F4xx devices, only few IO port pins are substituted, as shown in *Figure 3* and *Figure 4*.

The LQFP100, LQFP144 and UFBGA169 packages are incompatible with other STM32F4xx devices.

The DSI Host main features:

- Compliant with MIPI® Alliance standards
- Interface with MIPI® D-PHY
- Supports all commands defined in the MIPI® Alliance specification for DCS:
  - Transmission of all Command mode packets through the APB interface
  - Transmission of commands in low-power and high-speed during Video Mode
- Supports up to two D-PHY data lanes
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports Ultra Low-Power mode with PLL disabled
- ECC and Checksum capabilities
- Support for End of Transmission Packet (EoTp)
- Fault recovery schemes
- 3D transmission support
- Configurable selection of system interfaces:
  - AMBA APB for control and optional support for Generic and DCS commands
  - Video Mode interface through LTDC
  - Adapted Command Mode interface through LTDC
- Independently programmable Virtual Channel ID in
  - Video Mode
  - Adapted Command Mode
  - APB Slave

Video Mode interfaces features:

- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB
- Programmable polarity of all LTDC interface signals
- Extended resolutions beyond the DPI standard maximum resolution of 800x480 pixels: maximum resolution is limited by available DSI physical link bandwidth:
  - Number of lanes: 2
  - Maximum speed per lane: 500Mbps

Adapted interface features:

- Support for sending large amounts of data through the *memory_write_start* (WMS) and *memory_write_continue* (WMC) DCS commands
- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB

2.43 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

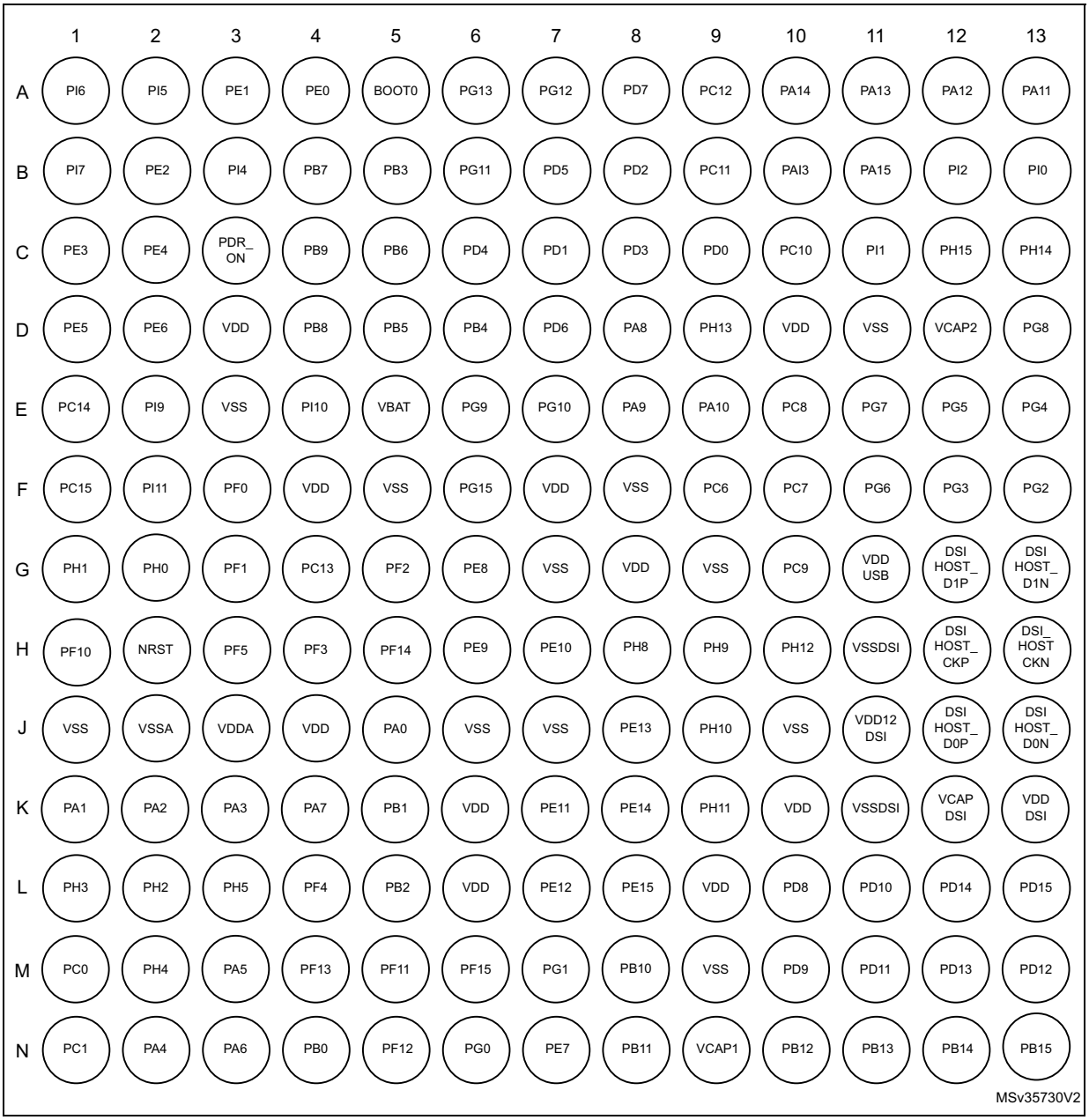
Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.44 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F46x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

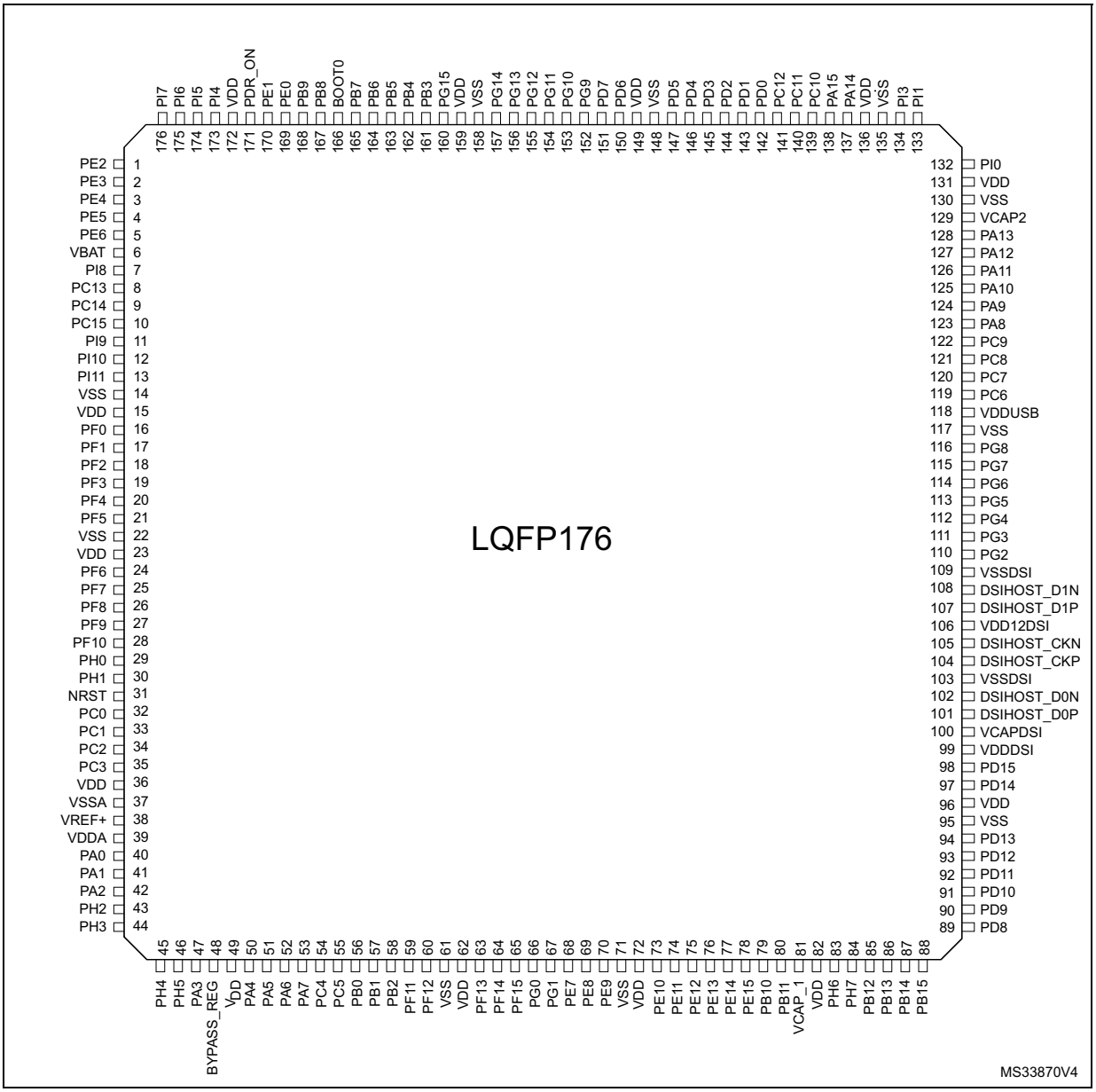
The Embedded Trace Macrocell operates with third party debugger software tools.

Figure 16. STM32F46x UFBGA169 ballout



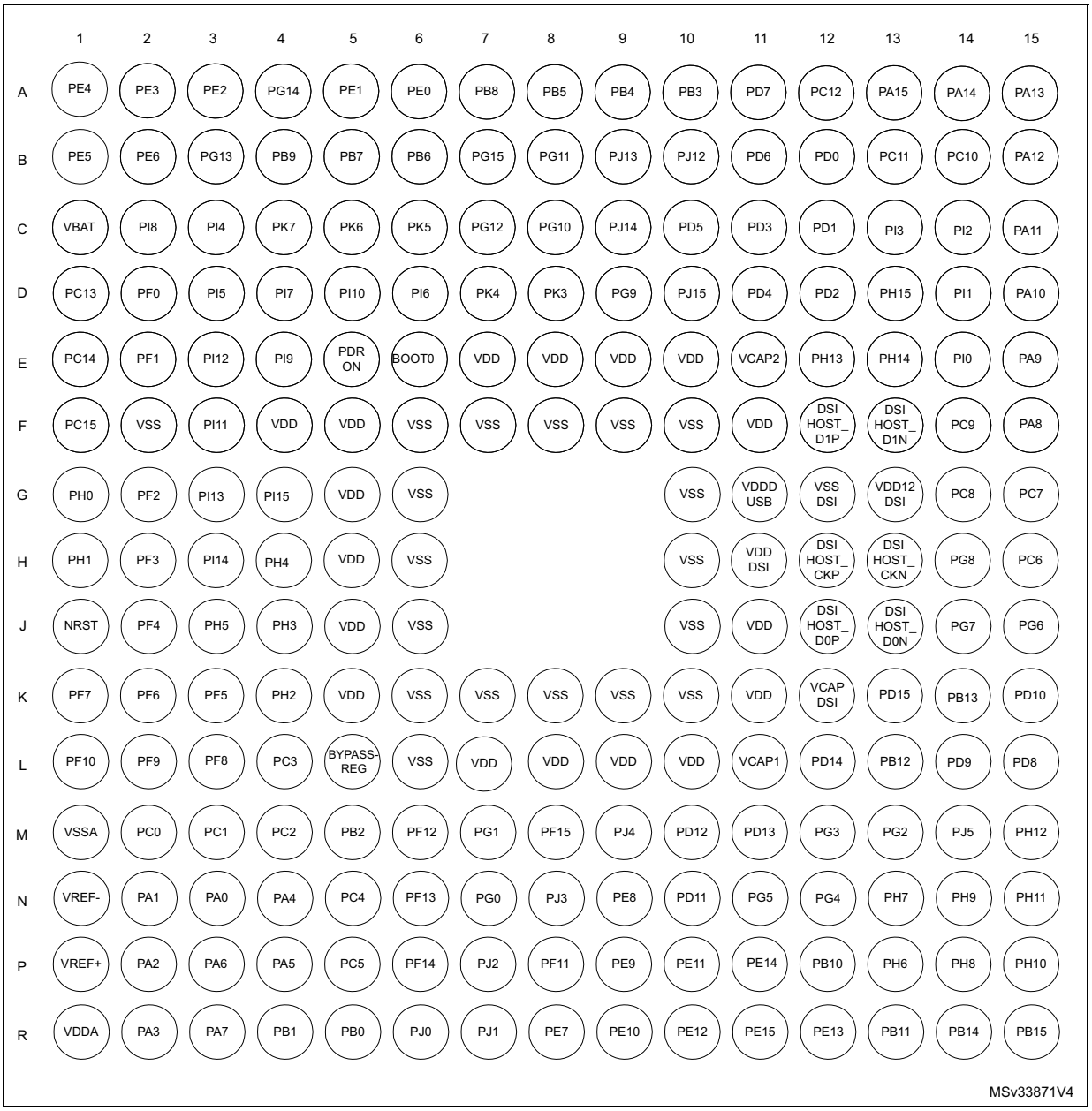
1. The above figure shows the package top view.

Figure 18. STM32F46x LQFP176 pinout



1. The above figure shows the package top view.

Figure 20. STM32F46x TFBGA216 ballout



1. The above figure shows the package top view.

Table 10. STM32F469xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	J9	M4	-	-	100	P15	PH10	I/O	FT	-	TIM5_CH1, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	K9	N3	-	-	101	N15	PH11	I/O	FT	-	TIM5_CH2, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	-	H10	P2	-	-	102	M15	PH12	I/O	FT	-	TIM5_CH3, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	-	H7	-	-	-	K10	VSS	S	-	-	-	-
-	66	-	-	-	-	103	K11	VDD	S	-	-	-	-
46	67	N10	H5	P12	85	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT	-
47	68	N11	K4	P13	86	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT	OTG_HS_VBUS
48	69	N12	P1	R14	87	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, I2S2ext_SD, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT	-
49	70	N13	N2	R15	88	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT	-
50	71	L10	L4	P15	89	108	L15	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
51	72	M10	N1	P14	90	109	L14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
52	73	L11	M3	N15	91	110	K15	PD10	I/O	FT	-	USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
-	74	M11	J4	N14	92	111	N10	PD11	I/O	FT	-	USART3_CTS, QUADSPI_BK1_IO0, FMC_A16/FMC_CLE, EVENTOUT	-

Table 10. STM32F469xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
96	136	B4	A9	B5	165	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT	-
97	137	A5	F8	D6	166	197	E6	BOOT0	I	B	-	-	VPP
98	138	D4	B9	A5	167	198	A7	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDIO_D4, DCMI_D6, LCD_B6, EVENTOUT	-
99	139	C4	E9	B4	168	199	B4	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDIO_D5, DCMI_D7, LCD_B7, EVENTOUT	-
NC (2)	140	A4	A10	A4	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, UART8_Rx, FMC_NBL0, DCMI_D2, EVENTOUT	-
NC (2)	141	A3	C9	A3	170	201	A5	PE1	I/O	FT	-	UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	E3	B10	D5	-	202	F6	VSS	S	-	-	-	-
-	142	C3	D9	C6	171	203	E5	PDR_ON	S	-	-	-	-
100	143	D3	A11	C5	172	204	E7	VDD	S	-	-	-	-
-	-	B3	D10	D4	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	A2	C10	C4	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	A1	B11	C3	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	B1	A12	C2	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

1. **Function availability depends on the chosen device.**
2. NC (not-connected) pins are not bonded. They must be configured by software to output push-pull and forced to “0” in the output data register to avoid extra current consumption in low power modes.
3. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
4. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F4xx reference manual, available from the STMicroelectronics website: www.st.com.
5. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

Table 12. Alternate function (continued)

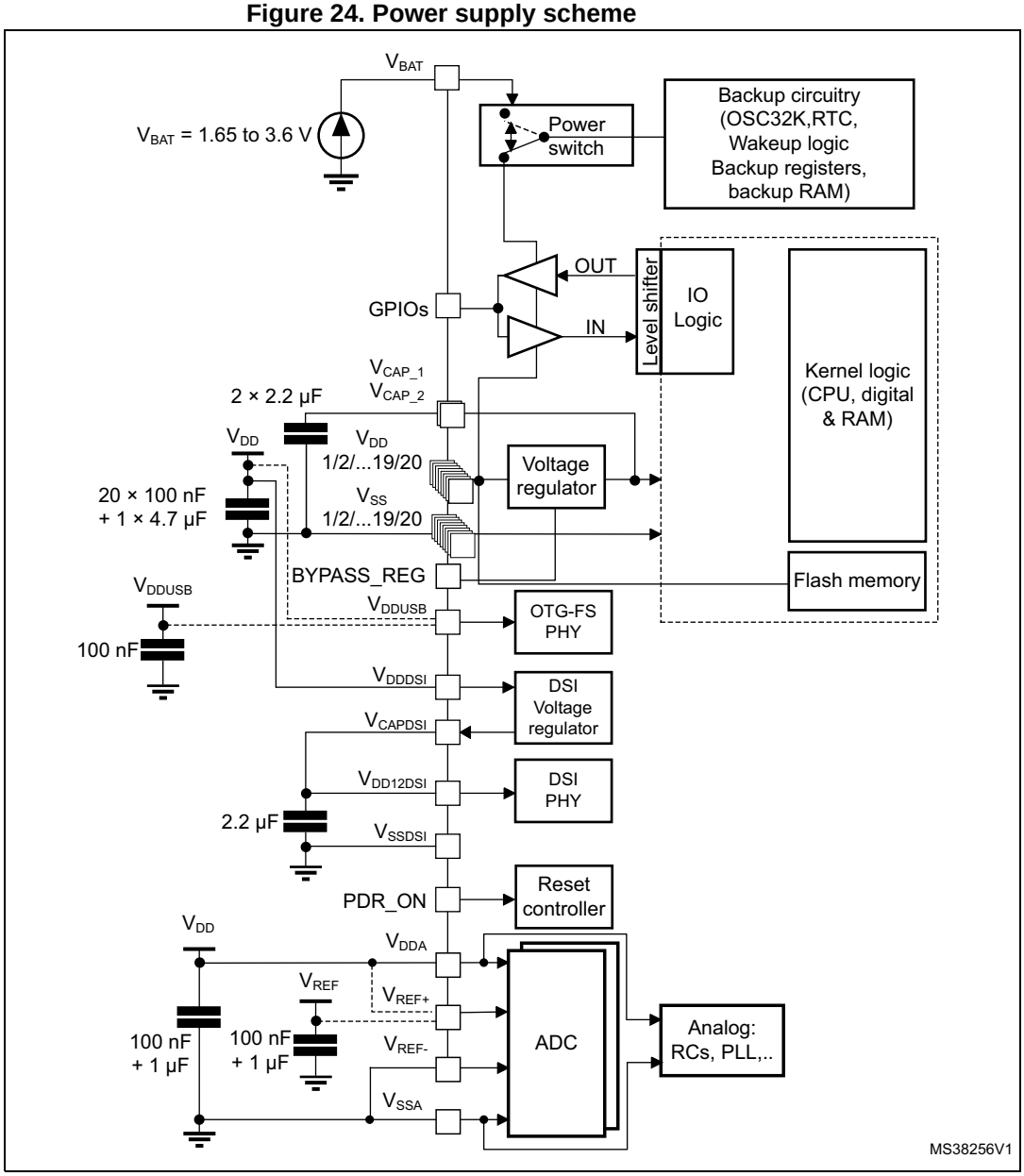
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI HOST	LCD	SYS
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_D2	-	-	EVENTOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	FMC_D3	-	-	EVENTOUT
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_CMD	DCMI_D11	-	EVENTOUT
	PD3	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	USART2_CTS	-	-	-	-	FMC_CLK	DCMI_D5	LCD_G7	EVENTOUT
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	-	SPI3_MOSI/I2S3_SD	SAI1_SD_A	USART2_RX	-	-	-	-	FMC_NWAIT	DCMI_D10	LCD_B2	EVENTOUT
	PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	FMC_NE1	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	FMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	FMC_D14	-	-	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	FMC_D15	-	LCD_B3	EVENTOUT
	PD11	-	-	-	-	-	-	-	USART3_CTS	-	QUADSPI_BK1_IO0	-	-	FMC_A16/FMC_CLE	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	QUADSPI_BK1_IO1	-	-	FMC_A17/FMC_ALE	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	QUADSPI_BK1_IO3	-	-	FMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	FMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	FMC_D1	-	-	EVENT‘OUT

Table 12. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI HOST	LCD	SYS
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENT OUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENT OUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	EVENT OUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	EVENT OUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/FMC_BA0	-	-	EVENT OUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/FMC_BA1	-	-	EVENT OUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-		DCMI_D12	LCD_R7	EVENT OUT
	PG7	-	-	-	-	-		SAI1_MCLK_A		USART6_CK	-	-	-	FMC_INT	DCMI_D13	LCD_CLK	EVENT OUT
	PG8	-	-	-	-	-	SPI6_NSS	-	-	USART6_RTS	-	-	ETH_PPS_OUT	FMC_SDCLK		LCD_G7	EVENT OUT
	PG9	-	-	-	-	-	-	-	-	USART6_RX	QUADSPI_BK2_IO2	-	-	FMC_NE2/FMC_NCE	DCMI_VSYNC		EVENT OUT
	PG10	-	-	-	-	-	-	-	-		LCD_G3	-	-	FMC_NE3	DCMI_D2	LCD_B2	EVENT OUT
	PG11	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_TX_EN / ETH_RMII_TX_EN	-	DCMI_D3	LCD_B3	EVENT OUT
	PG12	-	-	-	-	-	SPI6_MISO	-	-	USART6_RTS	LCD_B4	-	-	FMC_NE4	-	LCD_B1	EVENT OUT
	PG13	TRACED0	-	-	-	-	SPI6_SCK	-	-	USART6_CTS	-	-	ETH_MII_TXD0 / ETH_RMII_TXD0	FMC_A24	-	LCD_R0	EVENT OUT
	PG14	TRACED1	-	-	-	-	SPI6_MOSI	-	-	USART6_TX	QUADSPI_BK2_IO3	-	ETH_MII_TXD1 / ETH_RMII_TXD1	FMC_A25	-	LCD_B0	EVENT OUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	FMC_SDNCAS	DCMI_D13	-	EVENT ‘OUT

5.1.6 Power supply scheme

Figure 24. Power supply scheme



1. To connect BYPASS_REG and PDR_ON pins, refer to *Section 2.19* and *Section 2.20*.
2. The two 2.2 µF ceramic capacitors on V_{CAP_1} and V_{CAP_2} should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.
4. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

5.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 54*). It is available only on the main PLL.

Table 44. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	$2^{15} - 1$	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz, and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(peak)$$

Table 58. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{HYS}	FT, TTa and NRST I/O input hysteresis		1.7 V≤V_{DD}≤3.6 V	10%V_{DD} (3)	-	-	V
	BOOT0 I/O input hysteresis		1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	0.1	-	-	
			1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
I_{lkg}	I/O input leakage current (4)		V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (5)		V_{IN} = 5 V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10/PB12 (OTG_FS_ID, OTG_HS_ID)	V_{IN} = V_{DD}	30	40	50	
		PA10/PB12 (OTG_FS_ID, OTG_HS_ID)		7	10	14	
C_{IO}(8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 57*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 57*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Based on test during characterization.

Table 60. I/O AC characteristics(1)(2)

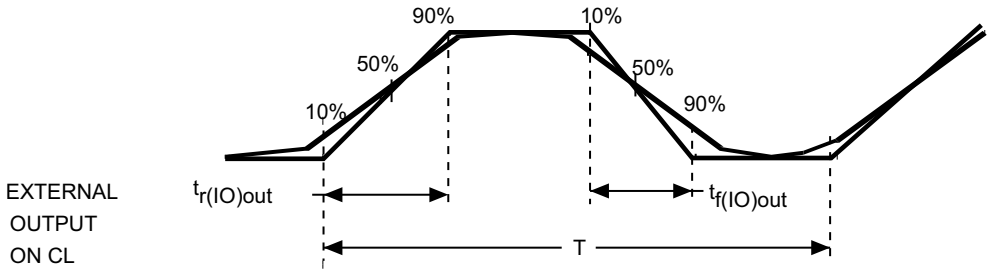
OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.7 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	2	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	8	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	4	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	3	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD}≥ 2.7 V	-	-	25	MHz
			C_L = 50 pF, V_{DD}≥ 1.8 V	-	-	12.5	
			C_L = 50 pF, V_{DD}≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	50	
			C_L = 10 pF, V_{DD}≥ 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	12.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} ≥ 2.7 V	-	-	10	ns
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	6	
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	20	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} ≥ 2.7 V	-	-	50(4)	MHz
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	100(4)	
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	25	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	50	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	42.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} ≥2.7 V	-	-	6	ns
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	4	
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	6	

Table 60. I/O AC characteristics(1)(2) (continued)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	100(4)	MHz
			C_L = 30 pF, V_{DD} ≥ 1.8 V	-	-	50	
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	42.5	
			C_L = 10 pF, V_{DD}≥ 2.7 V	-	-	180(4)	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	100	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	72.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	4	ns
			C_L = 30 pF, V_{DD} ≥1.8 V	-	-	6	
			C_L = 30 pF, V_{DD} ≥1.7 V	-	-	7	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	2.5	
			C_L = 10 pF, V_{DD} ≥1.8 V	-	-	3.5	
			C_L = 10 pF, V_{DD} ≥1.7 V	-	-	4	
-	tEXTIpw	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 40*.
4. For maximum frequencies above 50 MHz and V_{DD} > 2.4 V, the compensation cell should be used.

Figure 40. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 65* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.20* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 65. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data	-	64xFs	
		Slave data	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	0	5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	3.5	-	
		Slave mode PCM short pulse mode(3)	3.5	-	
$t_{h(WS)}$	WS hold time	Slave mode	0.5	-	
		Slave mode PCM short pulse mode(3)	1	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	5	-	
$t_{su(SD\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_SR)}$		Slave receiver	1.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	19	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	2.50	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed based on test during characterization.
2. 128xFs maximum is 24.756 MHz (APB1 Maximum frequency).
3. Measurement done with respect to I2S_CK rising edge.

Note: Refer to the I2S section of RM0386 reference manual for more details on the sampling frequency (F_S).

f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior, source clock precision might slightly change the values. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital

Figure 47. SAI master timing waveforms

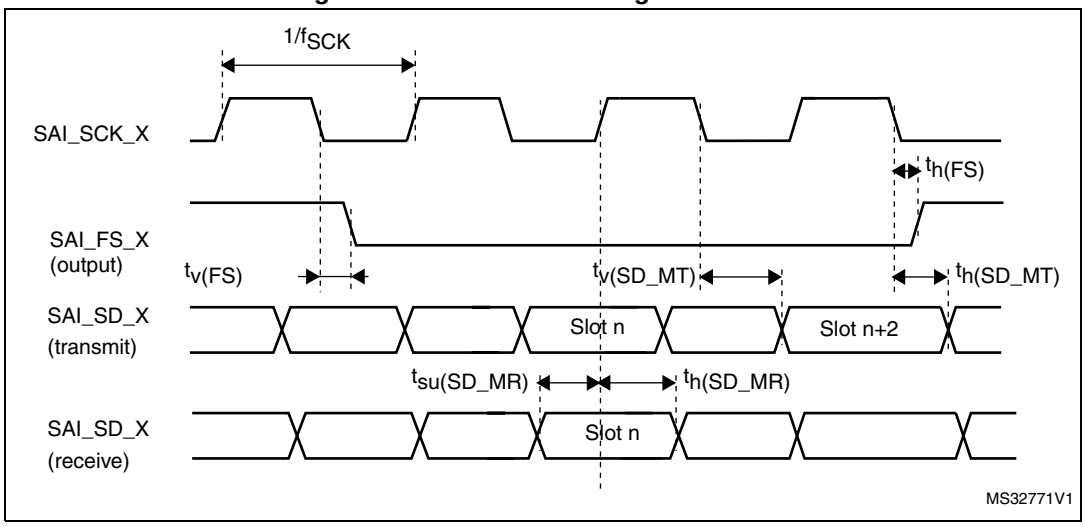


Figure 48. SAI slave timing waveforms

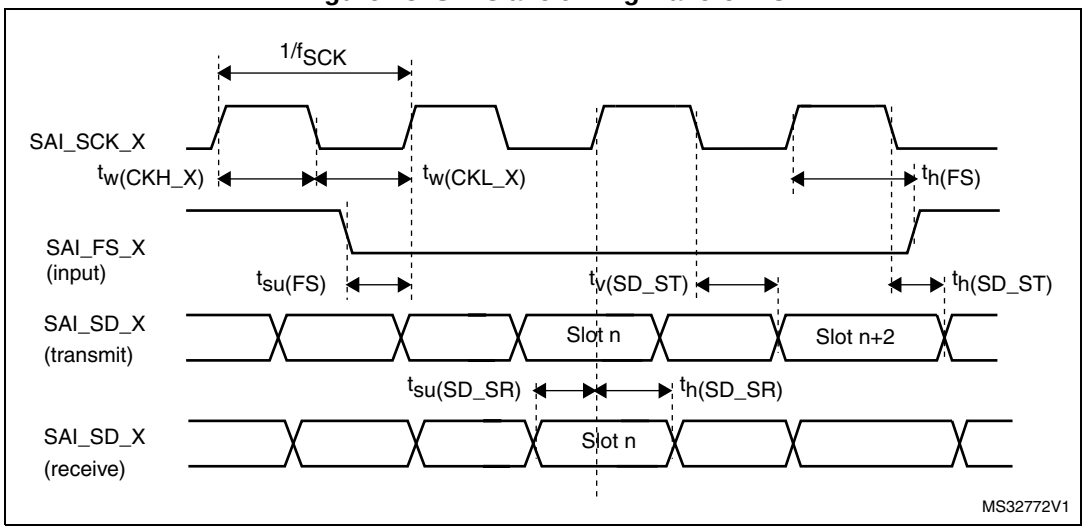
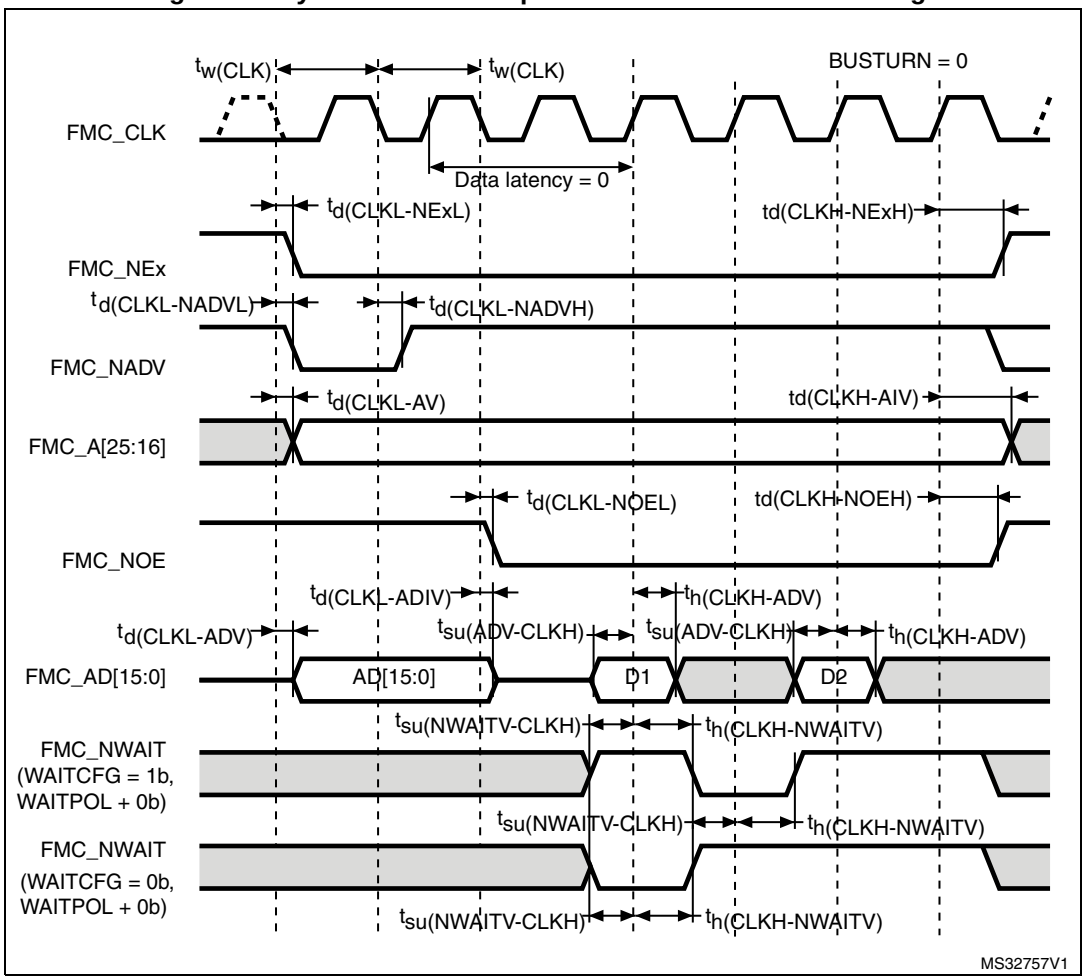


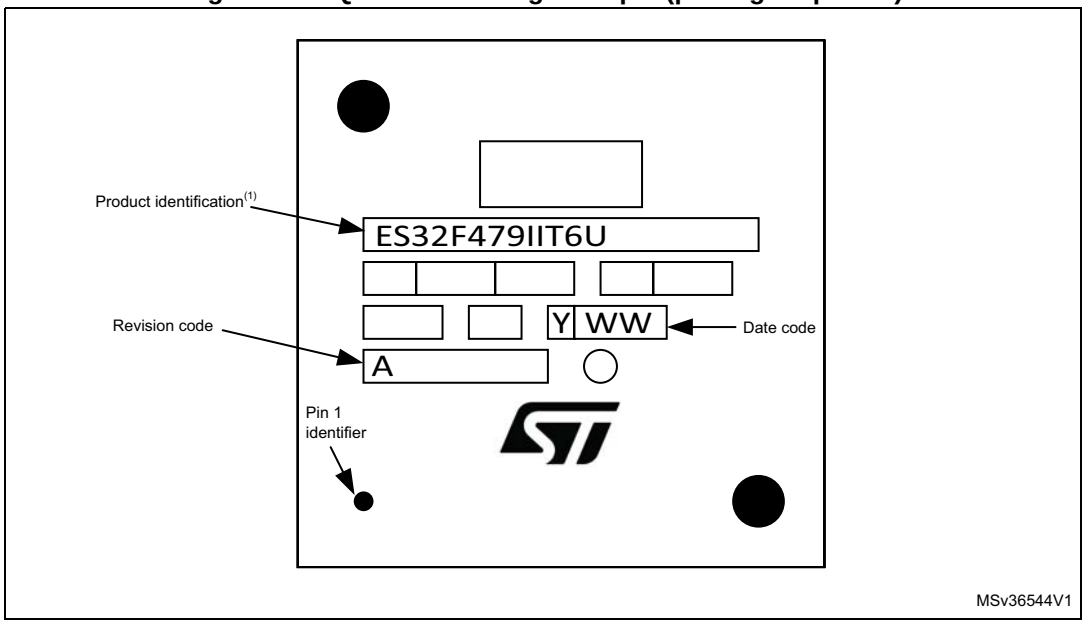
Figure 63. Synchronous multiplexed NOR/PSRAM read timings



Device Marking for LQFP176

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 91. LQFP176 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.