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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	161
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f469neh6">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f469neh6</a>

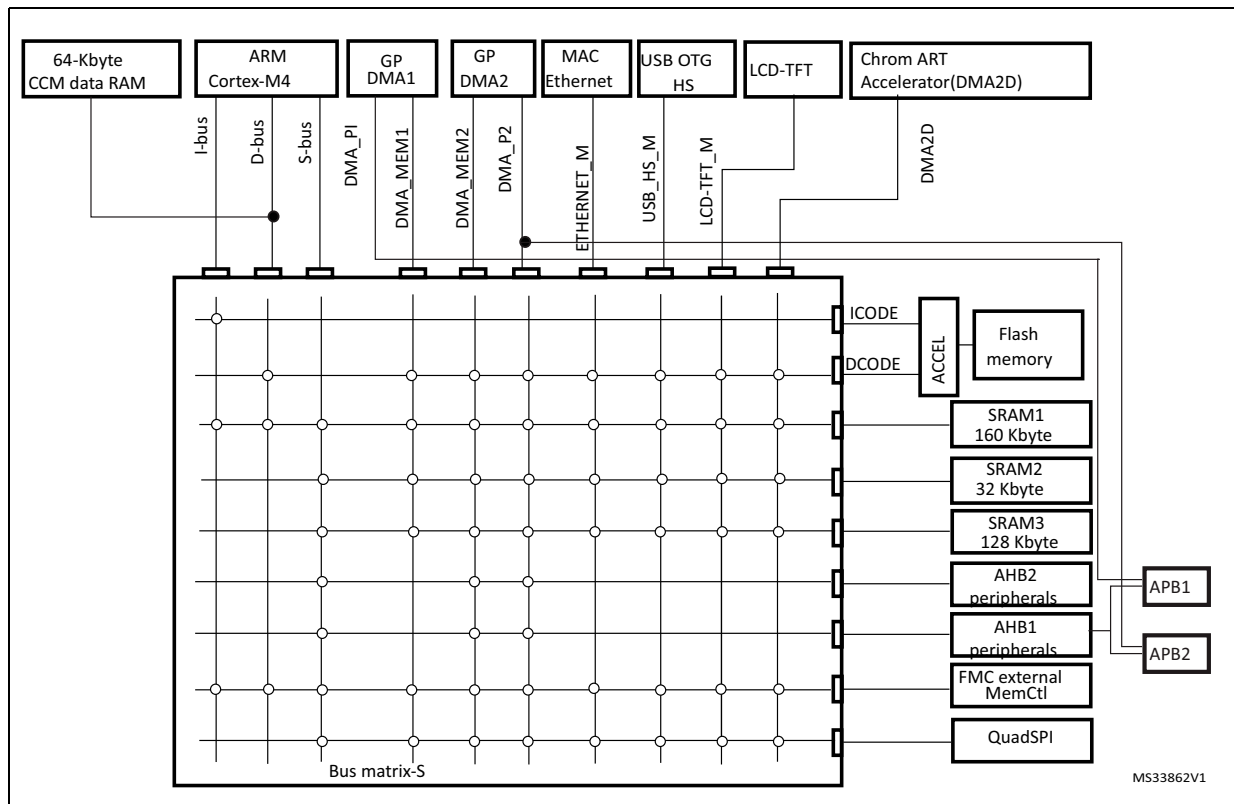
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Figure 6. STM32F469xx Multi-AHB matrix



## 2.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep mode
 

The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.
  - In Stop modes
 

The MR can be configured in two ways during stop mode:  
 MR operates in normal mode (default mode of MR in stop mode)  
 MR operates in under-drive mode (reduced leakage mode).
- LPR is used in the Stop modes:
 

The LP regulator mode is configured by software when entering Stop mode. Like the MR mode, the LPR can be configured in two ways during stop mode:

  - LPR operates in normal mode (default mode when LPR is ON)
  - LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.
 

The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to [Table 3](#) for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> pin. Refer to [Section 2.18](#) and [Table 124](#).

All packages have the regulator ON feature.

**Table 3. Voltage regulator configuration mode versus device operating mode<sup>(1)</sup>**

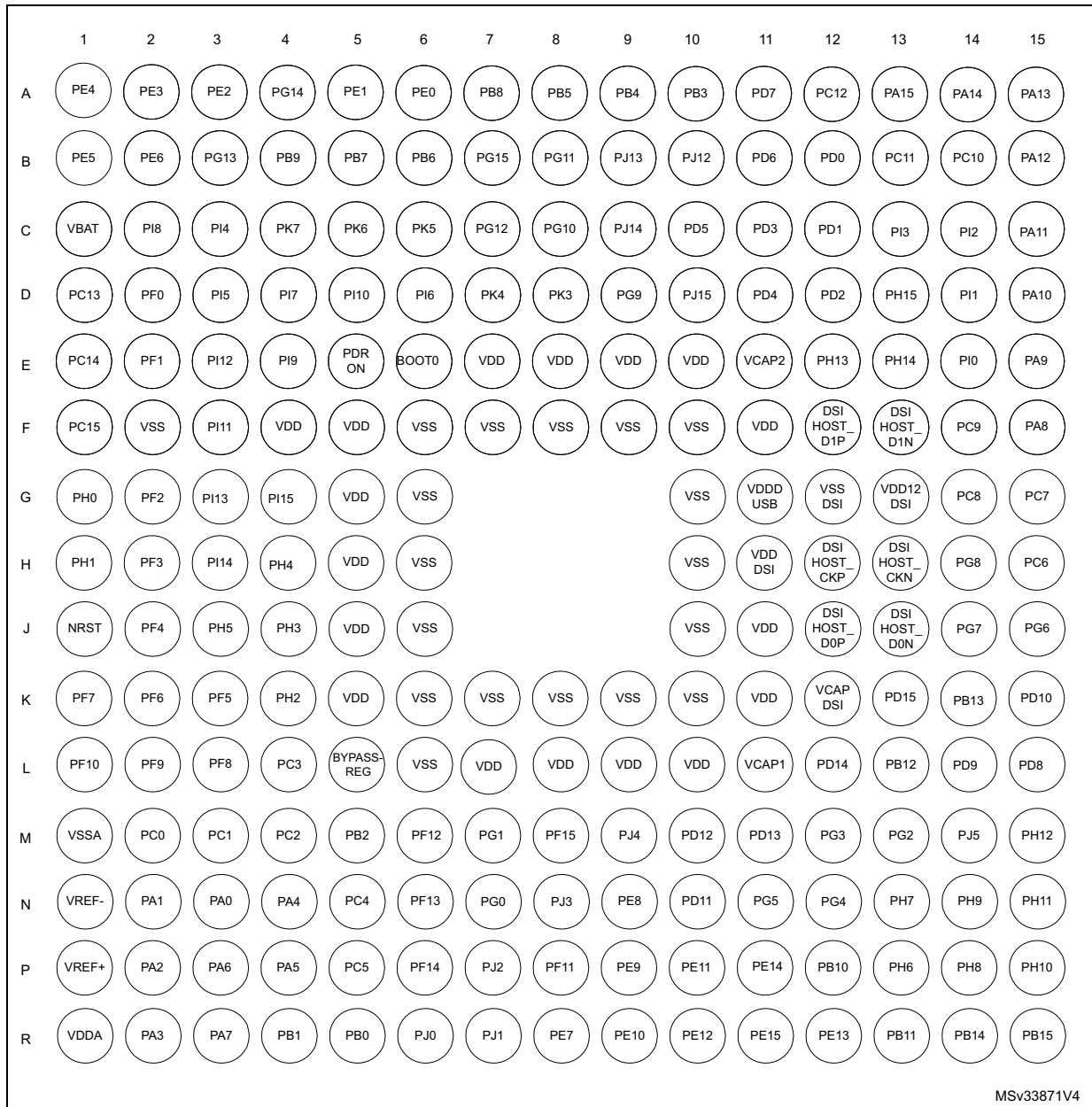
Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode <sup>(2)</sup>	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.  
 2. The over-drive mode is not available when V<sub>DD</sub> = 1.7 to 2.1 V.

### 2.20.2 Regulator OFF

This feature is available only on packages featuring the BYPASS\_REG pin. The regulator is disabled by holding BYPASS\_REG high. The regulator OFF mode allows to supply externally a V<sub>12</sub> voltage source through V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> pins.

Figure 20. STM32F46x TFBGA216 ballout



MSv33871V4

1. The above figure shows the package top view.



Table 10. STM32F469xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	96	D13	G6	H14	116	135	H14	PG8	I/O	FT	-	SPI6_NSS, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	-	G9	F2	G12	117	136	G10	VSS	S	-	-	-	-
65	97	G11	F1	H13	118	137	G11	VDDUSB	S	-	-	-	-
66	98	F9	F3	H15	119	138	H15	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDIO_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
67	99	F10	G7	G15	120	139	G15	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDIO_D7, DCMI_D1, LCD_G6, EVENTOUT	-
68	100	E10	F4	G14	121	140	G14	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, USART6_CK, SDIO_D0, DCMI_D2, EVENTOUT	-
69	101	G10	F5	F14	122	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, QUADSPI_BK1_IO0, SDIO_D1, DCMI_D3, EVENTOUT	-
70	102	D8	E1	F15	123	142	F15	PA8	I/O	FT	-	MCO1, TIM1_CH1, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT	-
71	103	E8	E2	E15	124	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, EVENTOUT	OTG_FS_ VBUS
72	104	E9	E3	D15	125	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT	-
73	105	A13	F7	C15	126	145	C15	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-
74	106	A12	F6	B15	127	146	B15	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
75	107	A11	D1	A15	128	147	A15	PA13(JTMS- SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
76	108	D12	D2	F13	129	148	E11	VCAP2	S	-	-	-	-
-	109	D11	C1	F12	130	149	F10	VSS	S	-	-	-	-



Table 10. STM32F469xx pin and ball definitions (continued)

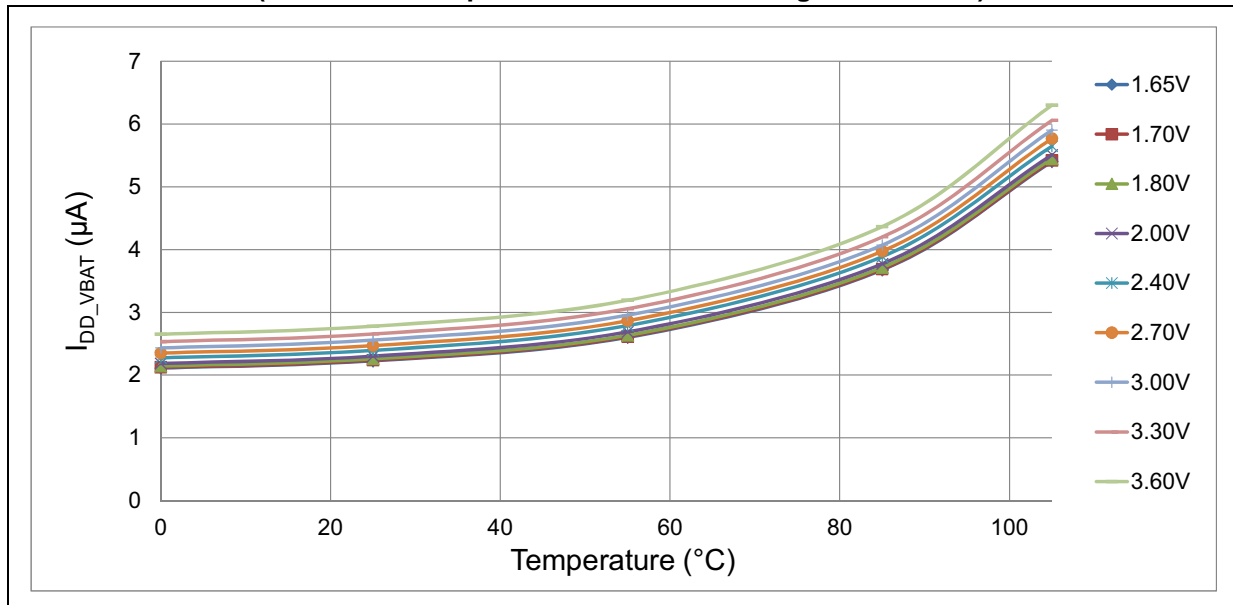
Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
77	110	D10	C2	G13	131	150	F11	VDD	S	-	-	-	-
-	-	D9	B1	-	-	151	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	C13	D3	-	-	152	E13	PH14	I/O	FT	-	TIM8_CH2N, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	C12	E4	-	-	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	B13	E5	E14	132	154	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS <sup>(7)</sup> , FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	C11	C3	D14	133	155	D14	PI1	I/O	FT	-	SPI2_SCK/I2S2_CK <sup>(7)</sup> , FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	B12	A1	-	NC (2)	156	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, I2S2ext_SD, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
-	-	B10	B2	C13	134	157	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT	-
78	-	-	-	D9	135	-	F9	VSS	S	-	-	-	-
-	-	-	B5	C9	136	158	E10	VDD	S	-	-	-	-
79	111	A10	D4	A14	137	159	A14	PA14(JTCK- SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
80	112	B11	A2	A13	138	160	A13	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS, SPI3_NSS/I2S3_WS, EVENTOUT	-
81	113	C10	D5	B14	139	161	B14	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDIO_D2, DCMI_D8, LCD_R2, EVENTOUT	-
82	114	B9	B3	B13	140	162	B13	PC11	I/O	FT	-	I2S3ext_SD, SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDIO_D3, DCMI_D4, EVENTOUT	-



**Table 12. Alternate function (continued)**

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI/HOST	LCD	SYS
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENT OUT
	PI1	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	FMC_D25	DCMI_D8	LCD_G6	EVENT OUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENT OUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	FMC_D27	DCMI_D10		EVENT OUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	FMC_NBL2	DCMI_D5	LCD_B4	EVENT OUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	-	FMC_NBL3	DCMI_VSYNCR	LCD_B5	EVENT OUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	FMC_D28	DCMI_D6	LCD_B6	EVENT OUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	-	FMC_D29	DCMI_D7	LCD_B7	EVENT OUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-		EVENT OUT
	PI9	-	-	-	-	-	-	-	-	-	CAN1_RX	-	FMC_D30	-	LCD_VSYNCR	EVENT OUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RX_ER	FMC_D31	LCD_HSYNCR	EVENT OUT
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-	-	-	EVENT OUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNCR	EVENT OUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNCR	EVENT OUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENT OUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	LCD_R0	EVENT OUT

**Figure 28. Typical  $V_{BAT}$  current consumption (RTC ON / backup SRAM ON and LSE in High drive mode)**



**I/O system current consumption**

The current consumption of the I/O system has two components: static and dynamic.

**I/O static current consumption**

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 58: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

**I/O dynamic current consumption**

In addition to the internal peripheral current consumption (see [Table 33](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses

the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$  is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$  is the MCU supply voltage

$f_{SW}$  is the I/O switching frequency

$C$  is the total capacitance seen by the I/O pin:  $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

**Table 32. Switching output I/O current consumption<sup>(1)</sup>**

Symbol	Parameter	Conditions	I/O toggling frequency (fsw)	Typ	Unit
I <sub>DDIO</sub>	I/O switching Current	V <sub>DD</sub> = 3.3 V C = C <sub>INT</sub> <sup>(2)</sup>	2 MHz	0.0	mA
			8 MHz	0.2	
			25 MHz	0.6	
			50 MHz	1.1	
			60 MHz	1.3	
			84 MHz	1.8	
			90 MHz	1.9	
		V <sub>DD</sub> = 3.3 V C <sub>EXT</sub> = 0 pF C = C <sub>INT</sub> + C <sub>EXT</sub> + C <sub>S</sub>	2 MHz	0.1	
			8 MHz	0.4	
			25 MHz	1.23	
			50 MHz	2.43	
			60 MHz	2.93	
			84 MHz	3.86	
			90 MHz	4.07	

### 5.3.16 Memory characteristics

#### Flash memory

The characteristics are given at  $T_A = -40$  to  $105$  °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

**Table 49. Flash memory characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD}$	Supply current	Write / Erase 8-bit mode, $V_{DD} = 1.7$ V	-	5	-	mA
		Write / Erase 16-bit mode, $V_{DD} = 2.1$ V	-	8	-	
		Write / Erase 32-bit mode, $V_{DD} = 3.3$ V	-	12	-	

**Table 50. Flash memory programming**

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Unit
$t_{prog}$	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100 <sup>(2)</sup>	$\mu$ s
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	

**Table 55. ESD absolute maximum ratings**

Symbol	Ratings	Conditions	Class	Maximum value <sup>(1)</sup>	Unit
V <sub>ESD(HBM)</sub>	Electrostatic discharge voltage (human body model)	T <sub>A</sub> = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
V <sub>ESD(CDM)</sub>	Electrostatic discharge voltage (charge device model)	T <sub>A</sub> = +25 °C conforming to ANSI/ESD S5.3.1, LQFP100, LQFP144, LQFP176, LQFP208, UFBGA169, UFBGA176, TFBGA216 and WLCSP148 packages	C3	250	

1. Guaranteed based on test during characterization.

**Static latchup**

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

**Table 56. Electrical sensitivities<sup>(1)</sup>**

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T <sub>A</sub> = +105 °C conforming to JESD78A	II level A

1. MSV on PA4 and PA5 is 5 V, versus 5.4 V on all IOs.

**5.3.19 I/O current injection characteristics**

As a general rule, current injection to the I/O pins, due to external voltage below V<sub>SS</sub> or above V<sub>DD</sub> (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

**Functional susceptibility to I/O current injection**

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of – 5 μA/+0 μA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in [Table 57](#).

### 5.3.22 TIM timer characteristics

The parameters given in [Table 62](#) are guaranteed by design. Refer to [Section 5.3.20](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 62. TIMx characteristics<sup>(1)(2)</sup>**

Symbol	Parameter	Conditions <sup>(3)</sup>	Min	Max	Unit
t <sub>res(TIM)</sub>	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, f <sub>TIMxCLK</sub> = 180 MHz	1	-	t <sub>TIMxCLK</sub>
		AHB/APBx prescaler>4, f <sub>TIMxCLK</sub> = 90 MHz	1	-	t <sub>TIMxCLK</sub>
f <sub>EXT</sub>	Timer external clock frequency on CH1 to CH4	f <sub>TIMxCLK</sub> = 180 MHz	0	f <sub>TIMxCLK</sub> /2	MHz
Res <sub>TIM</sub>	Timer resolution		-	16/32	bit
t <sub>MAX_COUNT</sub>	Maximum possible count with 32-bit counter		-	65536 × 65536	t <sub>TIMxCLK</sub>

1. TIMx is used as a general term to refer to the TIM1 to TIM12 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 180 MHz, by setting the TIMPRE bit in the RCC\_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK = 4x PCLKx.

### 5.3.23 Communications interfaces

#### I<sup>2</sup>C interface characteristics

The I<sup>2</sup>C interface meets the timings requirements of the I<sup>2</sup>C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.

The I<sup>2</sup>C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0386 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V<sub>DD</sub> is disabled, but is still present. Refer to [Section 5.3.20](#) for more details on the I<sup>2</sup>C I/O characteristics.

All I<sup>2</sup>C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

**Table 63. I2C analog filter characteristics<sup>(1)</sup>**

Symbol	Parameter	Min	Max	Unit
t <sub>AF</sub>	Maximum pulse width of spikes that are suppressed by the analog filter	50 <sup>(2)</sup>	150 <sup>(3)</sup>	ns



Table 85. internal reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{\text{Coeff}}^{(2)}$	Temperature coefficient		-	30	50	ppm/°C
$t_{\text{START}}^{(2)}$	Startup time		-	6	10	µs

- Shortest sampling time can be determined in the application by multiple iterations.
- Guaranteed by design

Table 86. Internal reference voltage calibration values

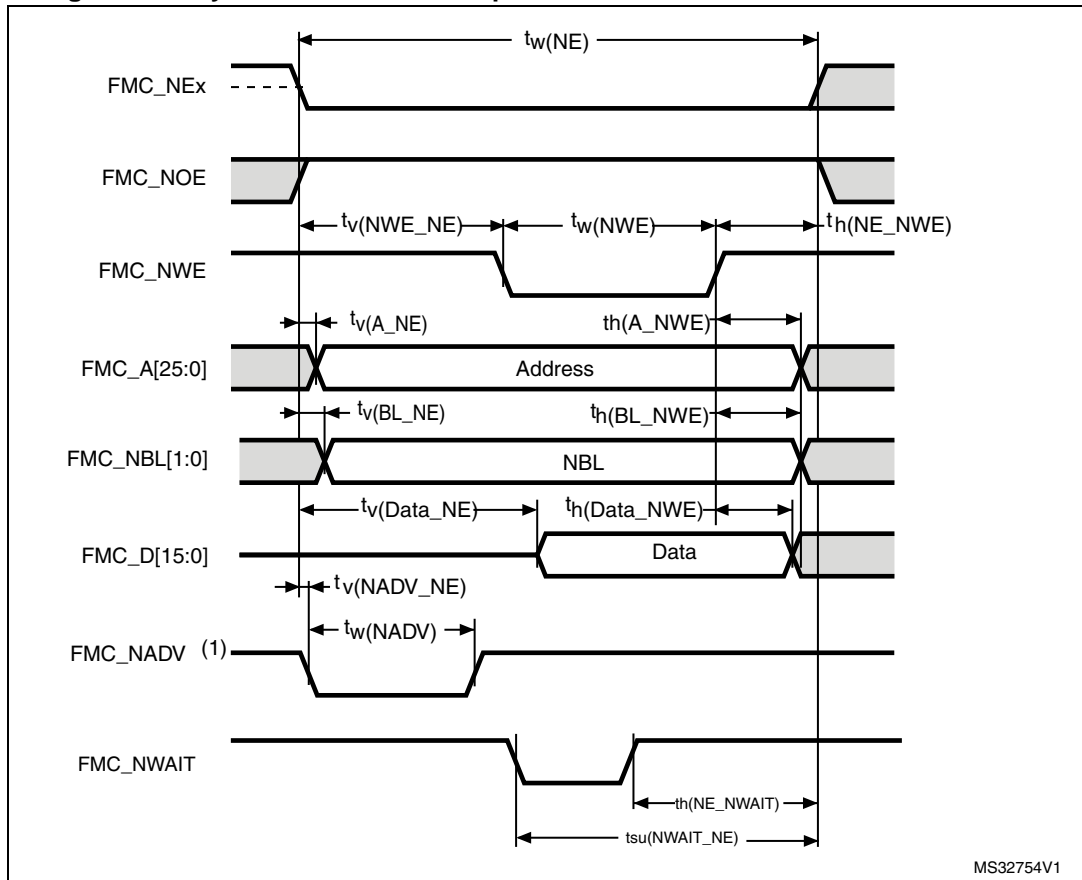
Symbol	Parameter	Memory address
$V_{\text{REFIN\_CAL}}$	Raw data acquired at temperature of 30 °C $V_{\text{DDA}} = 3.3 \text{ V}$	0x1FFF 7A2A - 0x1FFF 7A2B

### 5.3.28 DAC electrical characteristics

Table 87. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
$V_{\text{DDA}}$	Analog supply voltage	1.7 <sup>(1)</sup>	-	3.6	V	-
$V_{\text{REF+}}$	Reference supply voltage	1.7 <sup>(1)</sup>	-	3.6	V	$V_{\text{REF+}} \leq V_{\text{DDA}}$
$V_{\text{SSA}}$	Ground	0	-	0	V	-
$R_{\text{LOAD}}^{(2)}$	Resistive load with buffer ON	5	-	-	kΩ	-
$R_{\text{O}}^{(2)}$	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{\text{SS}}$ to have a 1% accuracy is 1.5 MΩ
$C_{\text{LOAD}}^{(2)}$	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
$\text{DAC\_OUT}_{\text{min}}^{(2)}$	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{\text{REF+}} = 3.6 \text{ V}$ and (0x1C7) to (0xE38) at $V_{\text{REF+}} = 1.7 \text{ V}$
$\text{DAC\_OUT}_{\text{max}}^{(2)}$	Higher DAC_OUT voltage with buffer ON	-	-	$V_{\text{DDA}} - 0.2$	V	
$\text{DAC\_OUT}_{\text{min}}^{(2)}$	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
$\text{DAC\_OUT}_{\text{max}}^{(2)}$	Higher DAC_OUT voltage with buffer OFF	-	-	$V_{\text{REF+}} - 1\text{LSB}$	V	
$I_{\text{VREF+}}^{(4)}$	DAC DC $V_{\text{REF}}$ current consumption in quiescent mode (Standby mode)	-	170	240	µA	With no load, worst code (0x800) at $V_{\text{REF+}} = 3.6 \text{ V}$ in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at $V_{\text{REF+}} = 3.6 \text{ V}$ in terms of DC consumption on the inputs

Figure 60. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC\_NADV is not used.

Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings<sup>(1)</sup>

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+1$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{HCLK}$	$T_{HCLK} + 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{HCLK} + 1.5$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{HCLK} + 2$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK} + 0.5$	

1. Based on test during characterization.

### 5.3.30 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 106](#) and [Table 107](#) for Quad-SPI are derived from tests performed under the ambient temperature,  $f_{\text{AHB}}$  frequency and  $V_{\text{DD}}$  supply voltage conditions summarized in Table xx, with the following configuration:

- Output speed is set to  $\text{OSPEEDRy}[1:0] = 11$
- Measurement points are done at CMOS levels:  $0.5 V_{\text{DD}}$

Refer to [Section 5.3.20](#) for more details on the input/output alternate function characteristics.

**Table 106. Quad-SPI characteristics in SDR mode<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$F_{\text{ck}}$ $1/t_{(\text{CK})}$	Quad-SPI clock frequency	$2.7 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}, C_{\text{L}} = 20 \text{ pF}$	-	-	90	MHz
		$1.71 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}, C_{\text{L}} = 15 \text{ pF}$	-	-	84	
$t_{\text{w}(\text{CKH})}$	Quad-SPI clock high time	-	$t_{(\text{CK})}/2-1$	-	$t_{(\text{CK})}/2$	ns
$t_{\text{w}(\text{CKL})}$	Quad-SPI clock low time	-	$t_{(\text{CK})}/2$	-	$t_{(\text{CK})}/2+1$	
$t_{\text{s}(\text{IN})}$	Data input set-up time	-	0.5	-	-	
$t_{\text{h}(\text{IN})}$	Data input hold time	-	3	-	-	
$t_{\text{v}(\text{OUT})}$	Data output valid time	-	-	3	4	
$t_{\text{h}(\text{OUT})}$	Data output hold time	-	2.5	-	-	

1. Guaranteed based on test during characterization.

**Figure 73. Quad-SPI SDR timing diagram**

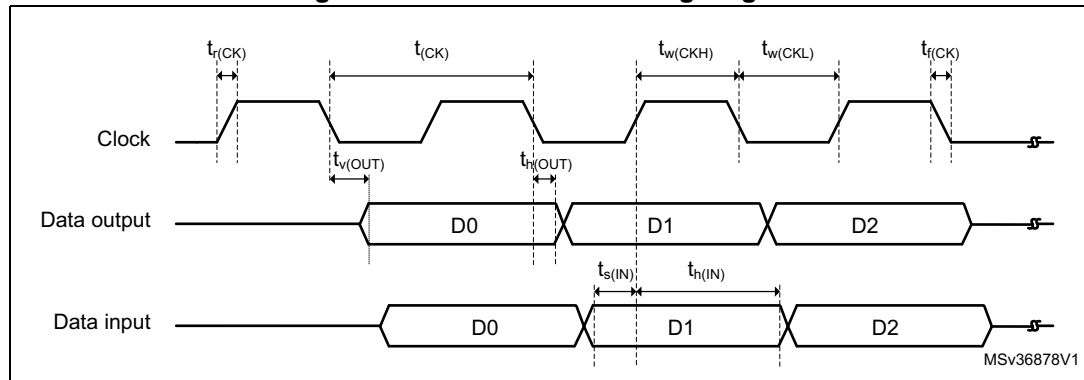


Table 113. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

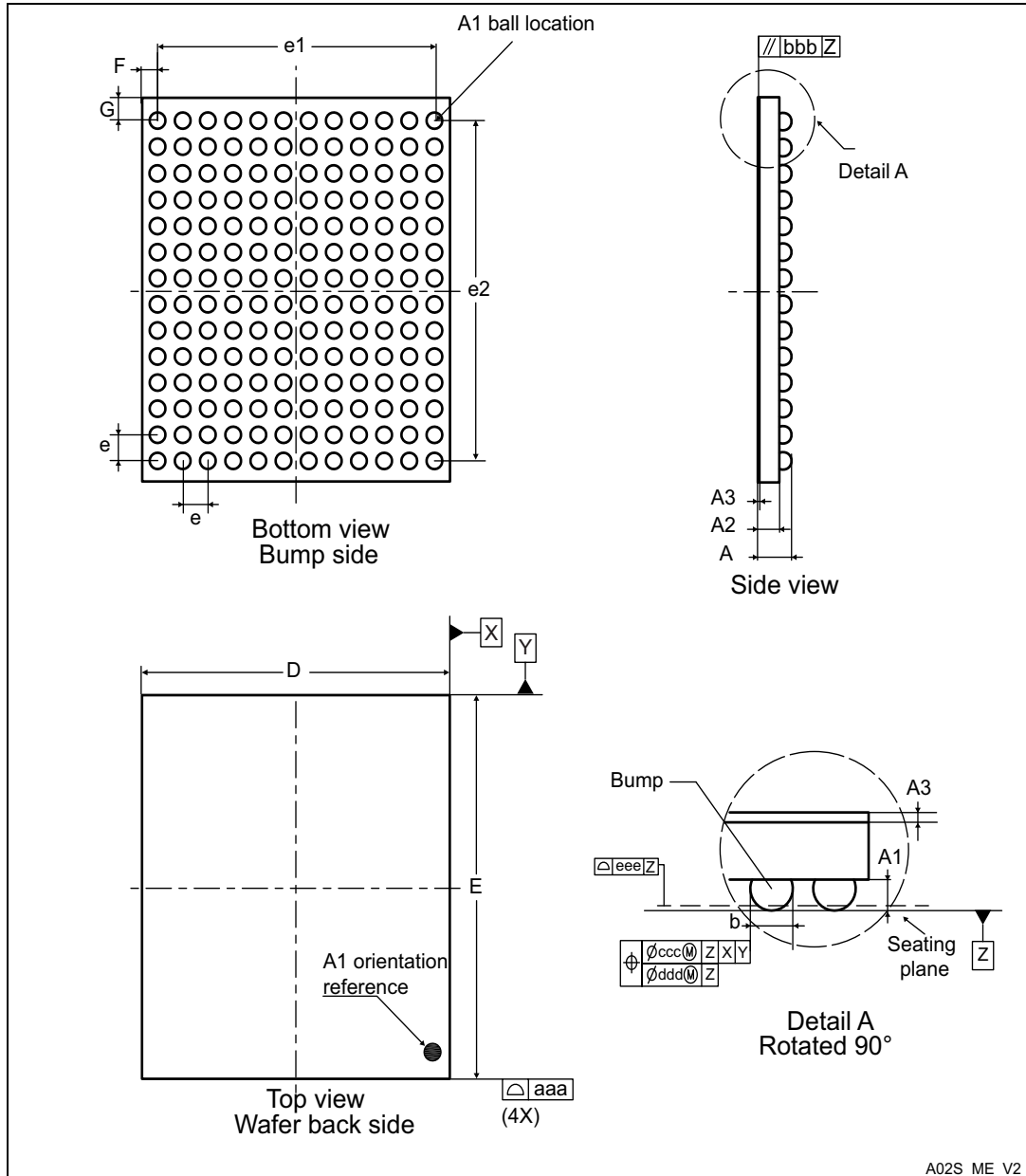
Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

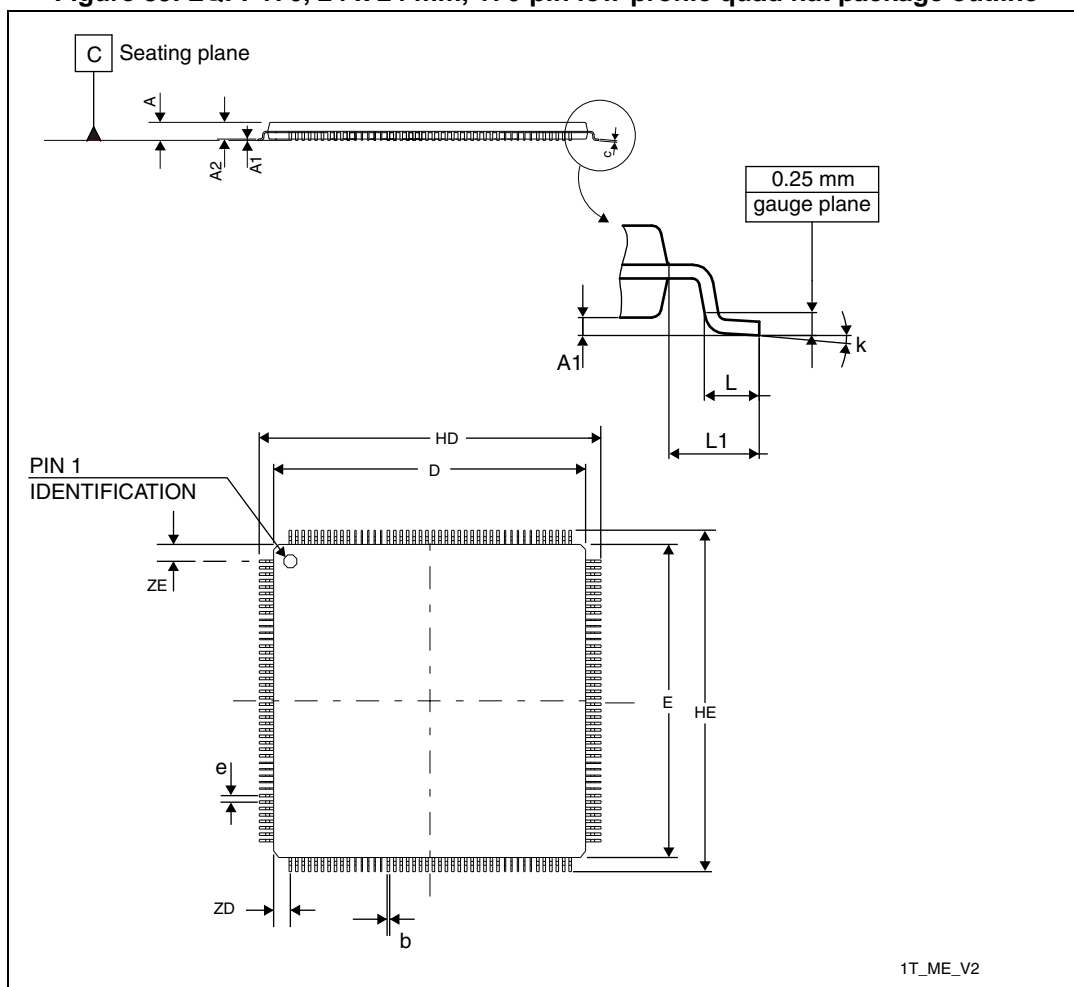
### 6.3 WLCSP168 package information

Figure 86. WLCSP168 - 168-pin, 4.891 x 5.692 mm, 0.4 mm pitch wafer level chip scale package outline



### 6.5 LQFP176 package information

Figure 89. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 117. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0060
b	0.170	-	0.270	0.0067	-	0.0106
C	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488
E	23.900	-	24.100	0.9409	-	0.9488