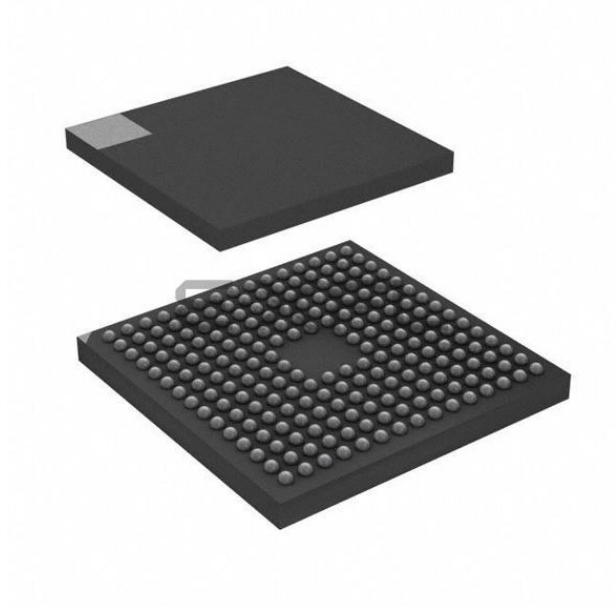

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	161
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f469nih6

Contents

2.10 Quad-SPI memory interface (QUADSPI)

All STM32F469xx devices embeds a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual, Quad or Dual-flash SPI memories. It can work in direct mode through registers, external flash status register polling mode and memory mapped mode. Up to 256 Mbytes external Flash memory are mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. Communication can be either in Single Data Rate or Dual Data Rate.

2.11 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

2.12 DSI Host (DSIHOST)

The DSI Host is a dedicated peripheral for interfacing with MIPI® DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

These interfaces are as follows:

- LTDC interface:
  - Used to transmit information in Video Mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI).
  - Through a customized for mode, this interface can be used to transmit information in full bandwidth in the Adapted Command Mode (DBI).
- APB slave interface:
  - Allows the transmission of generic information in Command mode, and follows a proprietary register interface.
  - Can operate concurrently with either LTDC interface in either Video Mode or Adapted Command Mode.
- Video mode pattern generator:
  - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli.

communicate at speeds of up to 11.25 Mbit/s. The other available interfaces communicate at up to 5.62 bit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 8. USART feature comparison(1)

Name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s		APB mapping
							Oversampling by 16	Oversampling by 8	
USART1	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
USART2	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
USART3	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
UART4	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART5	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
USART6	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
UART7	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART8	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)

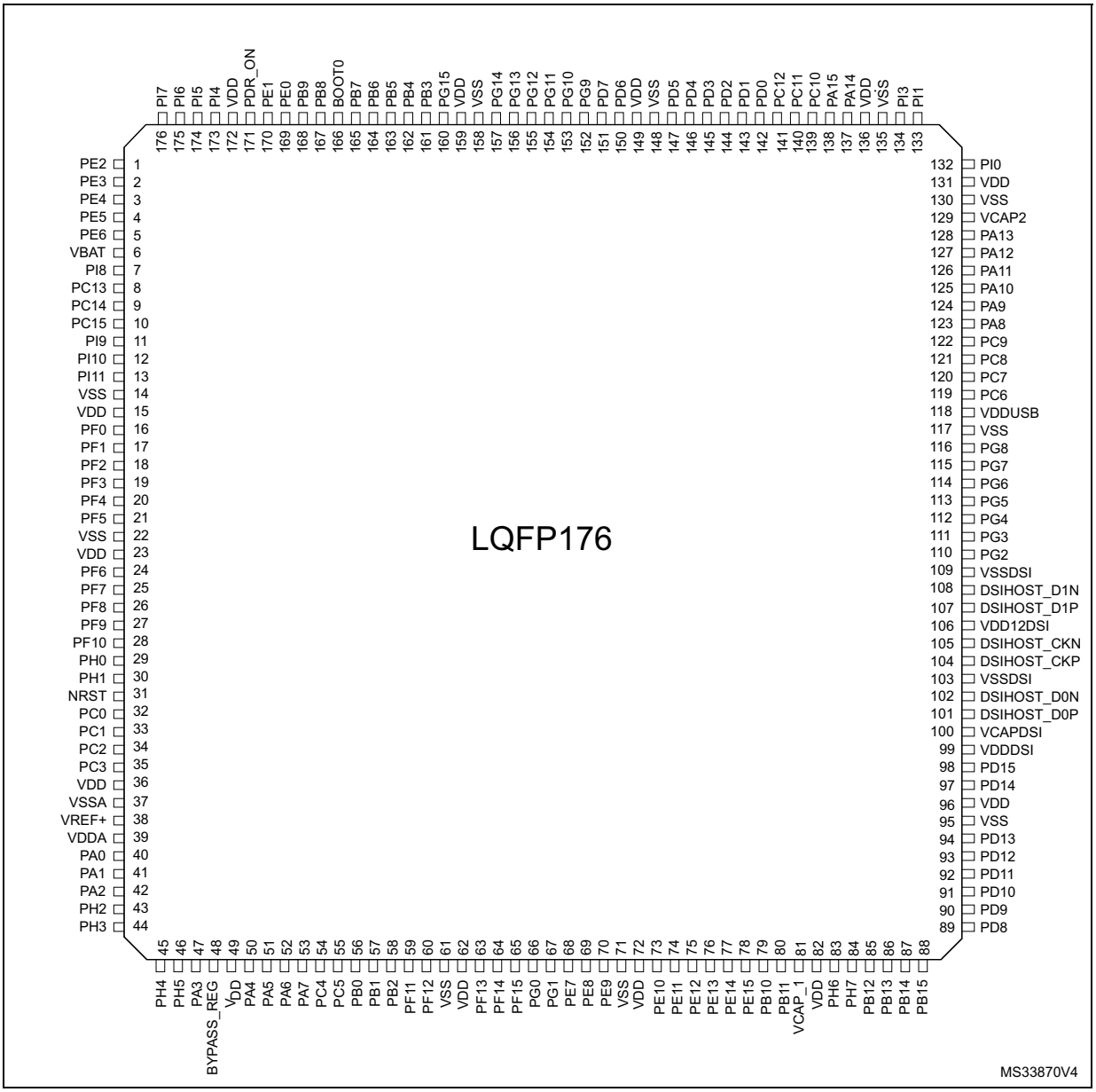
1. X = feature supported.

2.27 Serial peripheral interface (SPI)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 45 Mbits/s, SPI2 and SPI3 can communicate at up to 22.5 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

Figure 18. STM32F46x LQFP176 pinout



1. The above figure shows the package top view.

Table 10. STM32F469xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	96	D13	G6	H14	116	135	H14	PG8	I/O	FT	-	SPI6_NSS, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	-	G9	F2	G12	117	136	G10	VSS	S	-	-	-	-
65	97	G11	F1	H13	118	137	G11	VDDUSB	S	-	-	-	-
66	98	F9	F3	H15	119	138	H15	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDIO_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
67	99	F10	G7	G15	120	139	G15	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDIO_D7, DCMI_D1, LCD_G6, EVENTOUT	-
68	100	E10	F4	G14	121	140	G14	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, USART6_CK, SDIO_D0, DCMI_D2, EVENTOUT	-
69	101	G10	F5	F14	122	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, QUADSPI_BK1_IO0, SDIO_D1, DCMI_D3, EVENTOUT	-
70	102	D8	E1	F15	123	142	F15	PA8	I/O	FT	-	MCO1, TIM1_CH1, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT	-
71	103	E8	E2	E15	124	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, EVENTOUT	OTG_FS_ VBUS
72	104	E9	E3	D15	125	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT	-
73	105	A13	F7	C15	126	145	C15	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-
74	106	A12	F6	B15	127	146	B15	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
75	107	A11	D1	A15	128	147	A15	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
76	108	D12	D2	F13	129	148	E11	VCAP2	S	-	-	-	-
-	109	D11	C1	F12	130	149	F10	VSS	S	-	-	-	-

Table 10. STM32F469xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
77	110	D10	C2	G13	131	150	F11	VDD	S	-	-	-	-
-	-	D9	B1	-	-	151	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	C13	D3	-	-	152	E13	PH14	I/O	FT	-	TIM8_CH2N, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	C12	E4	-	-	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	B13	E5	E14	132	154	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS(7), FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	C11	C3	D14	133	155	D14	PI1	I/O	FT	-	SPI2_SCK/I2S2_CK(7), FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	B12	A1	-	NC (2)	156	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, I2S2ext_SD, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
-	-	B10	B2	C13	134	157	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT	-
78	-	-	-	D9	135	-	F9	VSS	S	-	-	-	-
-	-	-	B5	C9	136	158	E10	VDD	S	-	-	-	-
79	111	A10	D4	A14	137	159	A14	PA14(JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
80	112	B11	A2	A13	138	160	A13	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS, SPI3_NSS/I2S3_WS, EVENTOUT	-
81	113	C10	D5	B14	139	161	B14	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDIO_D2, DCMI_D8, LCD_R2, EVENTOUT	-
82	114	B9	B3	B13	140	162	B13	PC11	I/O	FT	-	I2S3ext_SD, SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDIO_D3, DCMI_D4, EVENTOUT	-

Table 12. Alternate function

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI HOST	LCD	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENT OUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	QUADSPI_BK1_IO3	-	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	LCD_R2	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	-	-	-	ETH_MDIO	-	-	LCD_R1	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	LCD_B2	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENT OUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENT OUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	-	OTG_HS_ULPI_CK	-	-	-	LCD_R4	EVENT OUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCLK	LCD_G2	EVENT OUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	QUADSPI_CLK	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FMC_SDNWE	-	-	EVENT OUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	LCD_R6	EVENT OUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	-	-	-	DCMI_D0	-	EVENT OUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENT OUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVENT OUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVENT OUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	-	-	-	-	-	-	-	-	EVENT ‘OUT

5.3 Operating conditions

5.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions[1]		Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF		0	-	120	MHz
		Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	Over-drive OFF	0	-	144	
			Over-drive ON		-	168	
		Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON	Over-drive OFF	0	-	168	
			Over-drive ON		-	180	
f_{PCLK1}	Internal APB1 clock frequency	Over-drive OFF		0	-	42	
		Over-drive ON		0	-	45	
f_{PCLK2}	Internal APB2 clock frequency	Over-drive OFF		0	-	84	
		Over-drive ON		0	-	90	
V_{DD}	Standard operating voltage	-		1.7[2]	-	3.6	V
V_{DDA}[3][4]	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}[5]		1.7[2]	-	2.4	
	Analog operating voltage (ADC limited to 2.4 M samples)			2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11, PA12, PB14 and PB15 pins)	USB not used		1.7	3.3	3.6	
		USB used		3.0	-	3.6	
V_{DDDSI}	DSI system operating voltage	-		1.7[2]	-	3.6	
V_{BAT}	Backup operating voltage	-		1.65	-	3.6	

Table 17. General operating conditions (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{12}	Regulator ON: 1.2 V internal voltage on V_{CAP_1}/V_{CAP_2} pins	Power Scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 120 MHz HCLK max frequency	1.08	1.14	1.20	V
		Power Scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 144 MHz HCLK max frequency with over-drive OFF or 168 MHz with over-drive ON	1.20	1.26	1.32	
		Power Scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON	1.26	1.32	1.40	
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V_{CAP_1}/V_{CAP_2} pins[6]	Max frequency 120 MHz	1.10	1.14	1.20	
		Max frequency 144 MHz	1.20	1.26	1.32	
		Max frequency 168 MHz	1.26	1.32	1.38	
V_{IN}	Input voltage on RST and FT pins[7]	2 V ≤V_{DD} ≤3.6 V	− 0.3	-	5.5	V
		V_{DD} ≤2 V	− 0.3	-	5.2	
	Input voltage on TTa pins	-	− 0.3	-	V_{DDA} +0.3	
	Input voltage on BOOT0 pin	-	0	-	9	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7[8]	LQFP100	-	-	465	mW
		LQFP144	-	-	500	
		WLCSP168	-	-	645	
		UFBGA169	-	-	385	
		LQFP176	-	-	526	
		UFBGA176	-	-	513	
		LQFP208	-	-	1053	
		TFBGA216	-	-	690	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	− 40	-	85	°C
		Low power dissipation[9]	− 40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	− 40	-	105	
		Low power dissipation[9]	− 40	-	125	
T_J	Junction temperature range	6 suffix version	− 40	-	105	
		7 suffix version	− 40	-	125	

1. The over-drive mode is not supported at the voltage ranges from 1.7 to 2.1 V.
2. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.19.2*).
3. When the ADC is used, refer to *Table 76*.
4. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.
5. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
6. The over-drive mode is not supported when the internal regulator is OFF.

Table 33. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
APB1 (up to 45 MHz)	TIM2	19.11	17.56	15.33	µA/MHz
	TIM3	15.62	14.22	12.17	
	TIM4	16.22	14.64	12.83	
	TIM5	18.44	16.72	14.00	
	TIM6	3.18	2.69	2.17	
	TIM7	3.11	2.56	2.00	
	TIM12	8.67	7.56	6.50	
	TIM13	6.11	5.33	4.43	
	TIM14	6.44	5.61	4.67	
	PWR	17.44	15.61	13.53	
	USART2	5.44	4.64	3.93	
	USART3	5.51	4.72	4.00	
	UART4	5.22	4.64	3.83	
	UART5	5.33	4.64	3.83	
	UART7	5.56	4.78	4.10	
	UART8	5.24	4.64	3.93	
	I2C1	4.78	4.08	3.43	
	I2C2	5.11	4.50	3.73	
	I2C3	4.78	4.08	3.43	
	SPI2/I2S2(4)	4.11	3.53	3.00	
	SPI3/I2S3(4)	4.33	3.67	3.17	
	CAN1	8.89	7.83	6.87	
	CAN2	7.22	6.44	5.50	
	DAC(5)	2.89	2.69	2.40	
	WWDG	1.73	1.44	1.00	

Table 33. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
APB2 (up to 90 MHz)	SDIO	7.94	7.18	6.37	µA/MHz
	TIM1	19.44	17.81	15.80	
	TIM8	19.44	17.81	15.80	
	TIM9	8.44	7.60	6.77	
	TIM10	5.67	5.03	4.50	
	TIM11	5.72	5.10	4.55	
	ADC1(6)	5.06	4.54	4.05	
	ADC2(6)	5.00	4.47	3.97	
	ADC3(6)	5.26	4.75	4.17	
	USART1	4.83	4.33	3.83	
	USART6	4.83	4.33	3.83	
	SPI1	2.11	1.76	1.60	
	SPI4	2.11	1.69	1.60	
	SPI5	2.11	1.76	1.60	
	SPI6	2.11	1.76	1.60	
	SYSCFG	1.72	1.35	1.22	
	LTDC	37.61	34.53	30.60	
	SAI1	3.44	3.01	2.72	
	DSI	32.98	30.32	26.87	

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. DMA1/DMA2 current consumption is calculated by the equation. N: is the number of streams enabled, N= [1..8]
3. The BusMatrix is automatically active when at least one master is ON.
4. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
5. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.8 mA per DAC channel for the analog part.
6. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

Table 55. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD S5.3.1, LQFP100, LQFP144, LQFP176, LQFP208, UFBGA169, UFBGA176, TFBGA216 and WLCSP148 packages	C3	250	

1. Guaranteed based on test during characterization.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 56. Electrical sensitivities(1)

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

1. MSV on PA4 and PA5 is 5 V, versus 5.4 V on all IOs.

5.3.19 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 57*.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 66* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.20* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 66. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCKL}	SAI Main clock output	-	256 x 8K	256xFs	MHz
f_{CK}	SAI clock frequency(2)	Master data: 32 bits	-	128xFs(3)	
		Slave data: 32 bits	-	128xFs	
$t_{v(FS)}$	FS valid time	Master mode, 2.7V ≤ V_{DD} ≤ 3.6V	-	17	ns
		Master mode, 1.71V ≤ V_{DD} ≤ 3.6V	-	23	
$t_{su(FS)}$	FS setup time	Slave mode	10	-	
$t_{h(FS)}$	FS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	6	-	
$t_{h(SD\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge), 2.7V ≤ V_{DD} ≤ 3.6V	-	14	
		Slave transmitter (after enable edge), 1.71V ≤ V_{DD} ≤ 3.6V	-	23	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge), 2.7V ≤ V_{DD} ≤ 3.6V	-	20	
		Master transmitter (after enable edge), 1.71V ≤ V_{DD} ≤ 3.6V	-	26	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	

1. Guaranteed based on test during characterization.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With Fs = 192 kHz.

Table 91. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}+1$	$8T_{HCLK}+2$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK}-1$	$6T_{HCLK}+2$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$	-	

1. Based on test during characterization.

Figure 61. Asynchronous multiplexed PSRAM/NOR read waveforms

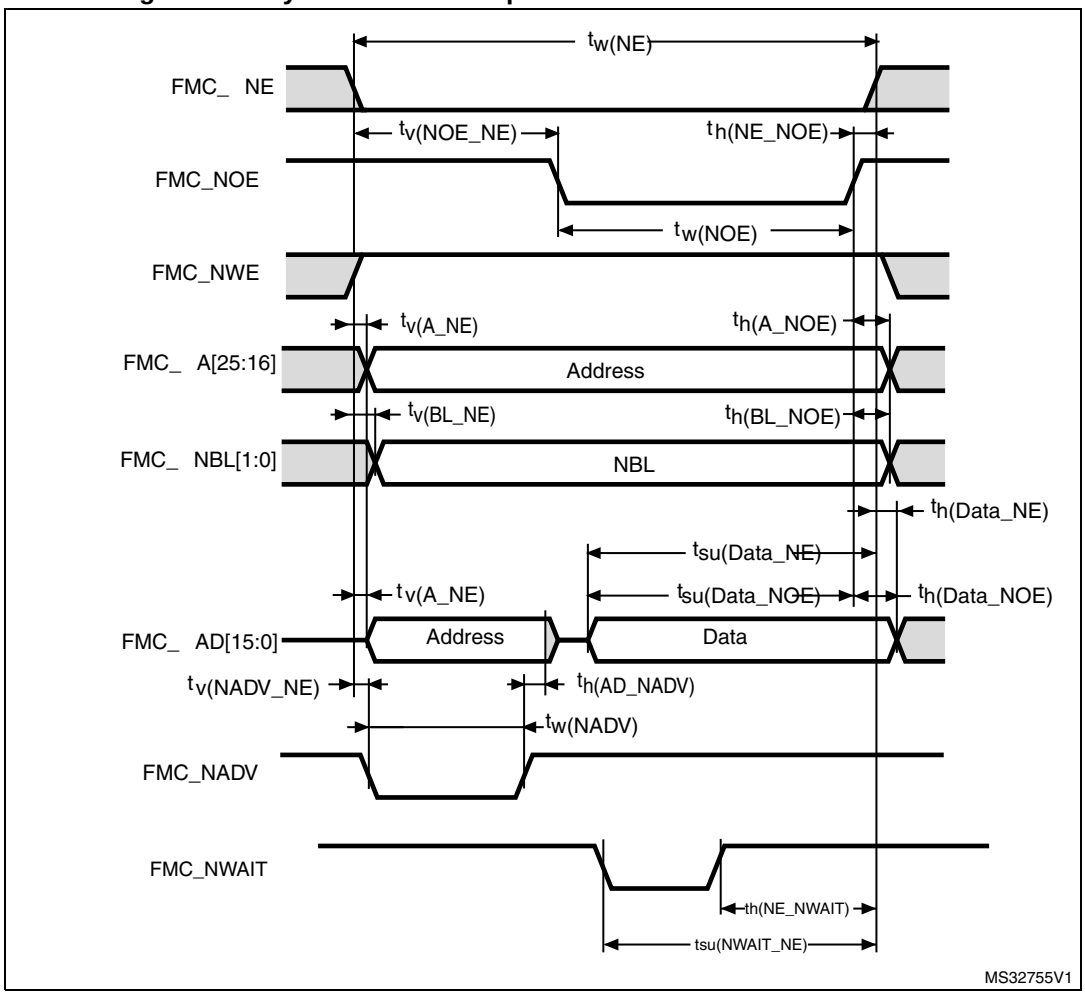


Table 95. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$	$7T_{HCLK}+2$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}-1$	-	

1. Based on test during characterization.

Synchronous waveforms and timings

Figures *63* through *66* represent synchronous waveforms and *Table 96* through *Table 99* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- C_L = 30 pF on data and address lines. C_L = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period:

- For 2.7 V≤ V_{DD}≤ 3.6 V, maximum FMC_CLK = 90 MHz at C_L = 30 pF (on FMC_CLK).
- For 1.71 V≤ V_{DD}<1.9 V, maximum FMC_CLK = 60 MHz at C_L = 10 pF (on FMC_CLK).

Table 103. LPSDR SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2.5	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	1	-	
$t_{d(SDCLKL\_SDNRAS}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	1	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	1	-	

1. Guaranteed based on test during characterization.

Figure 72. SDRAM write access waveforms

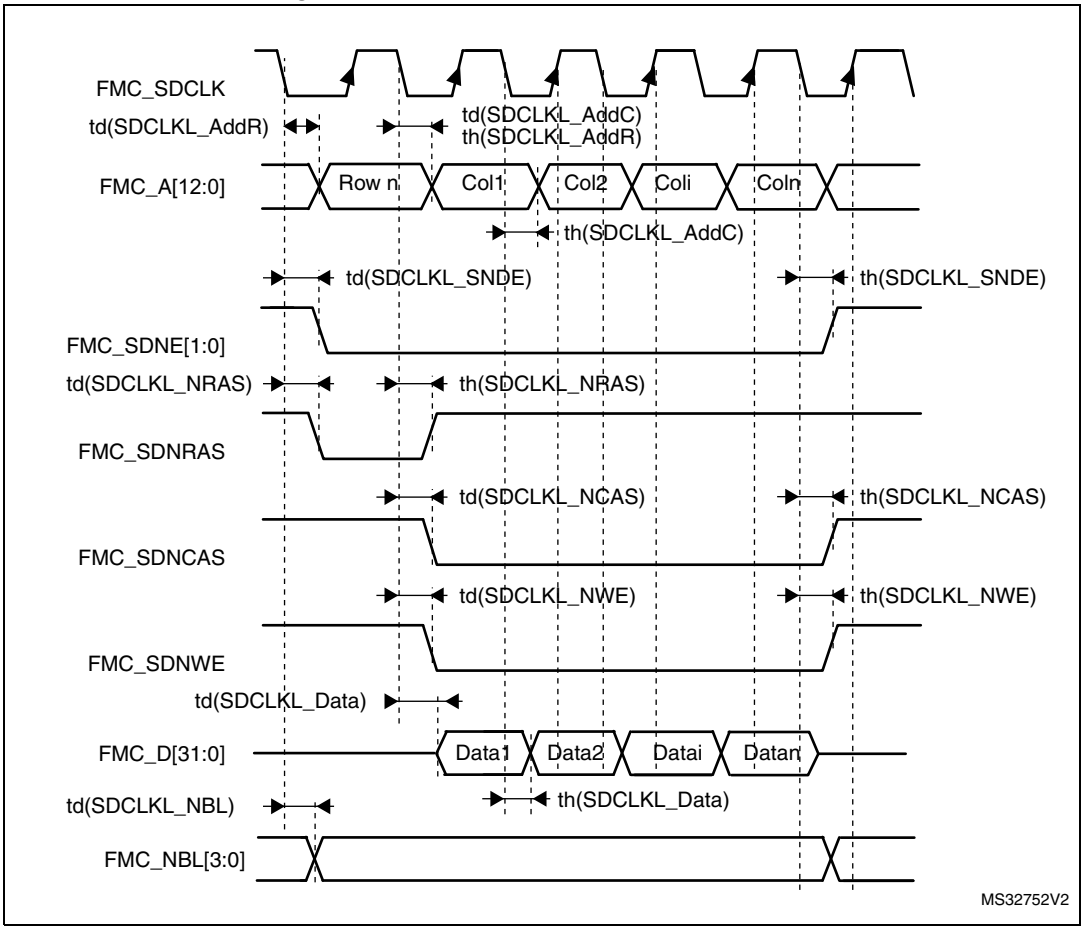


Table 116. UFBGA169 - 169-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

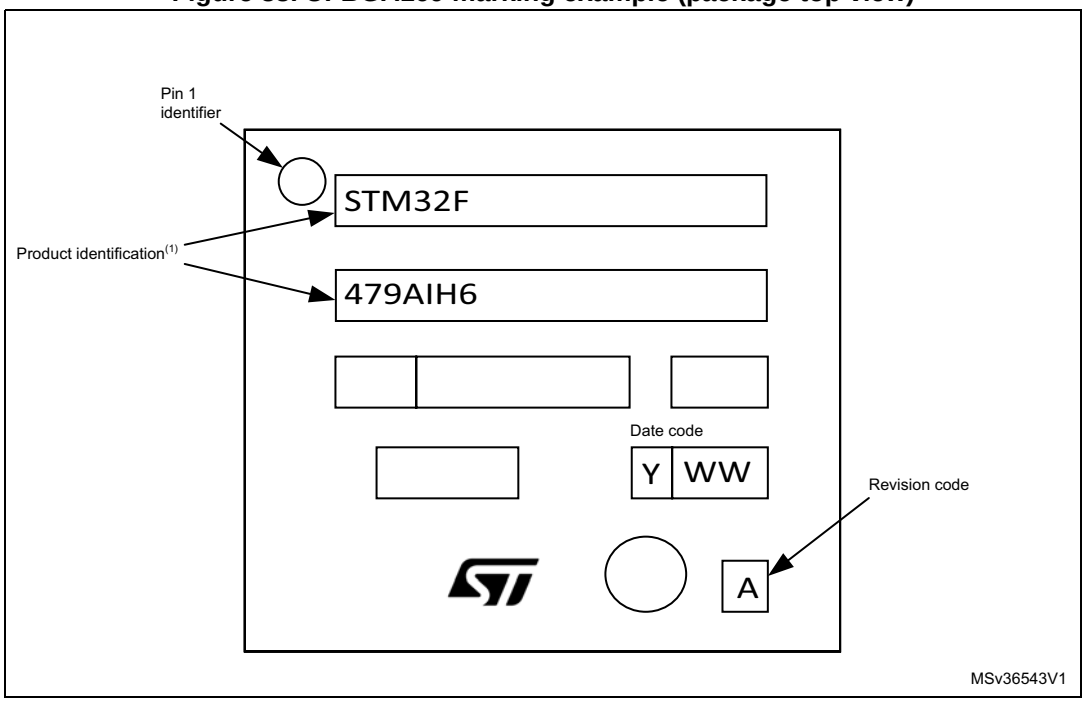
Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device Marking for UFBGA169

The following figure gives an example of topside marking orientation versus ball A1 identifier location. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 88. UFBGA169 marking example (package top view)

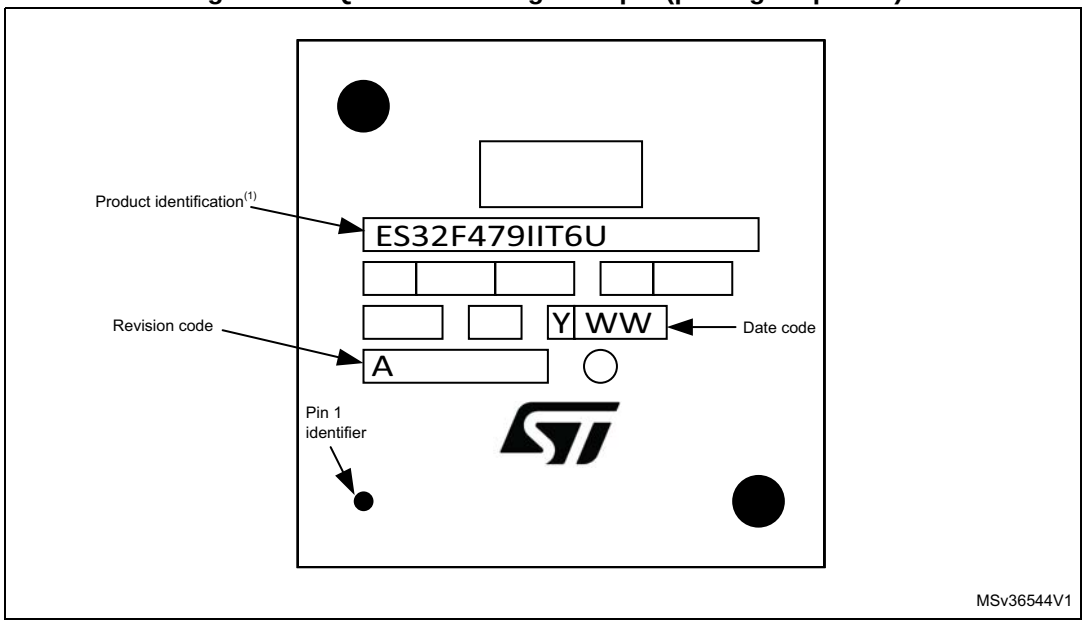


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device Marking for LQFP176

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 91. LQFP176 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.