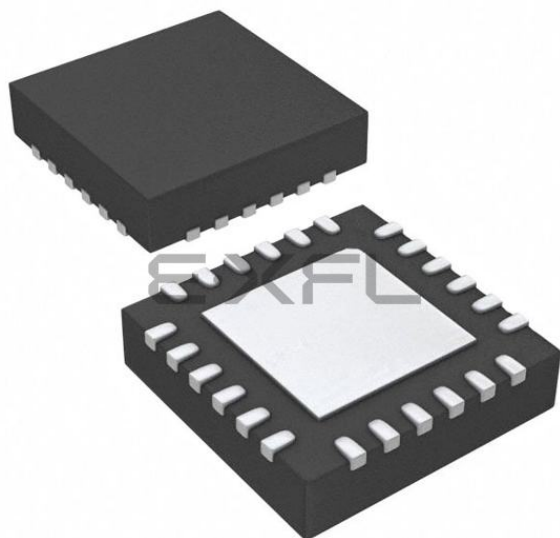




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	15
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VQFN Exposed Pad
Supplier Device Package	24-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg309f32g-a-qfn24r

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG309 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32HG309F32G-B-QFN24	32	8	25	1.98 - 3.8	-40 - 85	QFN24
EFM32HG309F64G-B-QFN24	64	8	25	1.98 - 3.8	-40 - 85	QFN24

Adding the suffix 'R' to the part number (e.g. EFM32HG309F32G-B-QFN24R) denotes tape and reel.

Visit **www.silabs.com** for information on global distributors and representatives.

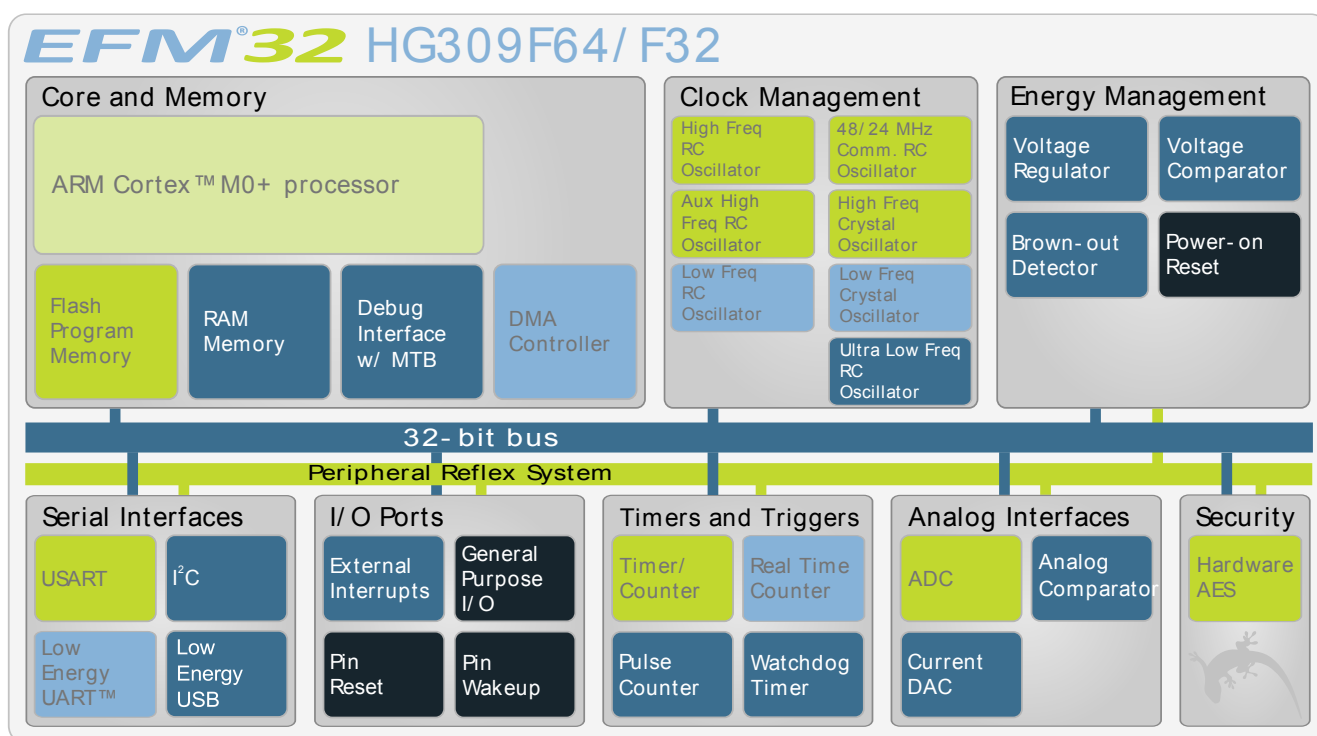
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0+, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32HG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32HG309 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32HG Reference Manual*.

A block diagram of the EFM32HG309 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and a Micro Trace Buffer (MTB) for data/instruction tracing.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32HG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits.

3.4 Current Consumption

Table 3.3. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash.	24 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		148	158	$\mu\text{A}/\text{MHz}$
		24 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		153	163	$\mu\text{A}/\text{MHz}$
		24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		161	172	$\mu\text{A}/\text{MHz}$
		24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		163	174	$\mu\text{A}/\text{MHz}$
		24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		127	137	$\mu\text{A}/\text{MHz}$
		24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		129	139	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		131	140	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		134	143	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		134	143	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		137	145	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		136	144	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		139	148	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		142	150	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		146	154	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		184	196	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		194	208	$\mu\text{A}/\text{MHz}$

Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz

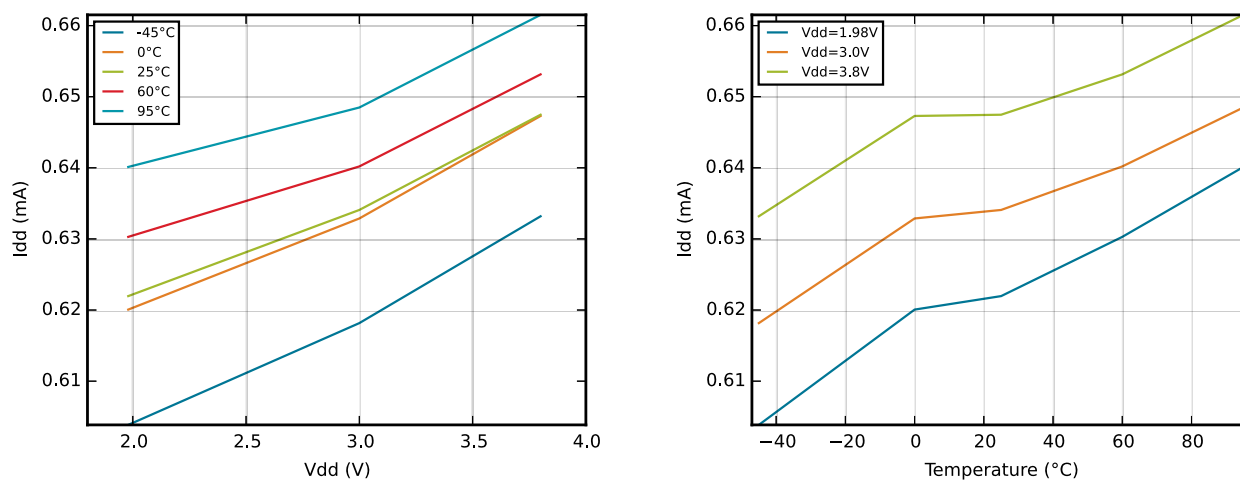
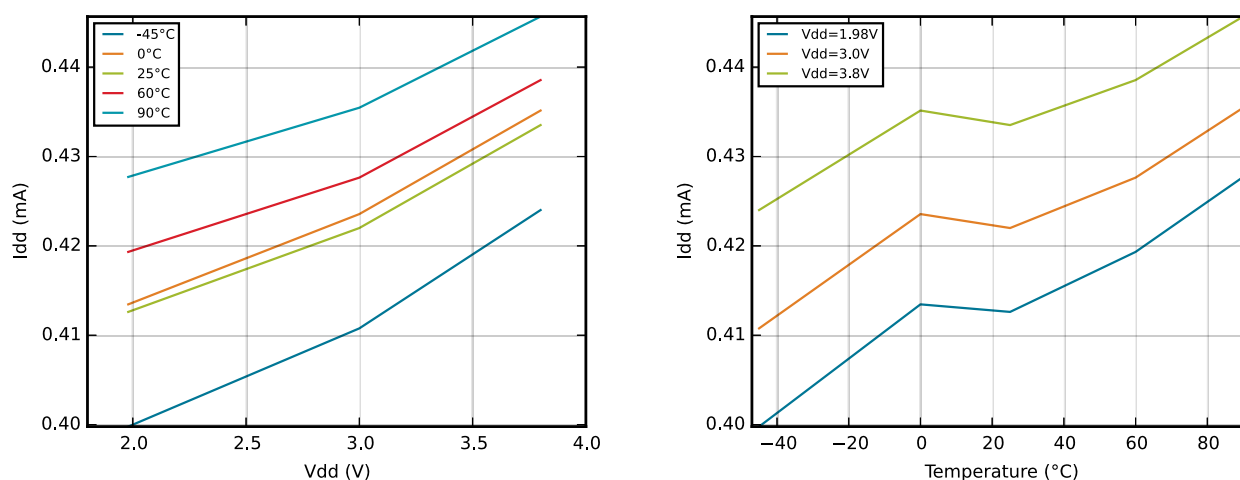
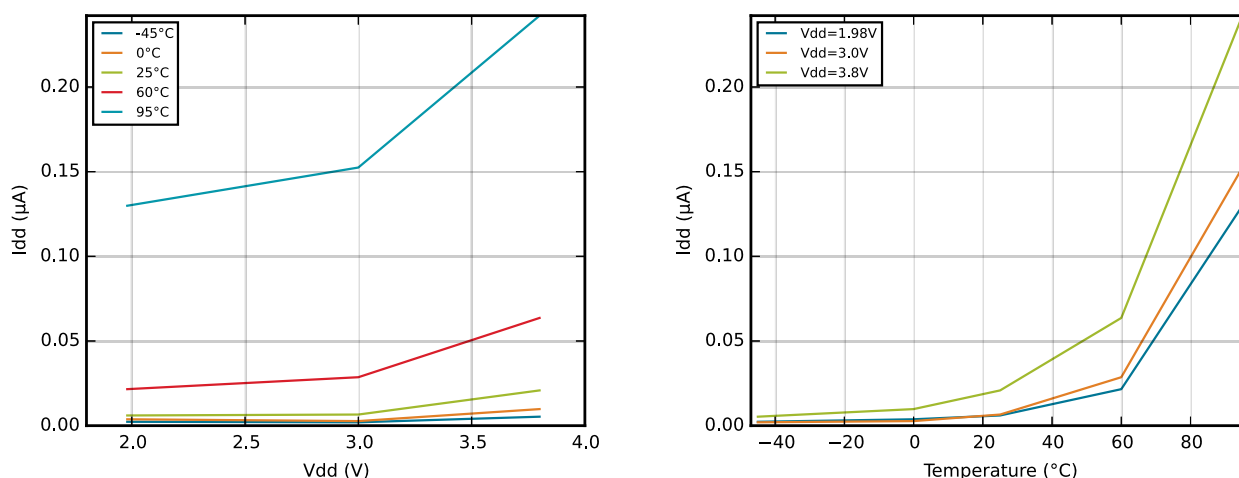


Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6 MHz



3.4.5 EM4 Current Consumption

Figure 3.13. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		µs
t_{EM30}	Transition time from EM3 to EM0		2		µs
t_{EM40}	Transition time from EM4 to EM0		163		µs

3.6 Power Management

The EFM32HG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{BODextthr-}	BOD threshold on falling external supply voltage	EM0	1.74		1.96	V
		EM2	1.71	1.86	1.98	V
V _{BODextthr+}	BOD threshold on rising external supply voltage			1.85		V
t _{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C _{DECOUPLE}	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF
C _{USB_VREGO}	USB voltage regulator out decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND		1		μF
C _{USB_VREGI}	USB voltage regulator in decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND		4.7		μF

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
RET _{FLASH}	Flash data retention	T _{AMB} <150°C	10000			h
		T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) programming time		20			μs
t _{P_ERASE}	Page erase time		20	20.4	20.8	ms
t _{D_ERASE}	Device erase time		40	40.8	41.6	ms
I _{ERASE}	Erase current				7 ¹	mA
I _{WRITE}	Write current				7 ¹	mA
V _{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

¹ Measured at 25°C

3.8 General Purpose Input Output

Table 3.7. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IOOH}	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V _{DD}		V
		Sourcing 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V _{DD}		V
		Sourcing 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V _{DD}		V
		Sourcing 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V _{DD}		V
		Sourcing 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V _{DD}			V
		Sourcing 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V _{DD}			V
		Sourcing 20 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60V _{DD}			V
		Sourcing 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80V _{DD}			V
V _{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.20V _{DD}		V
		Sinking 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.10V _{DD}		V
		Sinking 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.10V _{DD}		V
		Sinking 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.05V _{DD}		V
		Sinking 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.30V _{DD}	V
		Sinking 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.20V _{DD}	V
		Sinking 20 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.35V _{DD}	V
		Sinking 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.25V _{DD}	V
I _{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or Vdd		±0.1	±40	nA
R _{PU}	I/O pin pull-up resistor			40		kOhm

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
SFDR _{ADC}	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc

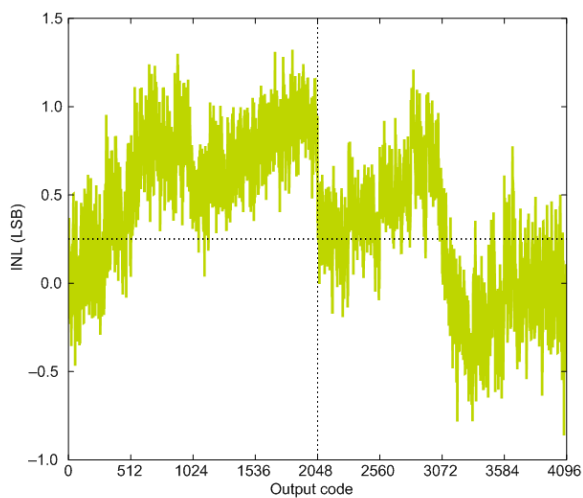
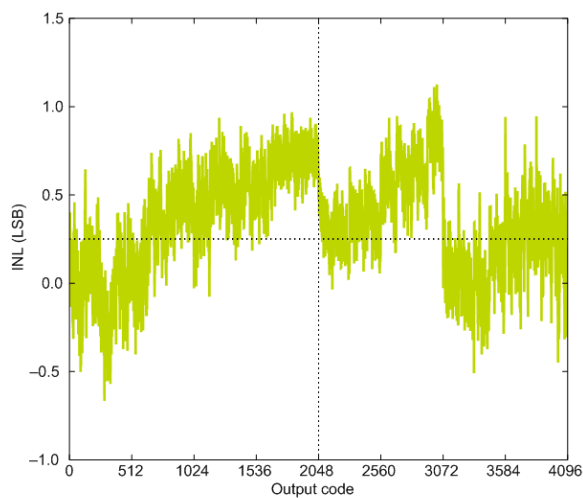
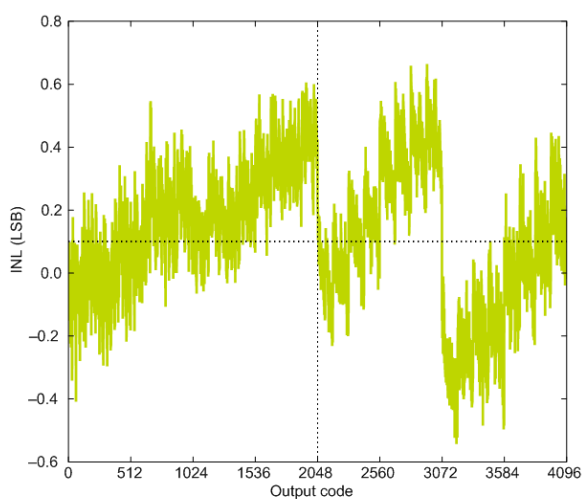
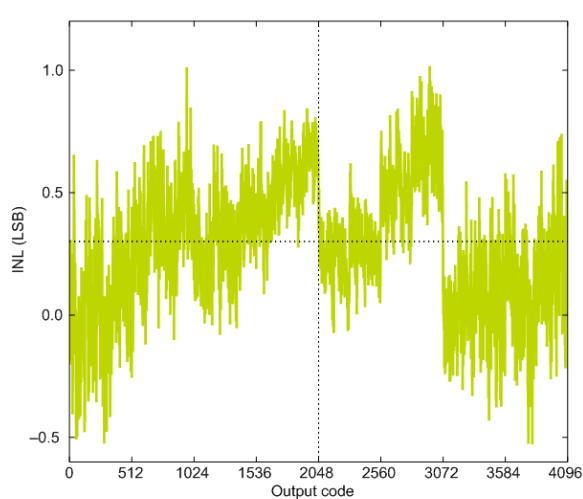
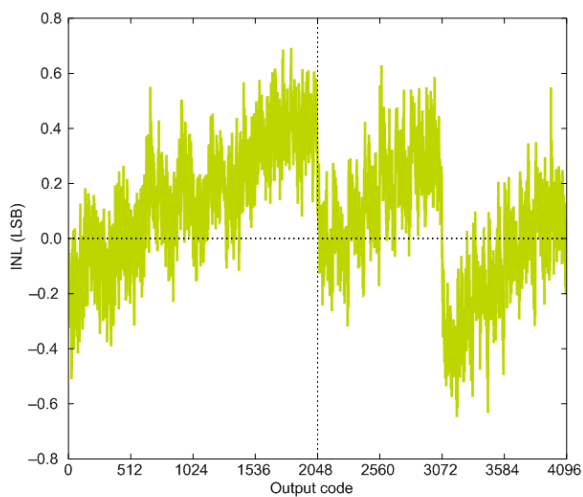
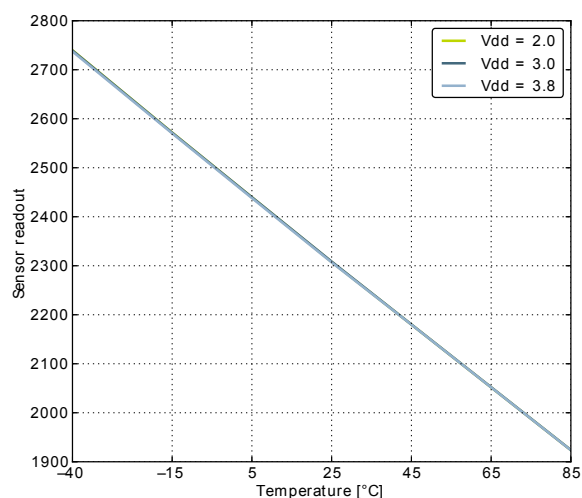
Figure 3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Figure 3.33. ADC Temperature sensor readout

3.11 Current Digital Analog Converter (IDAC)

Table 3.16. IDAC Range 0 Source

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		13.0		μA
		Duty-cycled		10		nA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			0.85		μA
I_{STEP}	Step size			0.05		μA
I_D	Current drop at high impedance load	$V_{IDAC_OUT} = V_{DD} - 100mV$		0.79		%
TC_{IDAC}	Temperature coefficient	$V_{DD} = 3.0V$, STEPSEL=0x10		0.3		nA/°C
VC_{IDAC}	Voltage coefficient	$T = 25\text{ }^{\circ}C$, STEPSEL=0x10		11.7		nA/V

Table 3.17. IDAC Range 0 Sink

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		15.1		μA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			0.85		μA
I_{STEP}	Step size			0.05		μA
I_D	Current drop at high impedance load	$V_{IDAC_OUT} = 200\text{ mV}$		0.30		%
TC_{IDAC}	Temperature coefficient	$V_{DD} = 3.0\text{ V}$, STEPSEL=0x10		0.2		nA/°C
VC_{IDAC}	Voltage coefficient	$T = 25\text{ }^{\circ}C$, STEPSEL=0x10		12.5		nA/V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			8.5		μA
I_{STEP}	Step size			0.5		μA
I_{D}	Current drop at high impedance load	$V_{\text{IDAC_OUT}} = 200 \text{ mV}$		0.62		%
TC_{IDAC}	Temperature coefficient	$V_{\text{DD}} = 3.0 \text{ V}$, STEPSEL=0x10		2.8		$\text{nA}/^\circ\text{C}$
VC_{IDAC}	Voltage coefficient	$T = 25^\circ\text{C}$, STEPSEL=0x10		94.4		nA/V

Table 3.22. IDAC Range 3 Source

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		18.7		μA
		Duty-cycled		10		nA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			33.9		μA
I_{STEP}	Step size			2.0		μA
I_{D}	Current drop at high impedance load	$V_{\text{IDAC_OUT}} = V_{\text{DD}} - 100 \text{ mV}$		3.54		%
TC_{IDAC}	Temperature coefficient	$V_{\text{DD}} = 3.0 \text{ V}$, STEPSEL=0x10		10.9		$\text{nA}/^\circ\text{C}$
VC_{IDAC}	Voltage coefficient	$T = 25^\circ\text{C}$, STEPSEL=0x10		159.5		nA/V

Table 3.23. IDAC Range 3 Sink

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		62.5		μA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			34.1		μA
I_{STEP}	Step size			2.0		μA
I_{D}	Current drop at high impedance load	$V_{\text{IDAC_OUT}} = 200 \text{ mV}$		1.75		%
TC_{IDAC}	Temperature coefficient	$V_{\text{DD}} = 3.0 \text{ V}$, STEPSEL=0x10		10.9		$\text{nA}/^\circ\text{C}$
VC_{IDAC}	Voltage coefficient	$T = 25^\circ\text{C}$, STEPSEL=0x10		148.6		nA/V

Table 3.24. IDAC

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{IDACSTART}}$	Start-up time, from enabled to output settled		40		μs

Figure 3.35. IDAC Sink Current as a function of voltage from IDAC_OUT

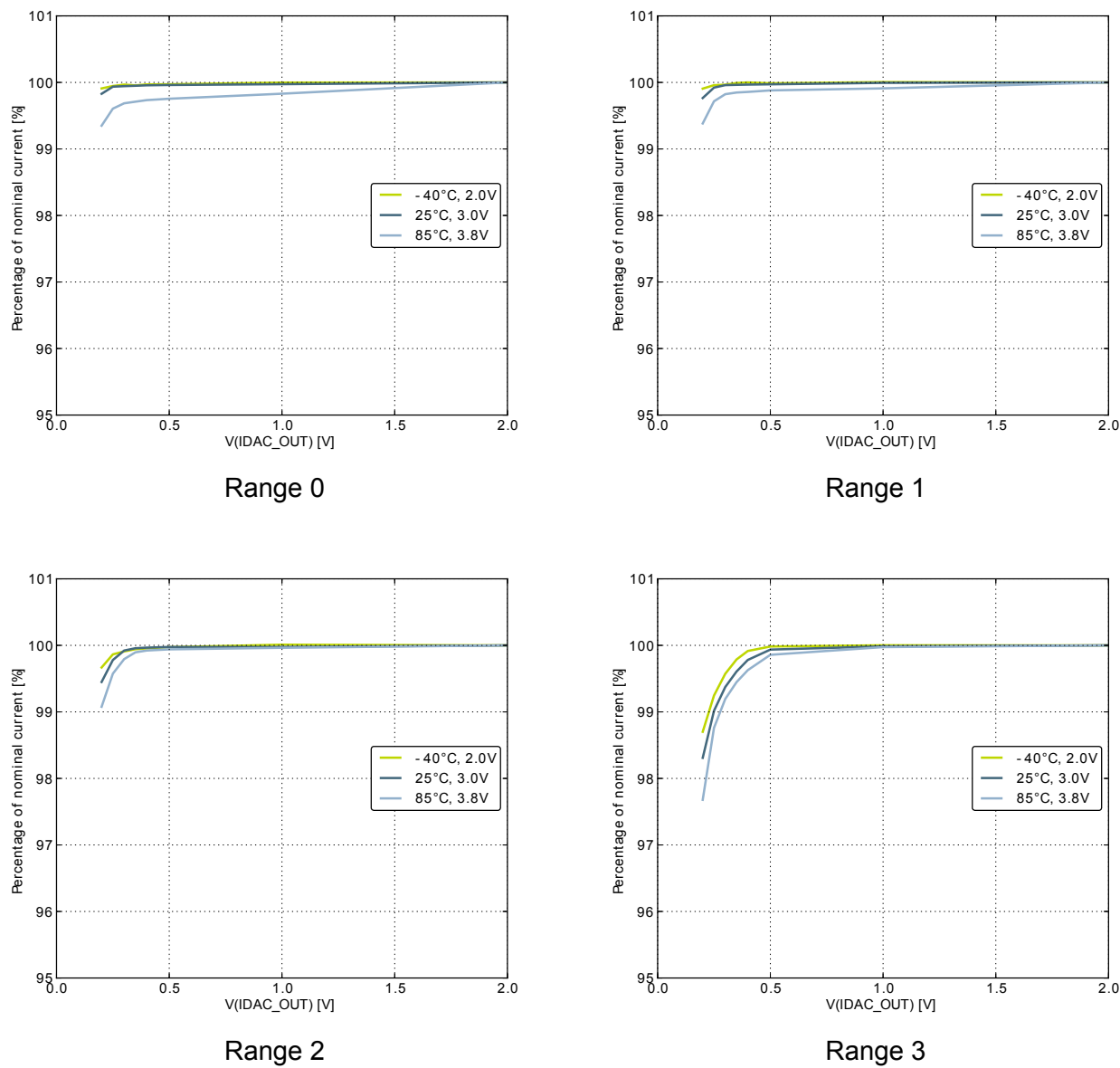
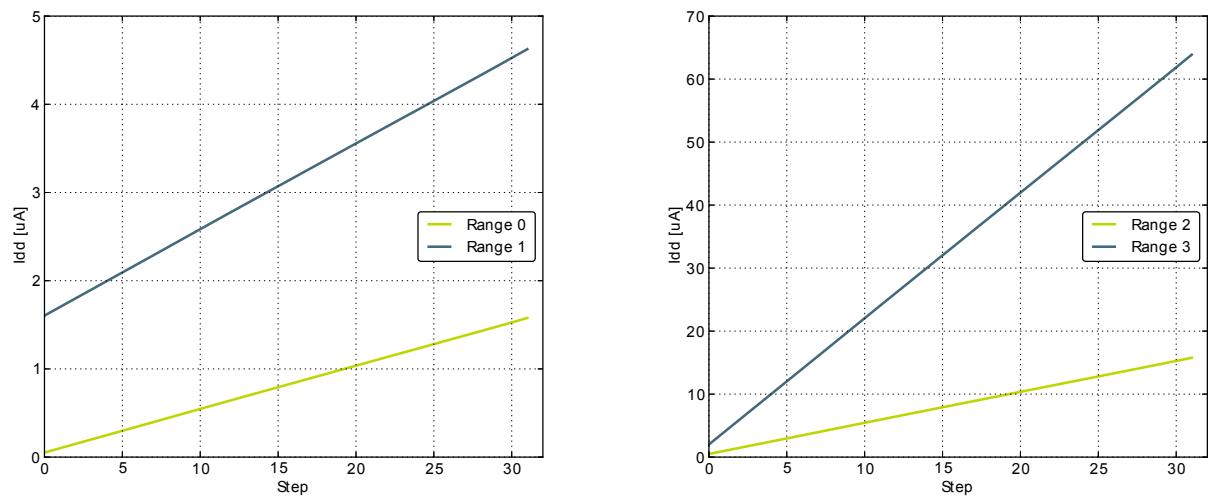


Figure 3.36. IDAC linearity



4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 54). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13			PB11				Analog comparator ACMP0, digital output.
ADC0_CH0	PE12							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PE13							Analog to digital converter ADC0, input channel number 1.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0				PF2				Clock Management Unit, clock output number 0.
CMU_CLK1			PE12	PB11				Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0							Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1							Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL					PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0				PC0	PF0	PE12	I2C0 Serial Data input / output.
IDAC0_OUT	PB11							IDAC0 output.
LEU0_RX		PB14		PF1	PA0	PC15		LEUART0 Receive input.
LEU0_TX		PB13		PF0	PF2	PC14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN			PC0		PA0			Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1		PB11			Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0		PC14	PF2				Peripheral Reflex System PRS, channel 0.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
PRS_CH1			PC15	PE12				Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0			PE13				Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1			PA0				Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1					PC0	PF1	PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2					PC1	PF2	PF2	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI1		PC14					PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15					PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0				PB7				Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14			PB8				Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0				PF2				Timer 2 Capture Compare input / output channel 0.
TIM2_CC1				PE12				Timer 2 Capture Compare input / output channel 1.
TIM2_CC2				PE13				Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12			PC15	PB13	PB13	PE12	USART0 clock input / output.
US0_CS	PE13			PC14	PB14	PB14	PE13	USART0 chip select input / output.
US0_RX				PE12	PB8	PC1	PC1	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX				PE13	PB7	PC0	PC0	USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7		PF0	PC15	PB11			USART1 clock input / output.
US1_CS	PB8		PF1	PC14	PC14	PC0		USART1 chip select input / output.
US1_RX	PC1				PA0			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0				PF2	PC1		USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PC14							USB D- pin.
USB_DMPU	PA0							USB D- Pullup control.
USB_DP	PC15							USB D+ pin.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32HG309* is shown in Table 4.3 (p. 56) . Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. QFN24 PCB Land Pattern

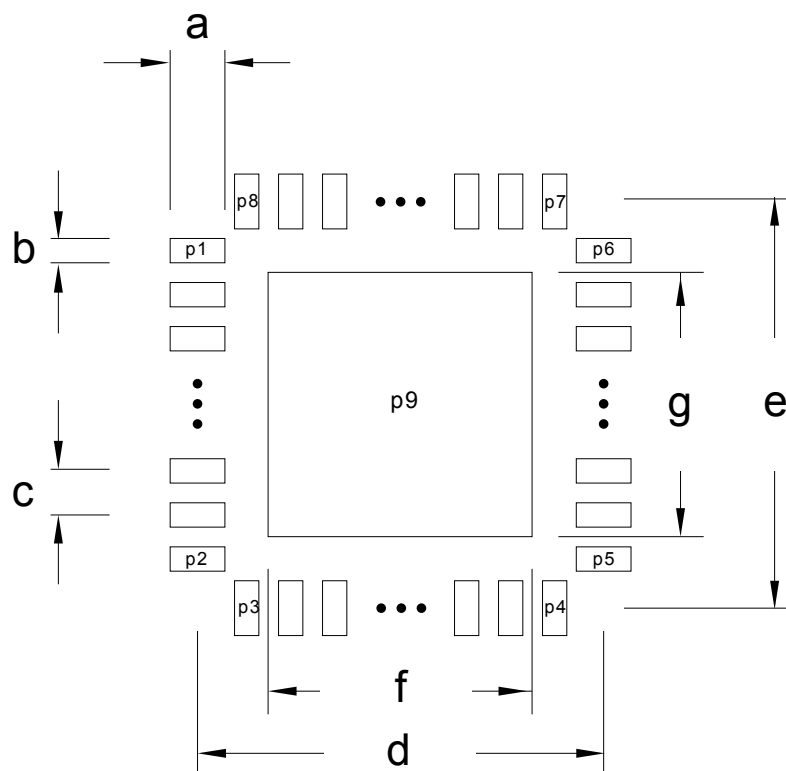


Table 5.1. QFN24 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	0.80	P1	1	P8	24
b	0.30	P2	6	P9	25
c	0.65	P3	7	-	-
d	5.00	P4	12	-	-
e	5.00	P5	13	-	-
f	3.60	P6	18	-	-
g	3.60	P7	19	-	-

B Contact Information

Silicon Laboratories Inc.

400 West Cesar Chavez

Austin, TX 78701

Please visit the Silicon Labs Technical Support web page:

<http://www.silabs.com/support/pages/contacttechnicalsupport.aspx>

and register to submit a technical support request.

Table of Contents

1. Ordering Information	2
2. System Summary	3
2.1. System Introduction	3
2.2. Configuration Summary	6
2.3. Memory Map	7
3. Electrical Characteristics	8
3.1. Test Conditions	8
3.2. Absolute Maximum Ratings	8
3.3. General Operating Conditions	8
3.4. Current Consumption	9
3.5. Transition between Energy Modes	17
3.6. Power Management	17
3.7. Flash	18
3.8. General Purpose Input Output	18
3.9. Oscillators	27
3.10. Analog Digital Converter (ADC)	32
3.11. Current Digital Analog Converter (IDAC)	42
3.12. Analog Comparator (ACMP)	47
3.13. Voltage Comparator (VCMP)	49
3.14. I2C	49
3.15. USB	50
3.16. Digital Peripherals	51
4. Pinout and Package	52
4.1. Pinout	52
4.2. Alternate Functionality Pinout	54
4.3. GPIO Pinout Overview	55
4.4. QFN24 Package	56
5. PCB Layout and Soldering	58
5.1. Recommended PCB Layout	58
5.2. Soldering Information	60
6. Chip Marking, Revision and Errata	61
6.1. Chip Marking	61
6.2. Revision	61
6.3. Errata	61
7. Revision History	62
7.1. Revision 1.00	62
7.2. Revision 0.91	62
7.3. Revision 0.90	62
7.4. Revision 0.20	63
A. Disclaimer and Trademarks	64
A.1. Disclaimer	64
A.2. Trademark Information	64
B. Contact Information	65
B.1.	65

List of Tables

1.1. Ordering Information	2
2.1. Configuration Summary	6
3.1. Absolute Maximum Ratings	8
3.2. General Operating Conditions	8
3.3. Current Consumption	9
3.4. Energy Modes Transitions	17
3.5. Power Management	18
3.6. Flash	18
3.7. GPIO	18
3.8. LFXO	27
3.9. HFXO	27
3.10. LFRCO	28
3.11. HFRCO	29
3.12. AUXHFRCO	31
3.13. USHFRCO	32
3.14. ULFRCO	32
3.15. ADC	32
3.16. IDAC Range 0 Source	42
3.17. IDAC Range 0 Sink	42
3.18. IDAC Range 1 Source	43
3.19. IDAC Range 1 Sink	43
3.20. IDAC Range 2 Source	43
3.21. IDAC Range 2 Sink	43
3.22. IDAC Range 3 Source	44
3.23. IDAC Range 3 Sink	44
3.24. IDAC	44
3.25. ACMP	47
3.26. VCMP	49
3.27. I2C Standard-mode (Sm)	49
3.28. I2C Fast-mode (Fm)	50
3.29. I2C Fast-mode Plus (Fm+)	50
3.30. USB	50
3.31. Digital Peripherals	51
4.1. Device Pinout	52
4.2. Alternate functionality overview	54
4.3. GPIO Pinout	56
4.4. QFN24 (Dimensions in mm)	57
5.1. QFN24 PCB Land Pattern Dimensions (Dimensions in mm)	58
5.2. QFN24 PCB Solder Mask Dimensions (Dimensions in mm)	59
5.3. QFN24 PCB Stencil Design Dimensions (Dimensions in mm)	60

List of Equations

3.1. Total ACMP Active Current 47

3.2. VCMP Trigger Level as a Function of Level Setting 49

silabs.com

