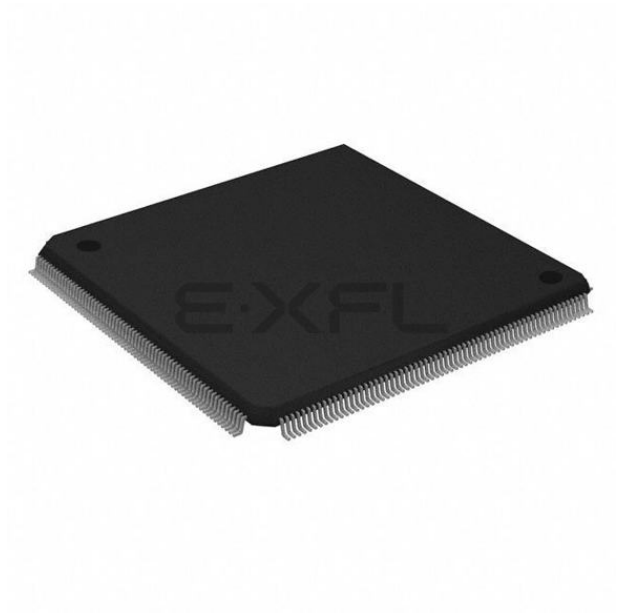
Renesas Electronics America Inc - R7S721000VCFP#AA1 Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DVD, VDC
Ethernet	10/100Mbps (1), 100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.2V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-LQFP
Supplier Device Package	256-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s721000vcfp-aa1

(2) Internal units

(a) CPU

The CPU uses five-stage pipeline control to enable single-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other instruction processing.

Other dedicated on-chip hardware, such as a multiplier (16 bits × 16 bits → 32 bits) and a barrel shifter (32 bits), help accelerate complex processing.

(b) Bus control unit (BCU)

The BCU controls the internal bus.

(c) ROM

This is flash memory that is mapped from address 00000000H.

During instruction fetch, ROM/flash memory can be accessed from the CPU in 1-clock cycles. The internal ROM capacity and area differ as follows depending on the product.

Part Number	Internal ROM Capacity	Internal ROM Area
μPD70F3713	64 KB (flash memory)	xn000000H to xn00FFFFH
μPD70F3714	128 KB (flash memory)	xn000000H to xn01FFFFH

Remark n = xx11B

(d) RAM

This is a 6 KB internal RAM that is mapped to the addresses xnFFD800H to xnFFEFFFH.

During instruction fetch or data access, data can be accessed from the CPU in 1-clock cycles.

Remark n = xx11B

(e) Interrupt controller (INTC)

This controller handles hardware interrupt requests (INTP0 to INTP6) from on-chip peripheral hardware and external hardware. Eight levels of interrupt priorities can be specified for these interrupt requests, and multiple-interrupt servicing control can be performed.

(f) Clock generator (CG)

The clock generator includes two basic operation modes: PLL mode (fixed to multiplication by eight) and clock-through mode. It generates four types of clocks (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$), and supplies one of them as the operating clock for the CPU (f_{CPU}).

(g) Timer/counter

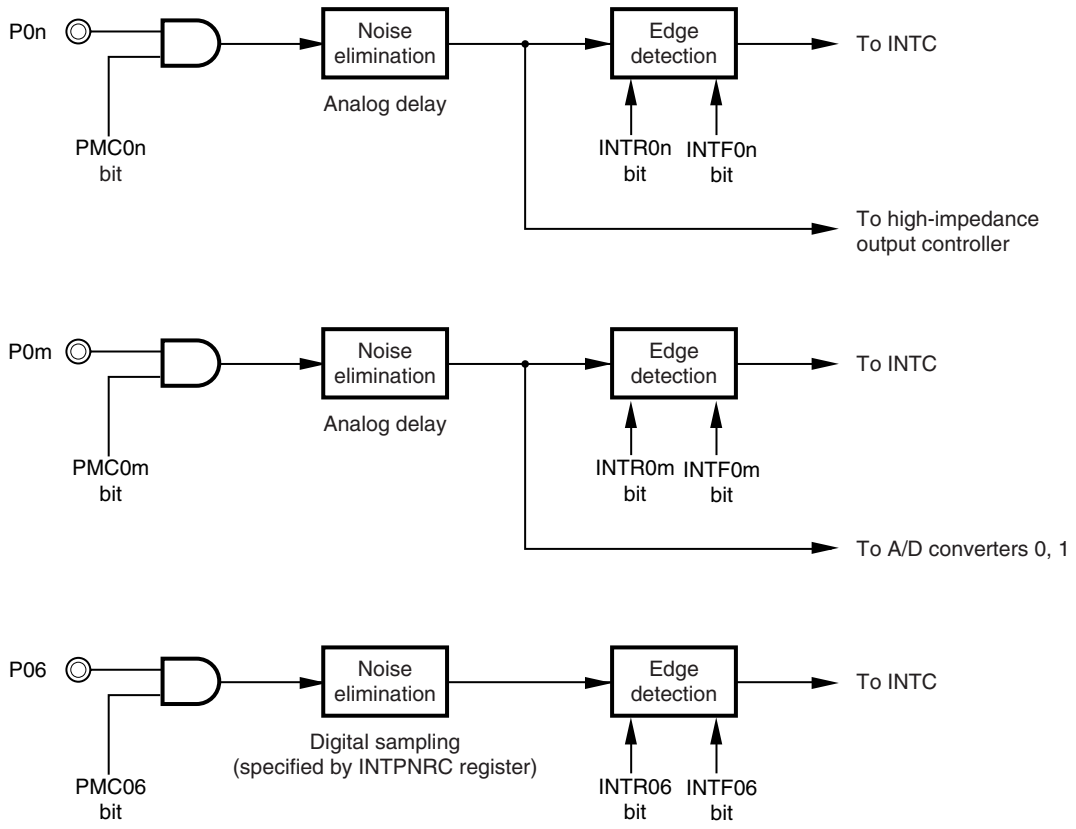
This unit incorporates one 16-bit interval timer M (TMM) channel, two 16-bit timer/event counter Q (TMQ) channels, and four 16-bit timer/event counter P (TMP) channels, and can measure pulse interval widths or frequency, enable an inverter function for motor control, and output a programmable pulse.

(h) Watchdog timer (WDT)

A watchdog timer is equipped to detect program loops, system abnormalities, etc.

It generates a non-maskable interrupt request signal (INTWDT) or internal reset signal (WDTRES) after an overflow occurs.

A noise elimination function is included as an alternate function of port 0.

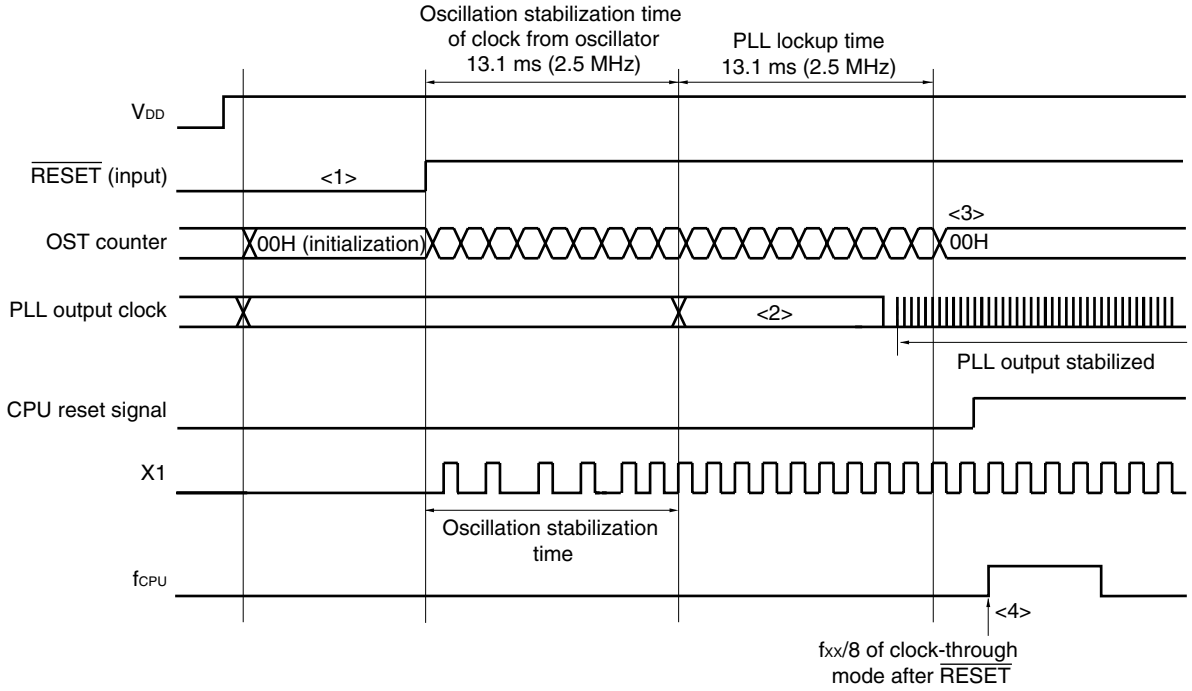


Caution To control high-impedance output of the external interrupt function and motor output control function, set the PMC0a bit to 1 (a = 0 to 6).

Remark n = 0 to 3
m = 4, 5

5.5.2 Operation timing

(1) Power on (power-on reset)



<1> The oscillator is activated by $\overline{\text{RESET}}$ release power application.
PLL stops during the $\overline{\text{RESET}}$ period and the oscillation stabilization time set using the OSTS register.

<2> When the oscillation stabilization time that elapses after the $\overline{\text{RESET}}$ signal is released expires, PLL stop is released, and counting the lockup time starts.

<3> PLL is locked when counting of the lockup time is over. The OST counter is initialized to 00H.

<4> When the lockup time expires, the CPU releases the reset signal and operates in the clock-through mode (f_X). The CPU operation clock (f_{CPU}) is $f_{XX}/8$. The PLL mode can be set by software.

Cautions 1. After the $\overline{\text{RESET}}$ signal is released, a specific wait time (oscillation stabilization time) elapses.

2. To avoid malfunction due to noise, do not change the division ratio of the CPU operation clock (f_{CPU}) by using the PCC register before setting the PLL mode. Before changing the division ratio, be sure to select the PLL mode.

(7) TMPn capture/compare register 0 (TPnCCR0)

The TP0CCR0 and TP2CCR0 registers are 16-bit registers that can be used as capture registers or compare registers depending on the mode. The TP1CCR0 and TP3CCR0 registers are 16-bit registers that can only be used as compare registers.

The TP0CCR0 and TP2CCR0 registers can be used as a capture register or a compare register only in the free-running timer mode, depending on the setting of the TP0OPT0.TP0CCS0 or TP2OPT0.TP2CCS0 bit. In the pulse width measurement mode, the TPnCCR0 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TPnCCR0 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

After reset: 0000H R/W Address: TP0CCR0 FFFFF646H, TP1CCR0 FFFFF666H, TP2CCR0 FFFFF686H, TP3CCR0 FFFFF6A6H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPnCCR0																

(n = 0 to 3)

(8) TMPn capture/compare register 1 (TPnCCR1)

The TP0CCR1 and TP2CCR1 registers are 16-bit registers that can be used as capture registers or compare registers depending on the mode. The TP1CCR1 and TP3CCR1 registers are 16-bit registers that can only be used as compare registers.

The TP0CCR1 and TP2CCR1 registers can be used as a capture register or a compare register only in the free-running timer mode, depending on the setting of the TP0OPT0.TP0CCS1 or TP2OPT0.TP2CCS1 bit. In the pulse width measurement mode, the TPnCCR1 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TPnCCR1 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

After reset: 0000H R/W Address: TP0CCR1 FFFFF648H, TP1CCR1 FFFFF668H, TP2CCR1 FFFFF688H, TP3CCR1 FFFFF6A8H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPnCCR1																

(n = 0 to 3)

When the TPnCE bit is set to 1, the value of the 16-bit counter is cleared from FFFFH to 0000H in synchronization with the count clock, and the counter starts counting. At this time, the output of the TOP00 pin is inverted. Additionally, the set value of the TPnCCR0 register is transferred to the CCR0 buffer register.

When the count value of the 16-bit counter matches the value of the CCR0 buffer register, the 16-bit counter is cleared to 0000H, the output of the TOP00 pin is inverted, and a compare match interrupt request signal (INTTPnCC0) is generated.

The interval can be calculated by the following expression.

Interval = (Set value of TPnCCR0 register + 1) × Count clock cycle

Remark n = 0 to 3

Figure 6-11. Register Setting for Interval Timer Mode Operation (1/3)

(a) TMPn control register 0 (TPnCTL0)

	TPnCE					TPnCKS2	TPnCKS1	TPnCKS0
TPnCTL0	0/1	0	0	0	0	0/1	0/1	0/1

Select count clock

0: Stop counting
1: Enable counting

(b) TMPn control register 1 (TPnCTL1)

	TP1SYE	TPmEST	TPkEEE			TPnMD2	TPnMD1	TPnMD0
<R> TPnCTL1	0	0	0/1[Note]	0	0	0	0	0

0, 0, 0:
Interval timer mode

0: Operate at count clock selected in TPkCKS0 to TPkCKS2 bits
1: Count operation by external event count input signal

<R> **Note** Enable setting of the TPkEEE bit to 1 only when timer output (TOPk1) is used. In this case, set the TPkCCR0 and TPkCCR1 registers to the same value.

Figure 6-11. Register Setting for Interval Timer Mode Operation (3/3)

(g) TMPn capture/compare register 1 (TPnCCR1)

The TPnCCR1 register is not used in the interval timer mode. However, the set value of the TPnCCR1 register is transferred to the CCR1 buffer register. When the count value of the 16-bit counter matches the value of the CCR1 buffer register, the TOPm1 pin output is inverted and a compare match interrupt request signal (INTTPnCC1) is generated.

By setting this register to the same value as the value set in the TPmCCR0 register, a PWM waveform with a duty factor of 50% can be output from the TOPm1 pin.

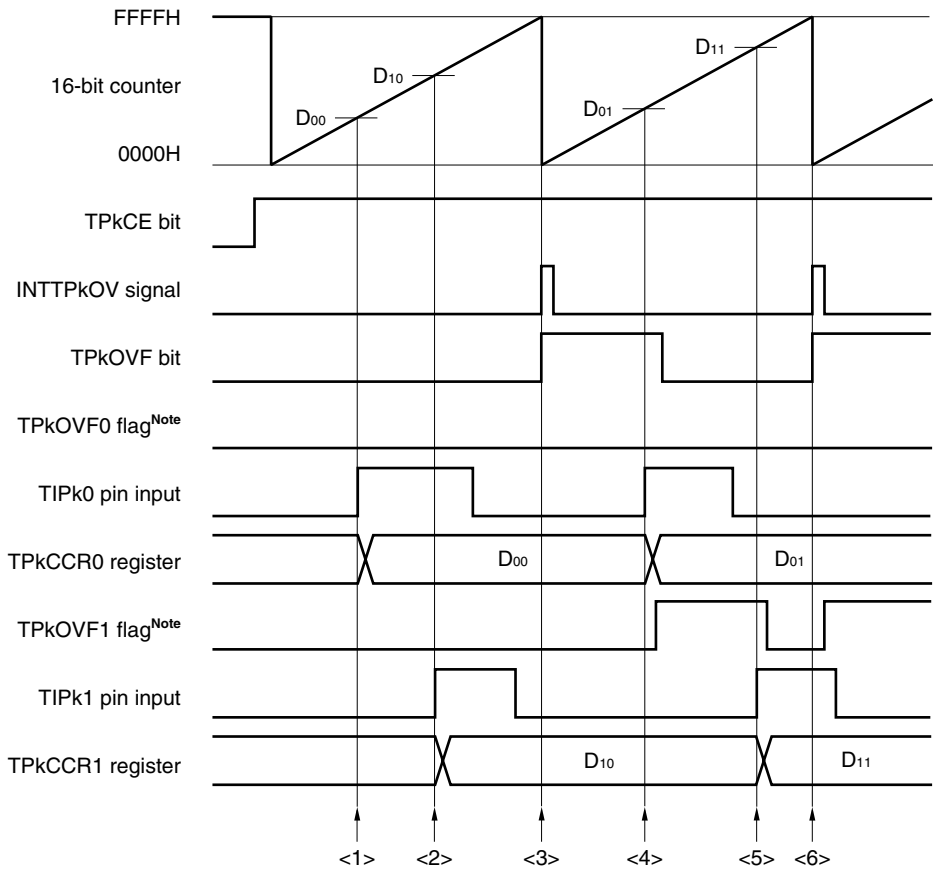
When the TPnCCR1 register is not used, it is recommended to set its value to FFFFH. Also mask the register by the interrupt mask flag (TPnCCIC1.TPnCCMK1).

<R> **Remarks 1.** TMPk I/O control register 1 (TPkIOC1) and TMPn option register 0 (TPnOPT0) are not used in the interval timer mode.

2. n = 0 to 3,
m = 0, 2, 3
k = 0, 2

(2/2)

Example when two capture registers are used (without using overflow interrupt)



Note The TPkOVF0 and TPkOVF1 flags are set on the internal RAM by software.

<1> Read the TPkCCR0 register (setting of the default value of the TIPk0 pin input).
<2> Read the TPkCCR1 register (setting of the default value of the TIPk1 pin input).
<3> An overflow occurs. Nothing is done by software.
<4> Read the TPkCCR0 register.
Read the overflow flag. If the overflow flag is 1, set only the TPkOVF1 flag to 1, and clear the overflow flag to 0.
Because the overflow flag is 1, the pulse width can be calculated by (10000H + D_{01} − D_{00}).
<5> Read the TPkCCR1 register.
Read the overflow flag. Because the overflow flag is cleared in <4>, 0 is read.
Read the TPkOVF1 flag. If the TPkOVF1 flag is 1, clear it to 0.
Because the TPkOVF1 flag is 1, the pulse width can be calculated by (10000H + D_{11} − D_{10}) (correct).
<6> Same as <3>

Remark k = 0, 2

(e) Interrupt operation

TMQn generates the following five interrupt request signals.

- INTTQnCC0 interrupt: This signal functions as a match interrupt request signal of the CCR0 buffer register and as a capture interrupt request signal to the TQnCCR0 register.
- INTTQnCC1 interrupt: This signal functions as a match interrupt request signal of the CCR1 buffer register and as a capture interrupt request signal to the TQnCCR1 register.
- INTTQnCC2 interrupt: This signal functions as a match interrupt request signal of the CCR2 buffer register and as a capture interrupt request signal to the TQnCCR2 register.
- INTTQnCC3 interrupt: This signal functions as a match interrupt request signal of the CCR3 buffer register and as a capture interrupt request signal to the TQnCCR3 register.
- INTTQnOV interrupt: This signal functions as an overflow interrupt request signal.

When the TQ0CE bit is set to 1, 16-bit timer/event counter Q waits for a trigger. When the trigger is generated, the 16-bit counter is cleared from FFFFH to 0000H, starts counting, and outputs a one-shot pulse from the TOQ0b pin. After the one-shot pulse is output, the 16-bit counter is cleared to 0000H, stops counting, and waits for a trigger. When the trigger is generated again, the 16-bit counter starts counting from 0000H. If a trigger is generated again while the one-shot pulse is being output, it is ignored.

The output delay period and active level width of the one-shot pulse can be calculated as follows.

Output delay period = (Set value of TQ0CCRb register) × Count clock cycle

Active level width = (Set value of TQ0CCR0 register − Set value of TQ0CCRb register + 1) × Count clock cycle

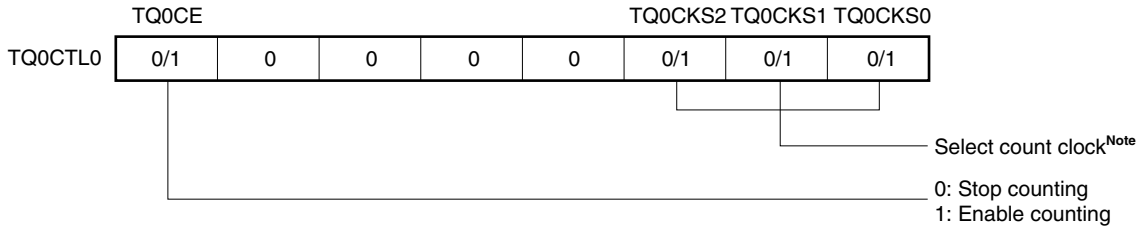
The compare match interrupt request signal INTTQ0CC0 is generated when the 16-bit counter counts after its count value matches the value of the CCR0 buffer register. The compare match interrupt request signal INTTQ0CCb is generated when the count value of the 16-bit counter matches the value of the CCRb buffer register.

Only setting the software trigger (TQ0CTL1.TQ0EST bit) to 1 is used as the trigger.

Remark b = 1 to 3

Figure 7-28. Register Setting in One-Shot Pulse Output Mode (1/3)

(a) TMQ0 control register 0 (TQ0CTL0)



Note The setting is invalid when the TQ0CTL1.TQ0EEE bit = 1.

(b) TMQ0 control register 1 (TQ0CTL1)

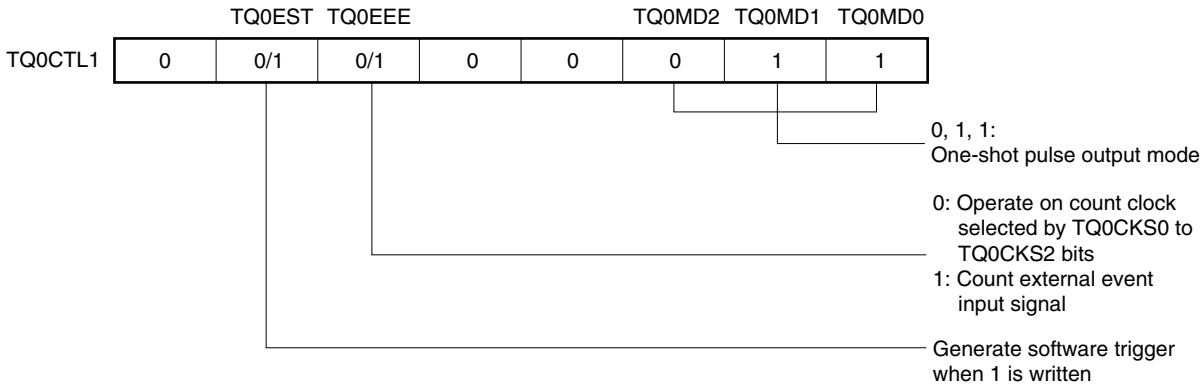


Figure 7-28. Register Setting in One-Shot Pulse Output Mode (3/3)

(f) TMQ0 capture/compare registers 0 to 3 (TQ0CCR0 to TQ0CCR3)

If D_0 is set to the TQ0CCR0 register and D_b to the TQ0CCRb register, the active level width and output delay period of the one-shot pulse are as follows.

<R> Active level width = $(D_0 - D_b + 1) \times$ Count clock cycle

Output delay period = $D_b \times$ Count clock cycle

<R> **Caution One-shot pulses are not output even in the one-shot pulse output mode, if the value set in the TQ0CCRb register is greater than that set in the TQ0CCR0 register.**

Remarks 1. TMQ0 I/O control register 1 (TQ0IOC1) and TMQ0 option register 0 (TQ0OPT0) are not used in the one-shot pulse output mode.

2. b = 1 to 3

(2/2)

TQ1ATM03	TQ1ATM03 mode selection
0	Output A/D trigger signal (TQTADT10) for INTTP1CC1 interrupt while dead-time counter is counting up.
1	Output A/D trigger signal (TQTADT10) for INTTP1CC1 interrupt while dead-time counter is counting down.

TQ1ATM02	TQ1ATM02 mode selection
0	Output A/D trigger signal (TQTADT10) for INTTP1CC0 interrupt while dead-time counter is counting up.
1	Output A/D trigger signal (TQTADT10) for INTTP1CC0 interrupt while dead-time counter is counting down.

TQ1AT03Note	A/D trigger output control 3
0	Disable output of A/D trigger signal (TQTADT10) for INTTP1CC1 interrupt.
1	Enable output of A/D trigger signal (TQTADT10) for INTTP1CC1 interrupt.

TQ1AT02Note	A/D trigger output control 2
0	Disable output of A/D trigger signal (TQTADT10) for INTTP1CC0 interrupt.
1	Enable output of A/D trigger signal (TQTADT10) for INTTP1CC0 interrupt.

TQ1AT01Note	A/D trigger output control 1
0	Disable output of A/D trigger signal (TQTADT10) for INTTQ1CC0 (crest interrupt).
1	Enable output of A/D trigger signal (TQTADT10) for INTTQ1CC0 (crest interrupt).

TQ1AT00Note	A/D trigger output control 0
0	Disable output of A/D trigger signal (TQTADT10) for INTTQ1OV (valley interrupt).
1	Enable output of A/D trigger signal (TQTADT10) for INTTQ1OV (valley interrupt).

Note For the setting of the TQ1AT03 to TQ1AT00 bits, see **CHAPTER 11 A/D CONVERTERS 0 AND 1**.

10.3 Control Registers

(1) Watchdog timer mode register (WDTM)

The WDTM register sets the overflow time and operation clock of the watchdog timer.

This register can be read or written in 8-bit units. This register can be read any number of times, but can be written only once following reset release; it cannot then be written a second or subsequent time.

Reset sets this register to 67H.

After reset: 67H R/W Address: FFFFF6D0H

	7	6	5	4	3	2	1	0
WDTM	0	WDM1	WDM0	0	0	WDCS2	WDCS1	WDCS0

WDM1	WDM0	Selection of operation mode of watchdog timer
0	0	Stop operation
0	1	Non-maskable interrupt request mode (generation of INTWDT signal)
1	×	Reset mode (generation of WDTRES signal)

Cautions 1. For details of the WDCS2 to WDCS0 bits, see Table 10-2 Overflow Time.

2. Be sure to clear bits 3, 4, and 7 to "0".

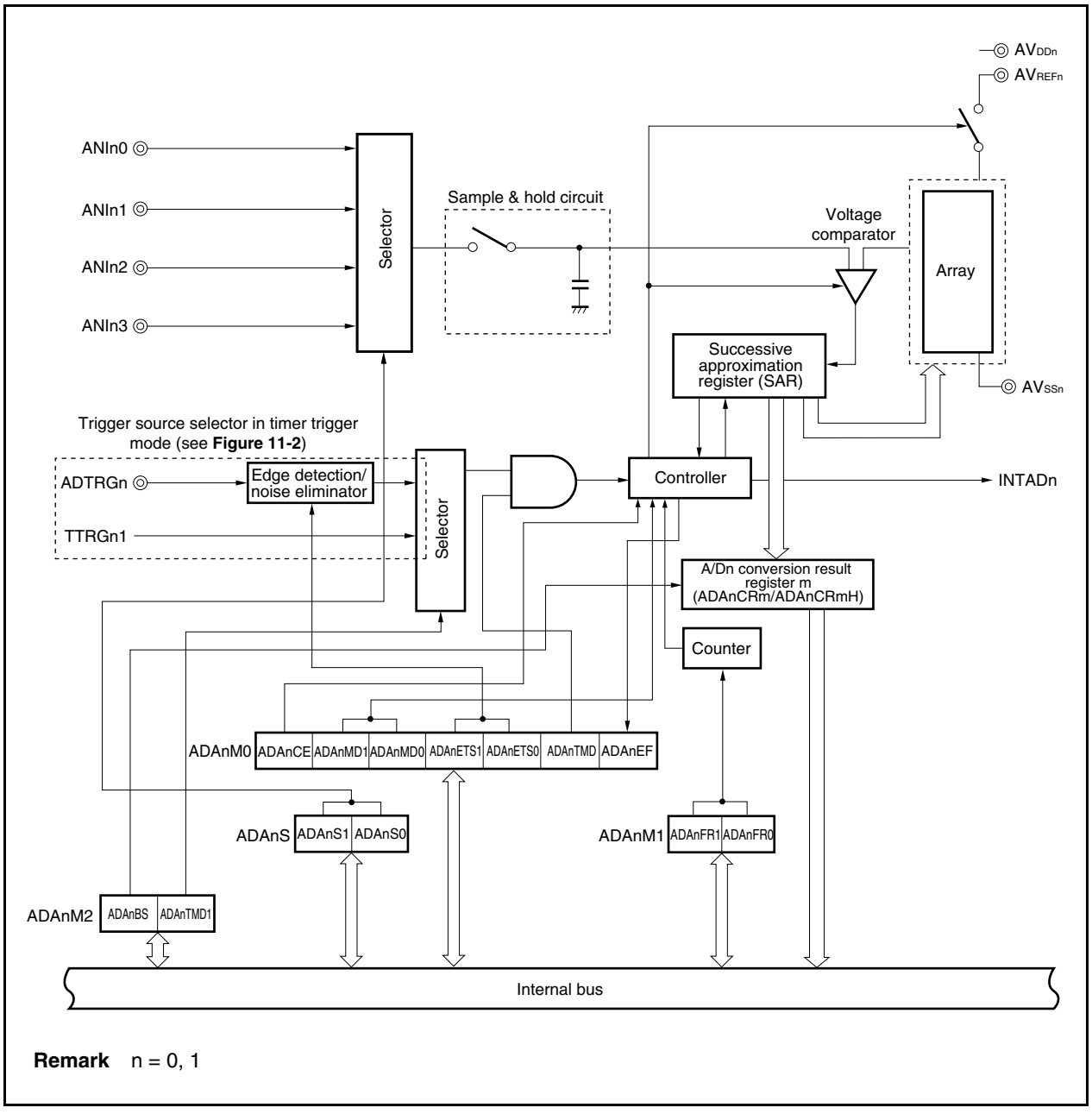
Table 10-2. Overflow Time

WDCS2	WDCS1	WDCS0	Overflow Time	f_{XX} = 20 MHz
0	0	0	$2^{18}/f_{XX}$	13.1 ms
0	0	1	$2^{19}/f_{XX}$	26.2 ms
0	1	0	$2^{20}/f_{XX}$	52.4 ms
0	1	1	$2^{21}/f_{XX}$	104.9 ms
1	0	0	$2^{22}/f_{XX}$	209.7 ms
1	0	1	$2^{23}/f_{XX}$	419.4 ms
1	1	0	$2^{24}/f_{XX}$	838.9 ms
1	1	1	$2^{25}/f_{XX}$	1677.7 ms

11.2 Configuration

The block diagram is shown below.

Figure 11-1. Block Diagram of A/D Converters 0 and 1



Remark n = 0, 1

(5) Successive approximation register (SAR)

The SAR is a 10-bit register that sets voltage tap data whose values from the array match the voltage values of the analog input pins, 1 bit at a time starting from the most significant bit (MSB).

If data is set in the SAR all the way to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR (conversion results) are held in A/Dn conversion result registers 0 to 3 (ADAnCR0 to ADAnCR3) (n = 0, 1). When all the specified A/D conversion operations have ended, an A/Dn conversion end interrupt request signal (INTADn) is generated.

(6) A/Dn conversion result registers 0 to 3 (ADAnCR0 to ADAnCR3), A/Dn conversion result registers 0H to 3H (ADAnCR0H to ADAnCR3H) (n = 0, 1)

The ADAnCR0 to ADAnCR3 and ADAnCR0H to ADAnCR3H registers are registers that hold the A/D conversion results. Each time A/D conversion ends, the conversion result is loaded from the successive approximation register (SAR) and stored in the higher 10 bits of the ADAnCR0 to ADAnCR3 registers. The lower 6 bits of these registers are always 0 when read.

The higher 8 bits of the result of A/D conversion are read from the ADAnCR0H to ADAnCR3H registers. To read the result of A/D conversion in 16-bit units, specify the ADAnCR0 to ADAnCR3 registers. To read the higher 8 bits, specify the ADAnCR0H to ADAnCR3H registers.

(7) A/D converter n mode register 0 (ADAnM0) (n = 0, 1)

This register is used to specify the operation mode and controls the conversion operation.

(8) A/D converter n mode register 1 (ADAnM1) (n = 0, 1)

This register is used to set the number of conversion clocks of the analog input to be A/D converted.

(9) A/D converter n channel specification register (ADAnS) (n = 0, 1)

This register is used to specify the analog input pin to be A/D converted.

(10) A/D converter n mode register 2 (ADA2M2) (n = 0, 1)

This register is used to specify the buffer mode and specify the mode in the hardware trigger mode.

(11) ANIn0 to ANIn3 pins (n = 0, 1)

The ANIn0 to ANIn3 pins are analog input pins for A/D converters 0 and 1. They input the analog signals to be A/D converted.

Caution Make sure that the voltages input to ANIn0 to ANIn3 do not exceed the rated values. If a voltage higher than or equal to AV_{REFn} or lower than or equal to AV_{SSn} (even within the range of the absolute maximum ratings) is input to a channel, the conversion value of the channel is undefined, and the conversion values of the other channels may also be affected.

(12) AV_{REF0} and AV_{REF1} pins

This is the pin for inputting the reference voltage of A/D converters 0 and 1. It converts signals input to the ANIn0 to ANIn3 pins to digital signals based on the voltage applied between AV_{REFn} and AV_{SSn} (n= 0, 1). Always make the potential at the AV_{REFn} pin the same as that at the EV_{DD} pin even when A/D converters 0 and 1 are not used.

The operating voltage range of the AV_{REFn} pin is $V_{DD} = EV_{DD} = AV_{DDn} = AV_{REFn}$ = 4.5 to 5.5 V.

(c) One-shot select mode

In this mode, the analog input pin (ANInm) specified by the ADAnS register is A/D converted once. The conversion results are stored in the A/Dn conversion result register (ADAnCRm) corresponding to the ANInm pin. In this mode, the 1-buffer mode and 4-buffer mode are provided for storing the A/D conversion results.

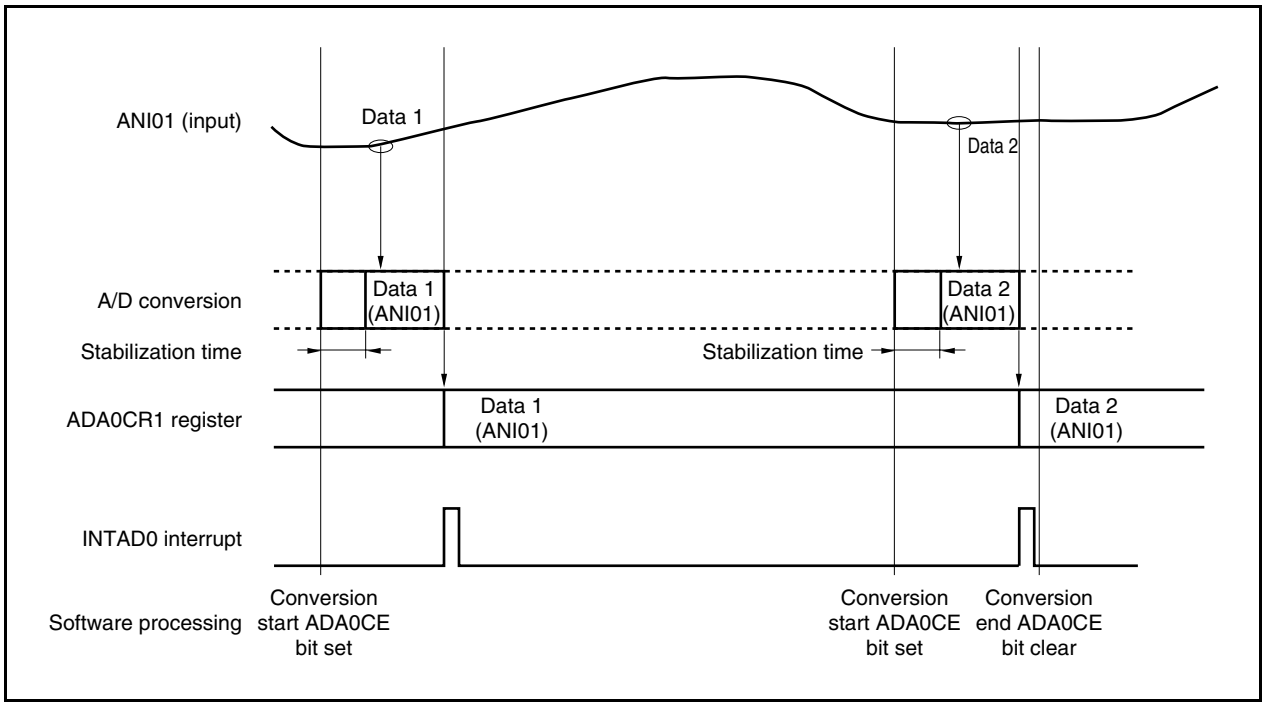
- **1-buffer mode**

  In this mode, the voltage of the analog input pin (ANInm) specified by the ADAnS register is A/D converted. The conversion results are stored in the ADAnCRm register corresponding to the ANInm pin. The ANInm pin and the ADAnCRm register correspond one to one, and an A/Dn conversion end interrupt request signal (INTADn) is generated each time one A/D conversion ends.

  After the end of A/D conversion, the conversion operation is stopped.

Remark n = 0, 1, m = 0 to 3

Figure 11-7. One-Shot Select 1-Buffer Mode Operation Timing (When ADA0M0.ADA0MD1 and ADA0M0.ADA0MD0 Bits = 10, ADA0M2.ADA0BS Bit = 0, ADA0S.ADA0S1 and ADA0S.ADA0S0 Bits = 01)



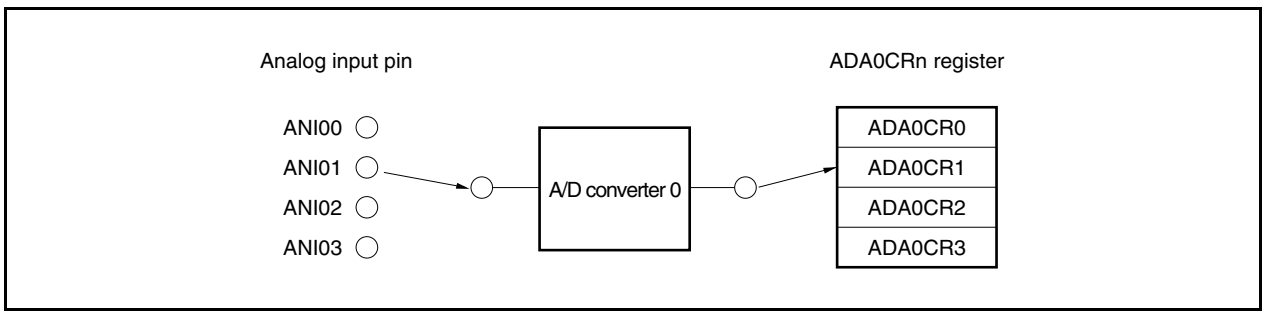


Table 14-1. Interrupt Source List (1/3)

Type	Classification	Default Priority	Name	Generating Source	Generating Unit	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Reset	Interrupt	–	RESET	$\overline{\text{RESET}}$ pin input	Pin	0000H	00000000H	Undefined	–
				WDT overflow (WDTRES)	WDT				
				Low-voltage detection (LVIRES)	POC/LVI				
Non-maskable	Interrupt	–	INTWDT	WDT overflow	WDT	0010H	00000010H	nextPC	–
Software exception	Exception	–	TRAP0n[Note 1]	TRAP instruction	–	004nH	00000040H	nextPC	–
	Exception	–	TRAP1n[Note 1]	TRAP instruction	–	005nH	00000050H	nextPC	–
Exception trap	Exception	–	ILGOP/ DBG0	Invalid instruction code/ DBTRAP instruction	–	0060H	00000060H	nextPC	–
Maskable	Interrupt	0	INTP0	INTP0 pin valid edge input	Pin	0080H	00000080H	nextPC	PIC0
	Interrupt	1	INTP1	INTP1 pin valid edge input	Pin	0090H	00000090H	nextPC	PIC1
	Interrupt	2	INTP2	INTP2 pin valid edge input	Pin	00A0H	000000A0H	nextPC	PIC2
	Interrupt	3	INTP3	INTP3 pin valid edge input	Pin	00B0H	000000B0H	nextPC	PIC3
	Interrupt	4	INTP4	INTP4 pin valid edge input	Pin	00C0H	000000C0H	nextPC	PIC4
	Interrupt	5	INTP5	INTP5 pin valid edge input	Pin	00D0H	000000D0H	nextPC	PIC5
	Interrupt	6	INTP6	INTP6 pin valid edge input	Pin	00E0H	000000E0H	nextPC	PIC6
	Interrupt	7	INTLVI	Low-voltage detection	POC/LVI	00F0H	000000F0H	nextPC	LVIIC
	Interrupt	–	–	Not used	–	–	00000100H	–	–
	Interrupt	–	–	Not used	–	–	00000110H	–	–
	Interrupt	8	INTTQ0OV	TMQ0 overflow	TMQ0	0120H	00000120H	nextPC	TQ0OVIC
	Interrupt	9	INTTQ0CC0	TQ0CCR0 capture input/ compare match	TMQ0	0130H	00000130H	nextPC	TQ0CCIC0
	Interrupt	10	INTTQ0CC1	TQ0CCR1 capture input/ compare match	TMQ0	0140H	00000140H	nextPC	TQ0CCIC1
	Interrupt	11	INTTQ0CC2	TQ0CCR2 capture input/ compare match	TMQ0	0150H	00000150H	nextPC	TQ0CCIC2
	Interrupt	12	INTTQ0CC3	TQ0CCR3 capture input/ compare match	TMQ0	0160H	00000160H	nextPC	TQ0CCIC3
	Interrupt	13	INTTQ1OV	TMQ1 overflow[Note 2]	TMQ1	0170H	00000170H	nextPC	TQ1OVIC
	Interrupt	14	INTTQ1CC0	TQ1CCR0 compare match[Note 3]	TMQ1	0180H	00000180H	nextPC	TQ1CCIC0
	Interrupt	15	INTTQ1CC1	TQ1CCR1 compare match	TMQ1	0190H	00000190H	nextPC	TQ1CCIC1
	Interrupt	16	INTTQ1CC2	TQ1CCR2 compare match	TMQ1	01A0H	000001A0H	nextPC	TQ1CCIC2
	Interrupt	17	INTTQ1CC3	TQ1CCR3 compare match	TMQ1	01B0H	000001B0H	nextPC	TQ1CCIC3
	Interrupt	–	–	Not used	–	–	000001C0H	–	–
	Interrupt	–	–	Not used	–	–	000001D0H	–	–

Notes 1. n is the value between 0 to FH.

2. When TMQ1 is used in the 6-phase PWM output mode, it functions as INTTQ1OV (valley interrupt) from the TMQ1 option (TMQOP1).

3. When TMQ1 is used in the 6-phase PWM output mode, it functions as INTTQ1CC0 (crest interrupt) from the TMQ1 option (TMQOP1).

(b) To use for interrupt

When the operation of LVI is enabled, the supply voltage and detection voltage are compared. If the supply voltage is lower than the detection voltage, an interrupt request signal (INTLVI) is generated (when the LVIM.LVIMD bit is cleared to 0).

The following shows the operation setting method and timing chart.

<To start operation>

<1> Mask the interrupt of LVI.

<2> Select the voltage to be detected by using the LVIS.LVIS0 bit.

<3> Set the LVIM.LVION bit to 1 (to enable operation).

<4> Insert a wait cycle of 0.1 ms (TYP) (target value) or more by software.

<5> By using the LVIM.LVIF bit, check if the supply voltage > detection voltage.

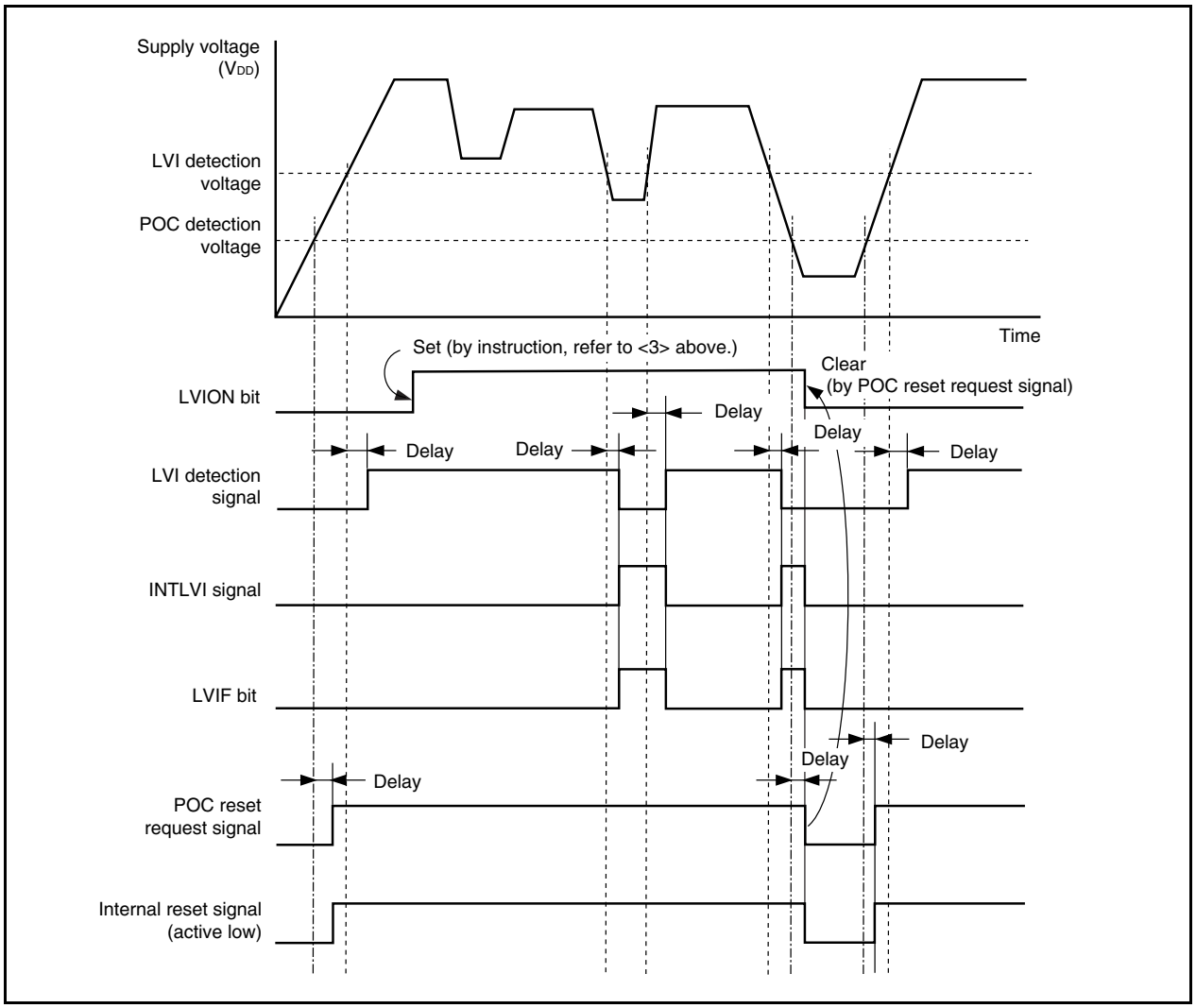
<6> Clear the interrupt request flag of LVI.

<7> Unmask the interrupt of LVI.

<To stop operation>

Clear the LVION bit to 0.

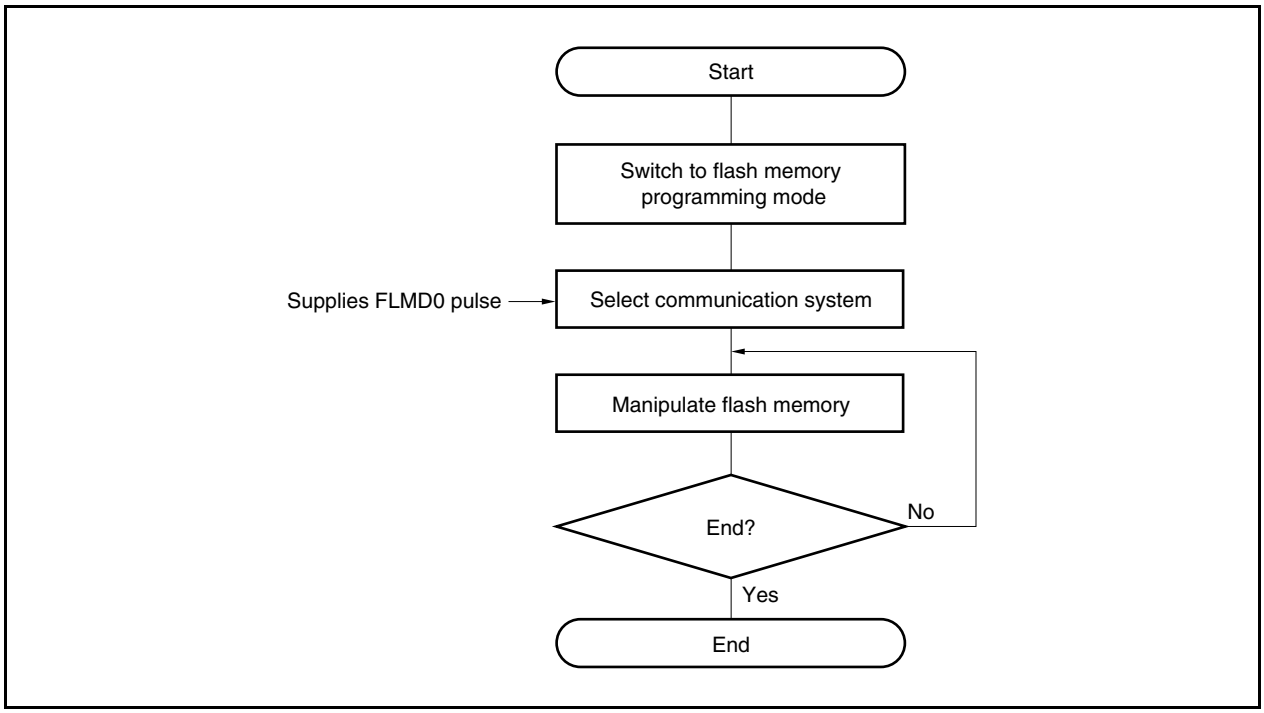
Figure 16-6. Operation Timing of Low-Voltage Detector (LVIMD Bit = 0)



18.4.3 Flash memory control

The following shows the procedure for manipulating the flash memory.

<R> **Figure 18-7. Procedure for Manipulating Flash Memory**



(5/5)

Symbol	Name	Unit	Page
TQ0OVIC	Interrupt control register	INTC	559
TQ1CCIC0	Interrupt control register	INTC	559
TQ1CCIC1	Interrupt control register	INTC	559
TQ1CCIC2	Interrupt control register	INTC	559
TQ1CCIC3	Interrupt control register	INTC	559
TQ1CCR0	TMQ1 capture/compare register 0	Timer	251
TQ1CCR1	TMQ1 capture/compare register 1	Timer	253
TQ1CCR2	TMQ1 capture/compare register 2	Timer	255
TQ1CCR3	TMQ1 capture/compare register 3	Timer	257
TQ1CNT	TMQ1 counter read buffer register	Timer	259
TQ1CTL0	TMQ1 control register 0	Timer	244
TQ1CTL1	TMQ1 control register 1	Timer	244
TQ1DTC	TMQ1 dead-time compare register	Timer	363
TQ1IOC0	TMQ1 I/O control register 0	Timer	246
TQ1IOC3	TMQ1 I/O control register 3	Timer	369
TQ1OPT0	TMQ1 option register 0	Timer	250, 364
TQ1OPT1	TMQ1 option register 1	Timer	365
TQ1OPT2	TMQ1 option register 2	Timer	366
TQ1OPT3	TMQ1 option register 3	Timer	368
TQ1OVIC	Interrupt control register	INTC	559
UA0CTL0	UARTA0 control register 0	UARTA0	477
UA0CTL1	UARTA0 control register 1	UARTA0	478
UA0CTL2	UARTA0 control register 2	UARTA0	478
UA0OPT0	UARTA0 option control register 0	UARTA0	479
UA0REIC	Interrupt control register	INTC	559
UA0RIC	Interrupt control register	INTC	559
UA0RX	UARTA0 receive data register	UARTA0	481
UA0STR	UARTA0 status register	UARTA0	479
UA0TIC	Interrupt control register	INTC	559
UA0TX	UARTA0 transmit data register	UARTA0	481
UA1CTL0	UARTA1 control register 0	UARTA1	477
UA1CTL1	UARTA1 control register 1	UARTA1	478
UA1CTL2	UARTA1 control register 2	UARTA1	478
UA1OPT0	UARTA1 option control register 0	UARTA1	479
UA1REIC	Interrupt control register	INTC	559
UA1RIC	Interrupt control register	INTC	559
UA1RX	UARTA1 receive data register	UARTA1	481
UA1STR	UARTA1 status register	UARTA1	479
UA1TIC	Interrupt control register	INTC	559
UA1TX	UARTA1 transmit data register	UARTA1	481
VSWC	System wait control register	BCU	61
WDTE	Watchdog timer enable register	WDT	425
WDTM	Watchdog timer mode register	WDT	424