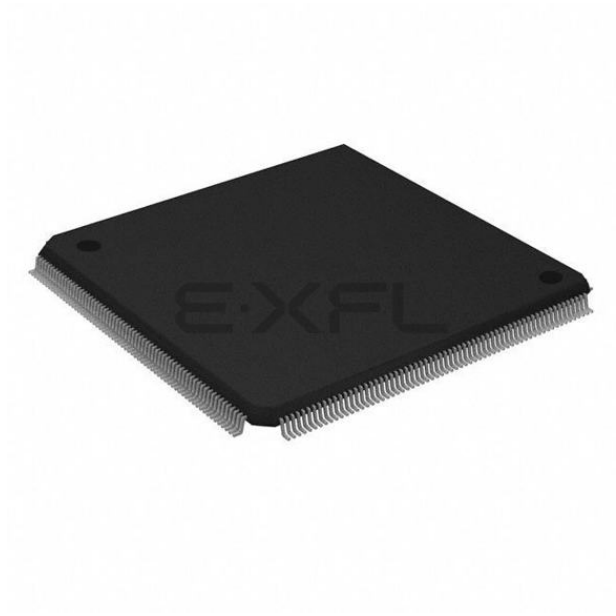
Renesas Electronics America Inc - R7S721000VLFP#AA0 Datasheet



Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DVD, VDC
Ethernet	10/100Mbps (1), 100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.2V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-LQFP
Supplier Device Package	256-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s721000vlfp-aa0

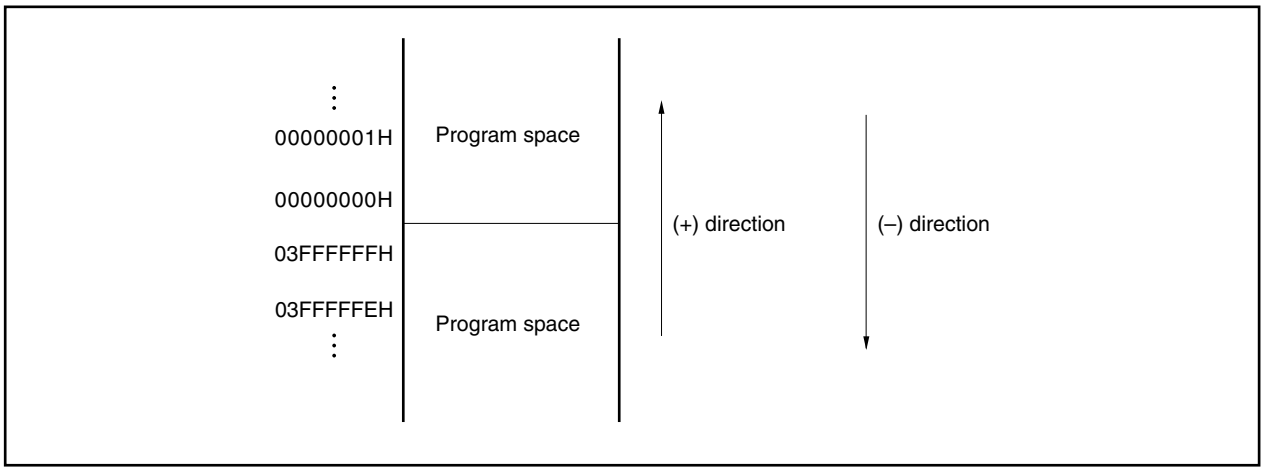
3.4.2 Wraparound of CPU address space

(1) Program space

Of the 32 bits of the program counter (PC), the higher 6 bits are fixed to 0 and only the lower 26 bits are valid. Even if a carry or borrow occurs from bit 25 to bit 26 as a result of branch address calculation, the higher 6 bits ignore this and remain 0.

Therefore, the upper-limit address of the program space, 03FFFFFFH, and the lower-limit address, 00000000H, are contiguous addresses, and the program space is wrapped around at the boundary of these addresses.

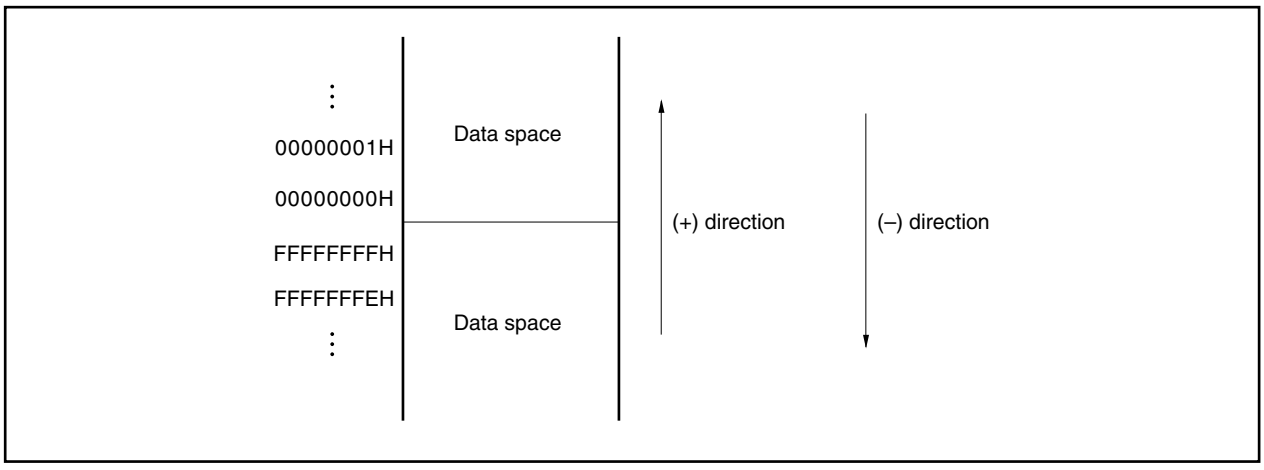
Caution No instructions can be fetched from the 4 KB area of 03FFF000H to 03FFFFFFH because this area is an on-chip peripheral I/O area. Therefore, do not execute any branch operation instructions in which the destination address will reside in any part of this area.



(2) Data space

The result of an operand address calculation that exceeds 32 bits is ignored.

Therefore, the upper-limit address of the data space, FFFFFFFFH, and the lower-limit address, 00000000H, are contiguous addresses, and the data space is wrapped around at the boundary of these addresses.



(1) Registers

(a) Port 2 register (P2)

After reset: Undefined R/W Address: FFFFF404H

	7	6	5	4	3	2	1	0
P2	P27	P26	P25	P24	P23	P22	P21	P20

P2n	Control of output data (in output mode) (n = 0 to 7)
0	Output 0.
1	Output 1.

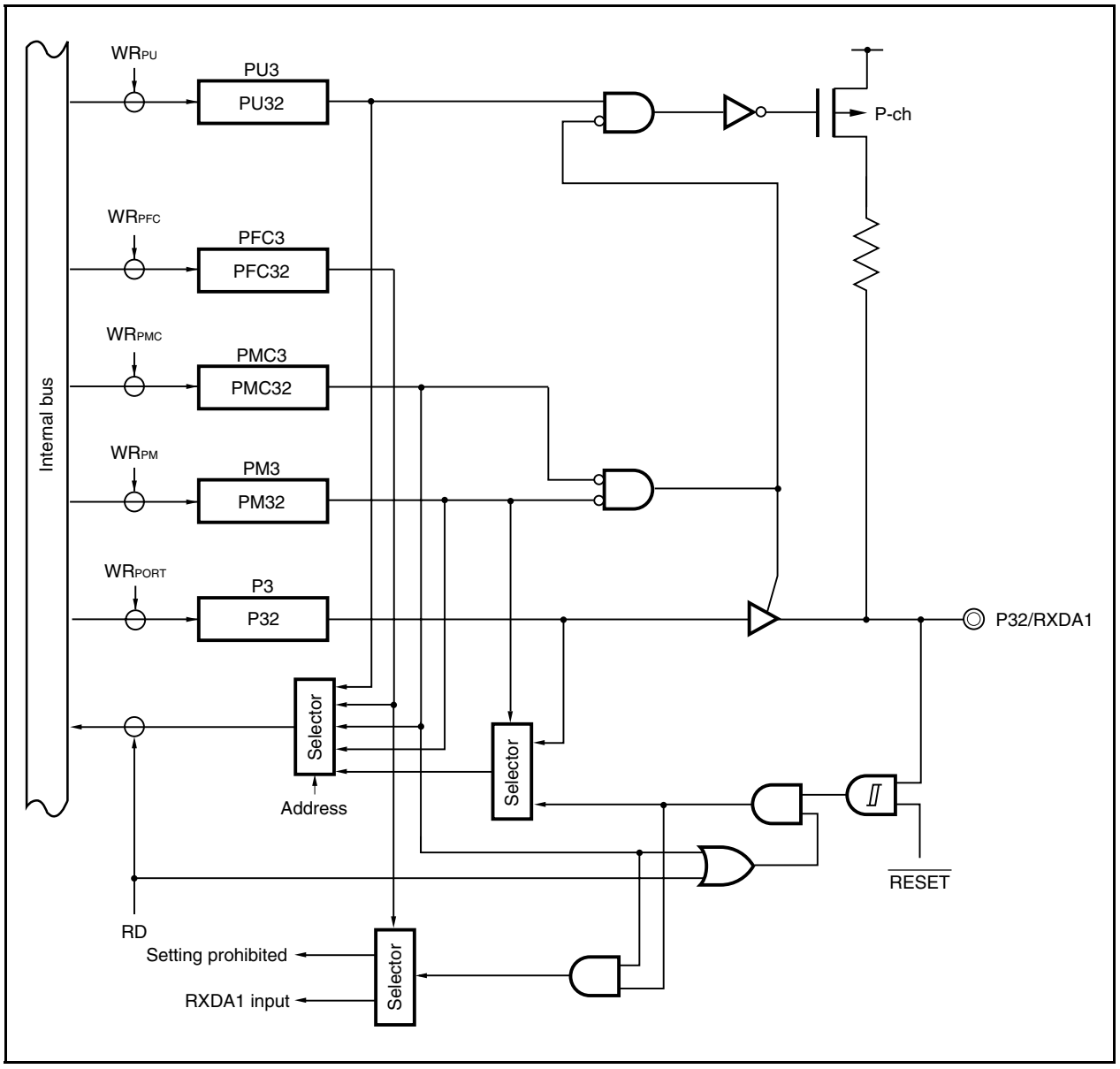
(b) Port 2 mode register (PM2)

After reset: FFH R/W Address: FFFFF424H

	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

PM2n	Control of input/output mode (in port mode) (n = 0 to 7)
0	Output mode
1	Input mode

Figure 4-15. Block Diagram of P32 Pin



CHAPTER 6 16-BIT TIMER/EVENT COUNTER P (TMP)

Timer P (TMP) is a 16-bit timer/event counter.
The V850ES/IE2 incorporates TMP0 to TMP3.

6.1 Overview

The TMPn of channels are outlined below (n = 0 to 3).

Table 6-1. TMPn Overview

Item	TMP0	TMP1	TMP2	TMP3
Clock selection	8 ways	8 ways	8 ways	8 ways
Capture trigger input pin	2	None	2	None
External event count input pin	1	None	1	None
External trigger input pin	1	None	1	None
Timer counter	1	1	1	1
Capture/compare register	2	2 Note	2	2 Note
Capture/compare match interrupt request signal	2	2 Note	2	2 Note
<R> Overflow interrupt request signal	1	1	1	1
Timer output pin	2	None	1	1

Note Compare function only

6.2 Functions

The functions of TMPn that can be realized differ from one channel to another, as shown in the table below (n = 0 to 3).

Table 6-2. TMPn Functions

Function	TMP0	TMP1	TMP2	TMP3
Interval timer	√	√	√	√
External event counter	√	×	√	×
External trigger pulse output	√	×	√	√ Note
One-shot pulse output	√	×	√	√ Note
PWM output	√	×	√	√
Free-running timer	√	√	√	√
Pulse width measurement	√	×	√	×
Timer tuning operation	×	√ (TMQ1)	×	×

Note Realized by software trigger only. External trigger input cannot be used.

(6) TMPn option register 0 (TPnOPT0)

The TPnOPT0 register is an 8-bit register that sets the capture/compare operation and detects overflow.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: TP0OPT0 FFFFF645H, TP1OPT0 FFFFF665H, TP2OPT0 FFFFF685H, TP3OPT0 FFFFF6A5H

TPnOPT0 (n = 0 to 3, k = 0, 2)

7	6	5	4	3	2	1	<0>
0	0	TPkCCS1[Note]	TPkCCS0[Note]	0	0	0	TPnOVF

TPkCCS1[Note]	TPkCCR1 register capture/compare selection
0	Compare register selected
1	Capture register selected (cleared by TPkCTL0.TPkCE bit = 0)
The TPkCCS1 bit setting is valid only in the free-running timer mode.	

TPkCCS0[Note]	TPkCCR0 register capture/compare selection
0	Compare register selected
1	Capture register selected (cleared by TPkCTL0.TPkCE bit = 0)
The TPkCCS0 bit setting is valid only in the free-running timer mode.	

TPnOVF	TMPn overflow detection flag
Set (1)	Overflow occurred
Reset (0)	0 written to TPnOVF bit or TPnCTL0.TPnCE bit = 0
• The TPnOVF bit is set to 1 when the 16-bit counter value overflows from FFFFH to 0000H in the free-running timer mode or the pulse width measurement mode. • An overflow interrupt request signal (INTTPnOV) is generated at the same time that the TPnOVF bit is set to 1. The INTTPnOV signal is not generated in modes other than the free-running timer mode and the pulse width measurement mode. • The TPnOVF bit is not cleared to 0 even when the TPnOVF bit or the TPnOPT0 register is read when the TPnOVF bit = 1. • Before clearing the TPnOVF bit to 0 after generation of the INTTPnOV signal, be sure to confirm (by reading) that the TPnOVF bit is set to 1. • The TPnOVF bit can be both read and written, but the TPnOVF bit cannot be set to 1 by software. Writing 1 has no effect on the operation of TMPn.	

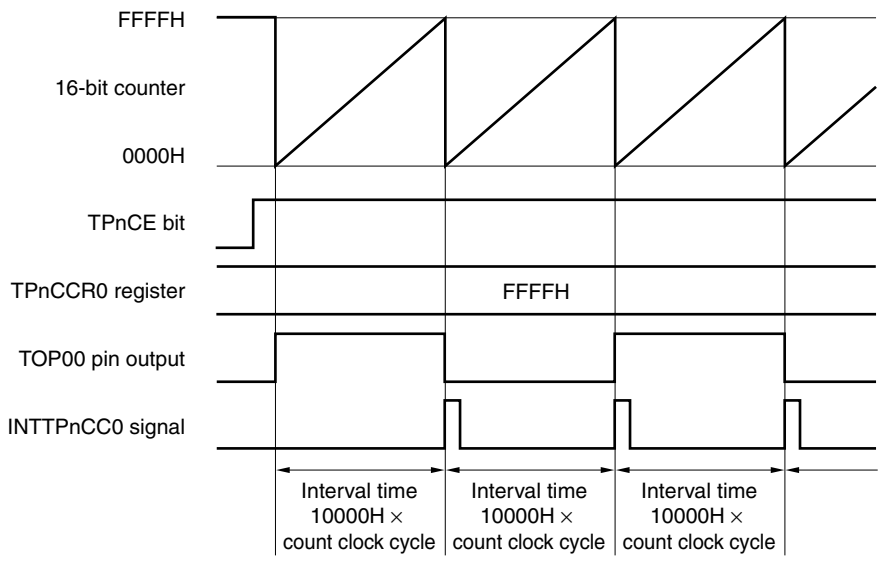
Note Valid only for TMP0 and TMP2. Be sure to clear bits 5 and 4 of TMP1 and TMP3 to 0.

Cautions 1. Rewrite the TPkCCS1 and TPkCCS0 bits when the TPkCE bit = 0. (The same value can be written when the TPkCE bit = 1.) If rewriting was mistakenly performed, clear the TPkCE bit to 0 and then set the bits again.

2. Be sure to clear bits 1 to 3, 6, and 7 to "0".

(b) Operation if TPnCCR0 register is set to FFFFH

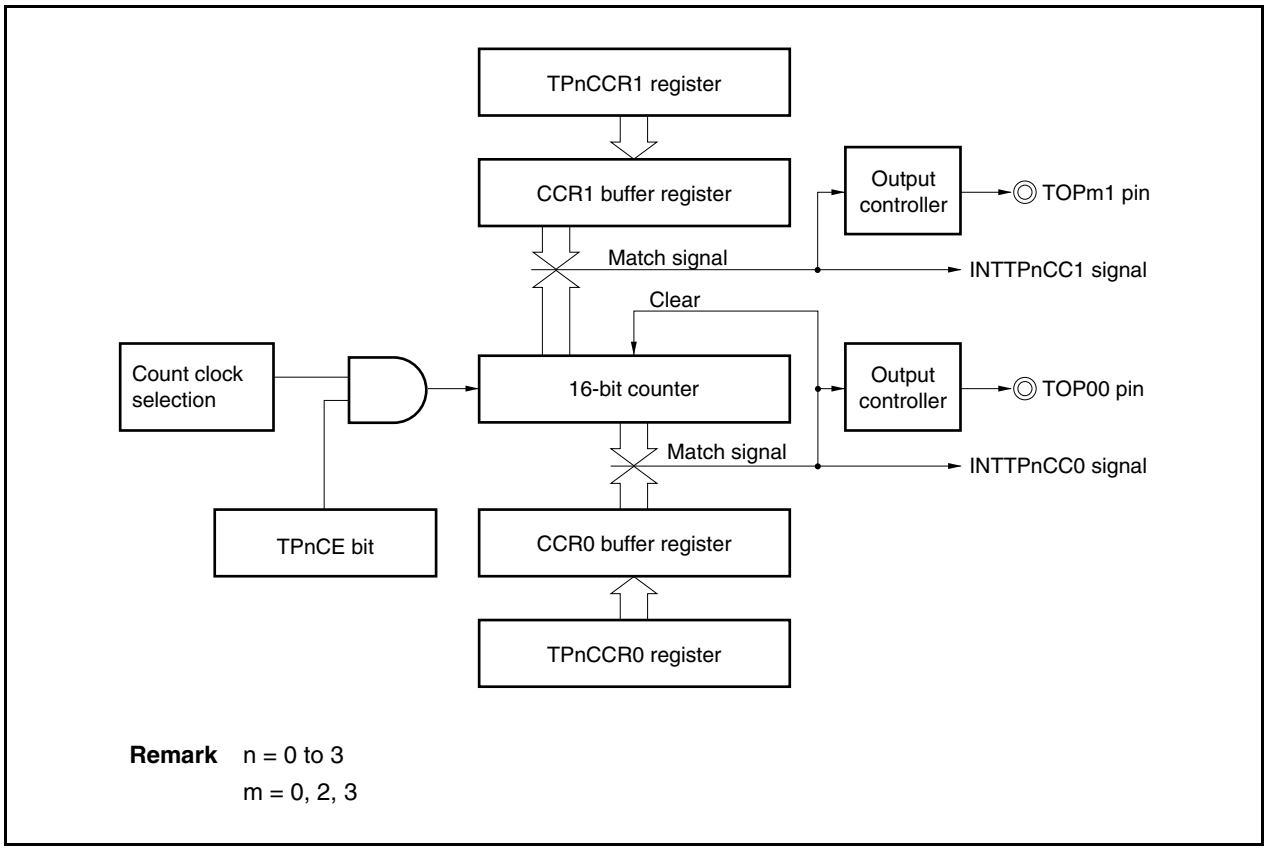
If the TPnCCR0 register is set to FFFFH, the 16-bit counter counts up to FFFFH. The counter is cleared to 0000H in synchronization with the next count-up timing. The INTTPnCC0 signal is generated and the output of the TOP00 pin is inverted. At this time, an overflow interrupt request signal (INTTPnOV) is not generated, nor is the overflow flag (TPnOPT0.TPnOVF bit) set to 1.



Remark n = 0 to 3

(d) Operation of TPnCCR1 register

Figure 6-13. Configuration of TPnCCR1 Register



Remark n = 0 to 3
m = 0, 2, 3

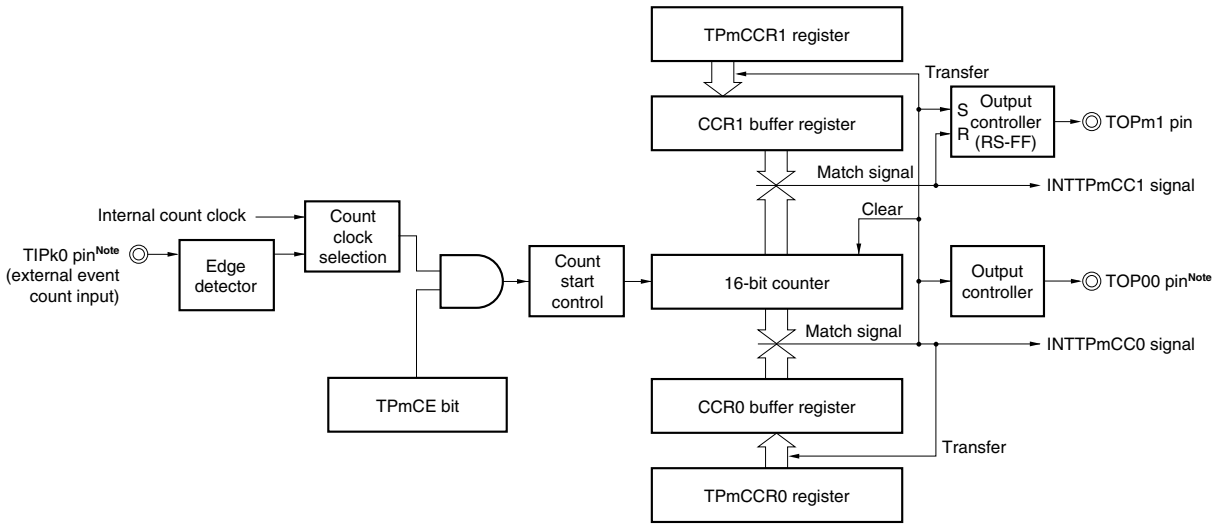
6.6.5 PWM output mode (TPmMD2 to TPmMD0 bits = 100)

This mode is valid only in TMP0, TMP2, and TMP3.

In the PWM output mode, a PWM waveform is output from the TOPm1 pin when the TPmCTL0.TPmCE bit is set to 1.

In addition, a PWM waveform with a duty factor of 50% with the set value of the TPmCCR0 register + 1 as half its cycle is output from the TOP00 pin.

Figure 6-31. Configuration in PWM Output Mode

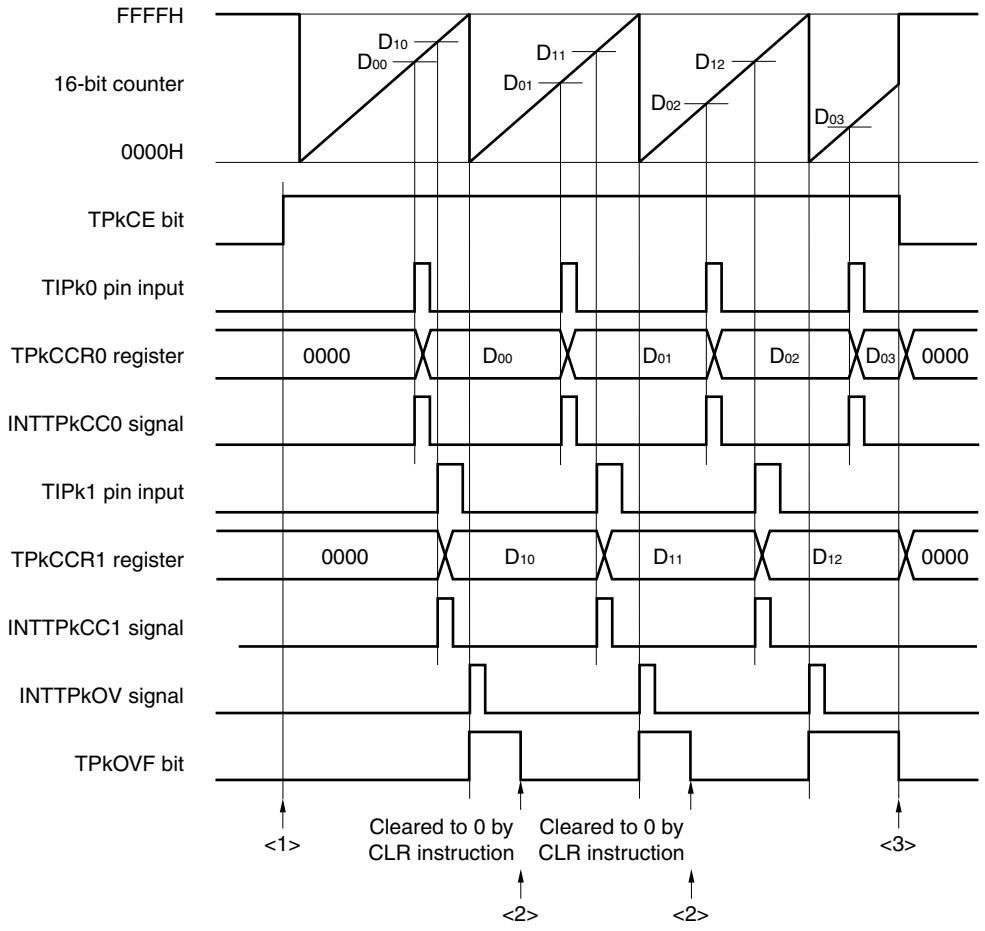


Note Because the external event count input pin (TIP00) and timer output pin (TOP00) share the same alternate-function pin, two functions cannot be used at the same time.

Remark m = 0, 2, 3
k = 0, 2

(b) When using capture/compare register as capture register

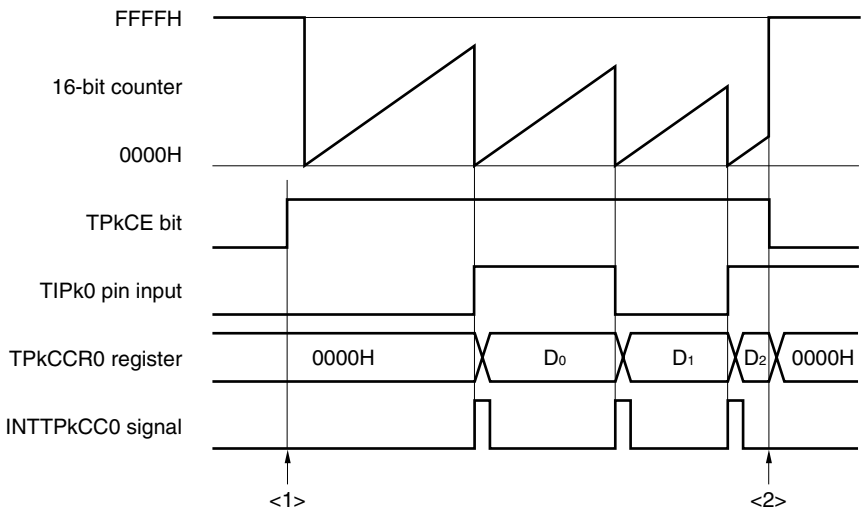
Figure 6-40. Software Processing Flow in Free-Running Timer Mode (Capture Function) (1/2)



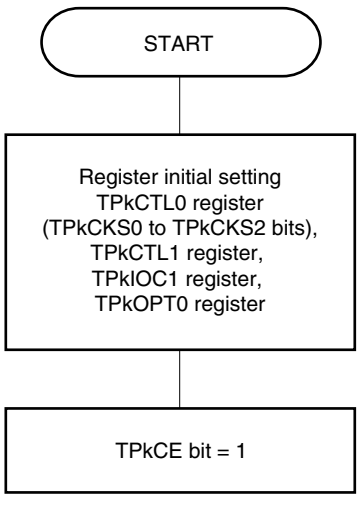
Remark k = 0, 2

(1) Operation flow in pulse width measurement mode

Figure 6-44. Software Processing Flow in Pulse Width Measurement Mode



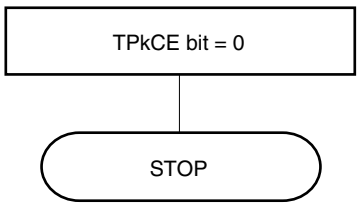
<R> <1> Count operation start flow



Initial setting of these registers is performed before setting the TPkCE bit to 1.

The TPkCKS0 to TPkCKS2 bits can be set at the same time when counting has been started (TPkCE bit = 1).

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TPkCE bit to 0.

Remark k = 0, 2

(2/2)

Cautions 2. Rewrite the TQnOLm and TQnOEm bits when the TQnCTL0.TQnCE bit = 0. (The same value can be written when the TQnCE bit = 1.) If rewriting was mistakenly performed, clear (0) the TQnCE bit and then set the bits again.

3. If the TQnOLm bit is manipulated when the TQnCE and TQnOE bits are 0, the output level of the TOQnm, TOQH0b, and TOQ1Tb pins changes.

4. To generate the TOQ1Tb pin output and the A/D conversion start trigger signal of A/D converters 0 and 1 in the 6-phase PWM output mode, be sure to set the TOQ1Tb pin output mode using the TQ1IOC0 register. At this time, be sure to clear the TQ1OL0 bit to 0 and set the TQ1OE0 bit to 1 (b = 1 to 3).

7.6 Operation

The functions that can be realized differ between TMQ0 and TMQ1. The functions of each channel are shown below.

Table 7-10. TMQ0 Specifications in Each Mode

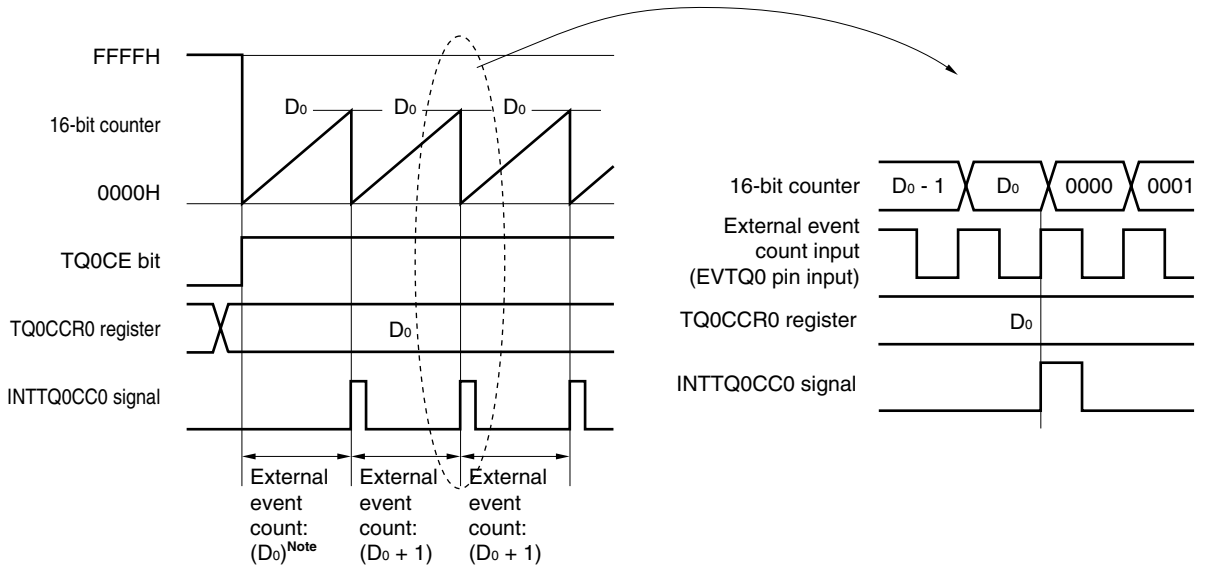
Operation	TQ0CTL1.TQ0EST Bit (Software Trigger Bit)	Capture/Compare Register Setting	Compare Register Write Method
Interval timer mode	Invalid	Compare only	Anytime write
External event count mode	Invalid	Compare only	Anytime write
External trigger pulse output mode	Valid	Compare only	Batch write
One-shot pulse output mode	Valid	Compare only	Anytime write
PWM output mode	Invalid	Compare only	Batch write
Free-running timer mode	Invalid	Switchable	Anytime write
Pulse width measurement mode	Invalid	Capture only	Not applicable

Table 7-11. TMQ1 Specifications in Each Mode

Operation	Software Trigger Bit	Capture/Compare Register Setting	Compare Register Write Method
Interval timer mode	Invalid	Compare only	Anytime write
External event count mode	None		
External trigger pulse output mode	None		
One-shot pulse output mode	None		
PWM output mode	None		
Free-running timer mode	Invalid	Compare only	Anytime write
Pulse width measurement mode	None		

Remark TMQ1 has a function to execute tuning with TMP1. For details, see **CHAPTER 9 MOTOR CONTROL FUNCTION**.

Figure 7-16. Basic Timing in External Event Count Mode

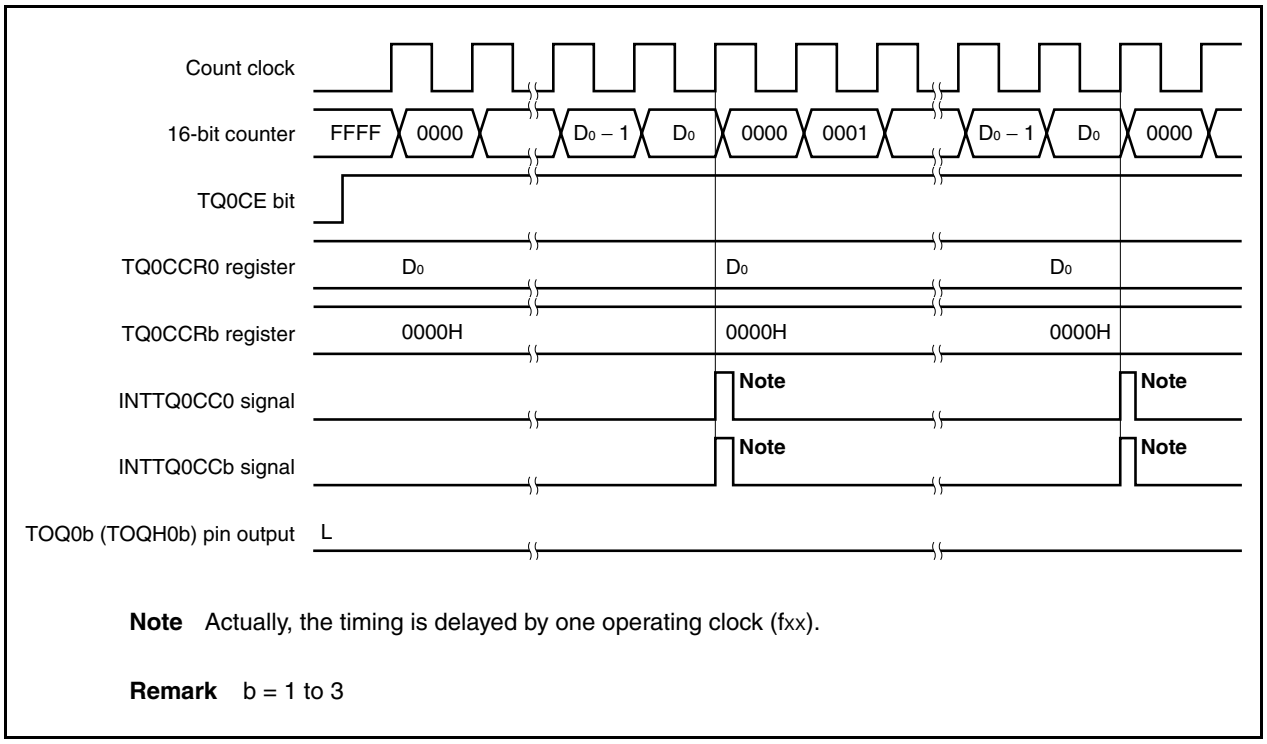


Note In the external event count mode, when the TQ0CTL0.TQ0CE bit is set to 1 (operation starts), the 16-bit counter is cleared from FFFFH to 0000H at the same time. The first count operation starts from 0001H every time the valid edge of the external event count input is detected. Therefore, the count of the first count operation is one number smaller than the count of second or subsequent count operation.

Remark This figure shows the basic timing when the rising edge is specified as the valid edge of the external event count input.

(b) 0%/100% output of PWM waveform

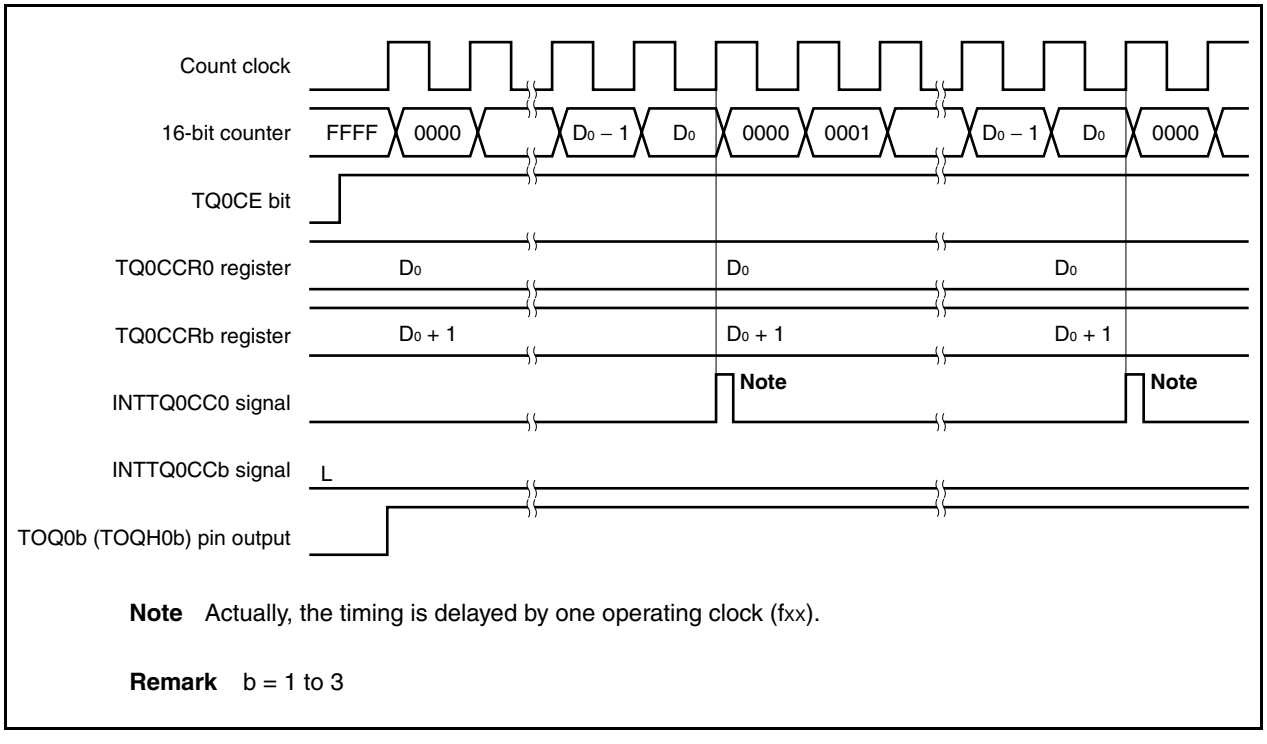
To output a 0% waveform, set the TQ0CCRb register to 0000H. The 16-bit counter is cleared to 0000H and the INTTQ0CC0 and INTTQ0CCb signals are generated at the next timing after a match between the count value of the 16-bit counter and the value of the CCR0 buffer register.



Note Actually, the timing is delayed by one operating clock (fxx).

Remark b = 1 to 3

To output a 100% waveform, set a value of (set value of TQ0CCR0 register + 1) to the TQ0CCRb register. If the set value of the TQ0CCR0 register is FFFFH, 100% output cannot be produced.

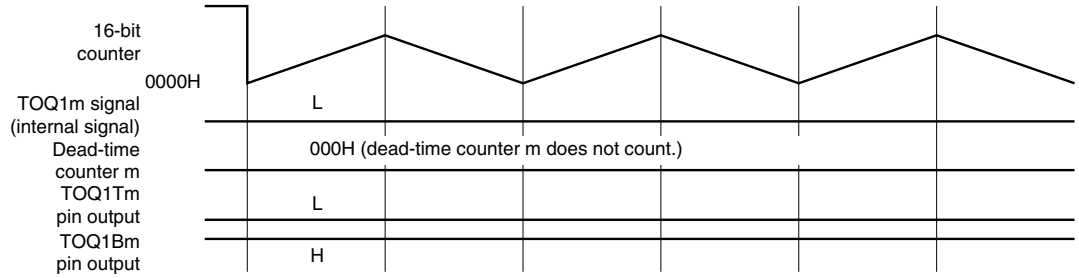


Note Actually, the timing is delayed by one operating clock (fxx).

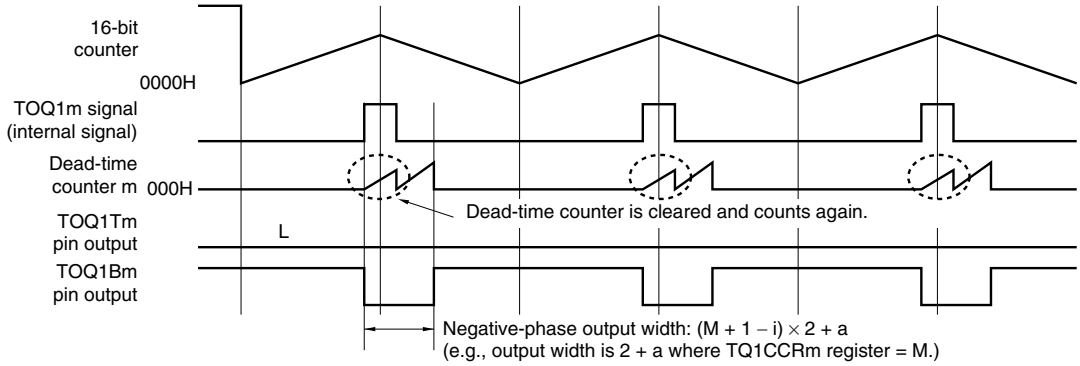
Remark b = 1 to 3

Figure 9-12. PWM Output Waveform with Dead Time (2)

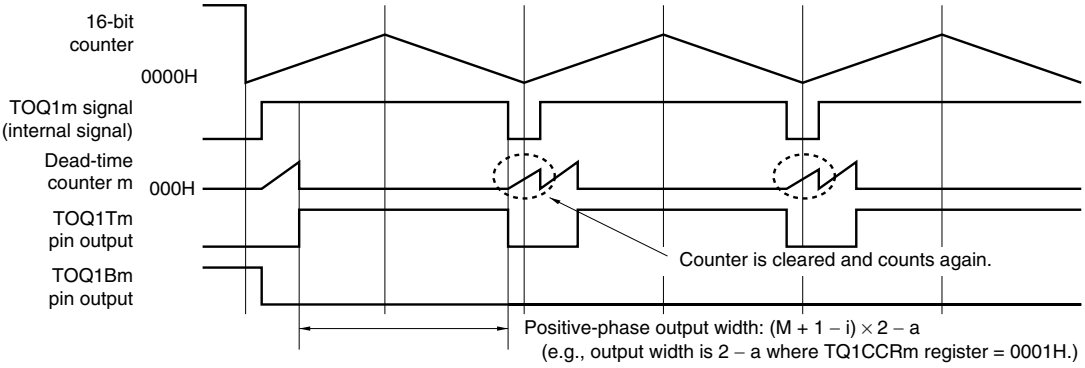
(a) 0% output (TQ1CCRm register = M + 1, TQ1CCR0 register = M, TQ1DTC register = a)



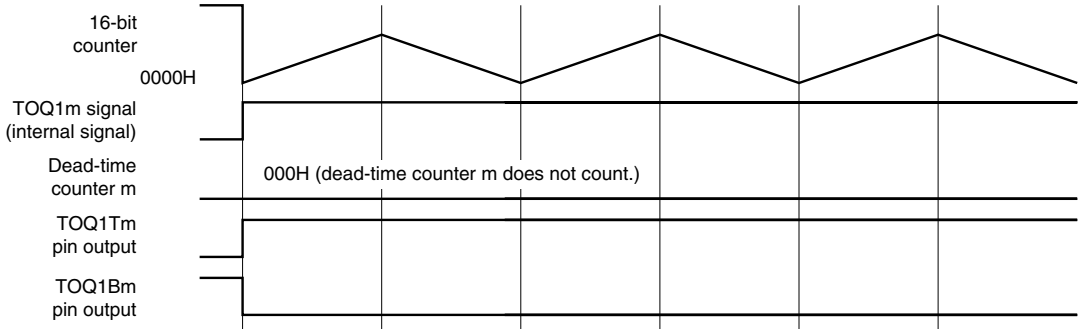
(b) In vicinity of 0% output (TQ1CCRm register = i ≥ M + 1 − a/2, TQ1CCR0 register = M, TQ1DTC register = a)



(c) In vicinity of 100% output (TQ1CCRm register = i ≤ a/2, TQ1CCR0 register = M, TQ1DTC register = a)

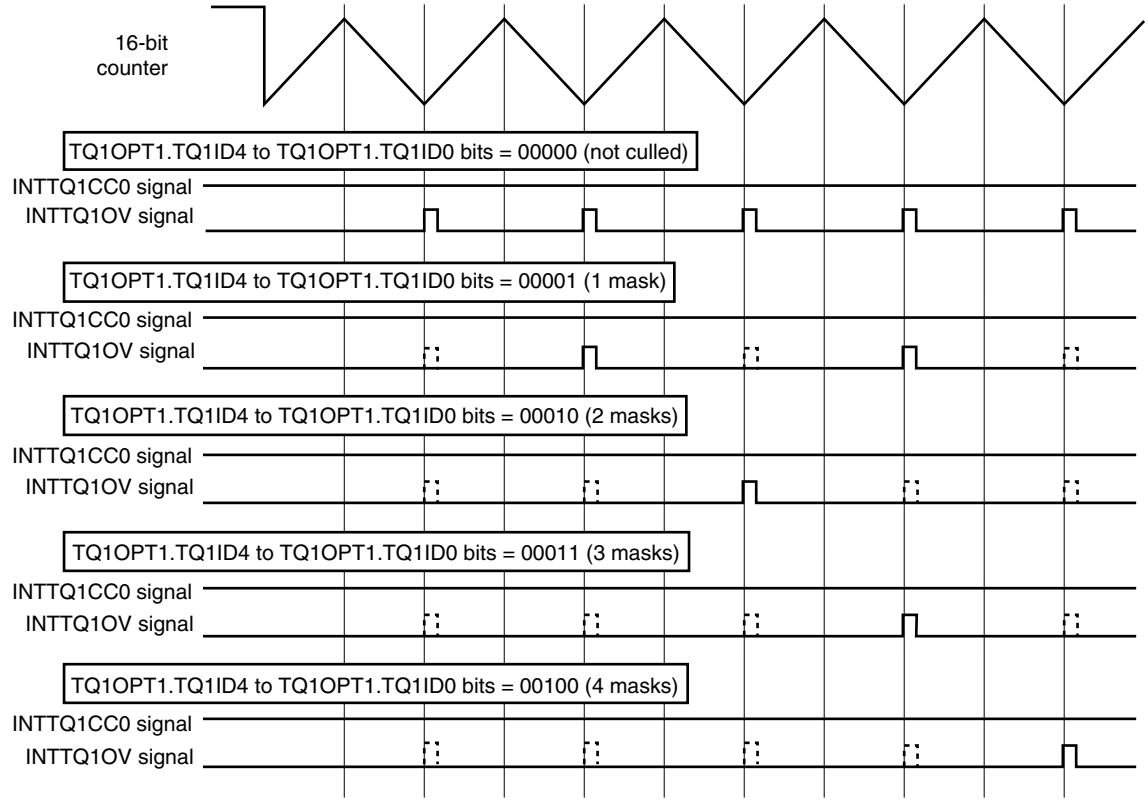


(d) 100% output (TQ1CCRm register = 0000H, TQ1CCR0 register = M, TQ1DTC register = a)



Remark m = 1 to 3

Figure 9-17. Interrupt Culling Operation When TQ1OPT1.TQ1ICE Bit = 0, TQ1OPT1.TQ1IOE Bit = 1, TQ1OPT2.TQ1RDE Bit = 1 (Valley Interrupt Output)



Remark : Culled interrupt

(2) Tuning operation clearing procedure

To clear the tuning operation and exit the 6-phase PWM output mode, set the TMP1 and TMQ1 registers using the following procedure.

<1> Clear the TQ1CTL0.TQ1CE bit to 0 and stop the timer operation.

<2> Clear the TP1CTL0.TP1CE bit to 0 so that TMP1 can be separated.

<3> Stop the timer output by using the TQ1IOC0 register.

<4> Clear the TP1CTL1.TP1SYE bit to 0 to clear the tuning operation.

Caution Manipulating (reading/writing) the other TMQ1, TMP1, and TMQ1 option registers is prohibited until the TQ1CE bit is set to 0 and then the TP1CE bit is set to 0.

(3) When not tuning TMP1

When the match interrupt signal of TMP1 is not necessary as the conversion trigger source that starts A/D converters 0 and 1, TMP1 can be used independently as a separate timer without being tuned. In this case, the match interrupt signal of TMP1 cannot be used as a trigger source to start A/D conversion in the 6-phase PWM output mode. Therefore, fix the TQ1OPT2.TQ1AT00 to TQ1OPT2.TQ1AT03 bits and the TQ1OPT3.TQ1AT10 to TQ1OPT3.TQ1AT13 bits to 0.

The other control bits can be used in the same manner as when TMP1 is tuned.

If TMP1 is not tuned, the compare registers (TP1CCR0 and TP1CCR1) of TMP1 are not affected by the setting of the TQ1OPT0.TQ1CMS and TQ1OPT2.TQ1RDE bit. For the initialization procedure when TMP1 is not tuned, see (b) to (e) in **9.4.5 (1) Tuning operation starting procedure**. (a) is not necessary because it is a step used to set TMP1 for the tuning operation.

(4) Basic operation of TMP1 during tuning operation

The 16-bit counter of TMP1 only counts up. The 16-bit counter is cleared by the set cycle value of the TQ1CCR0 register and starts counting from 0000H again. The count value of this counter is the same as the value of the 16-bit counter of TMQ1 when it counts up. However, it is not the same when the 16-bit counter of TMP1 counts down.

- When TMQ1 counts up (same value)
  16-bit counter of TMQ1: 0000H → M (counting up)
  16-bit counter of TMP1: 0000H → M (counting up)
- When TMQ1 counts down (not same value)
  16-bit counter of TMQ1: M + 1 → 0001H (counting down)
  16-bit counter of TMP1: 0000H → M (counting up)

(3) CSIB0 control register 2 (CB0CTL2)

CB0CTL2 is an 8-bit register that controls the number of CSIB0 serial transfer bits.

This register can be read or written in 8-bit units.

Reset sets this register to 00H.

Caution The CB0CTL2 register can be rewritten only when the CB0CTL0.CB0PWR bit = 0 or when both the CB0TXE and CB0RXE bits = 0.

After reset: 00H R/W Address: FFFFFD02H

	7	6	5	4	3	2	1	0
CB0CTL2	0	0	0	0	CB0CL3	CB0CL2	CB0CL1	CB0CL0

CB0CL3	CB0CL2	CB0CL1	CB0CL0	Serial register bit length
0	0	0	0	8 bits
0	0	0	1	9 bits
0	0	1	0	10 bits
0	0	1	1	11 bits
0	1	0	0	12 bits
0	1	0	1	13 bits
0	1	1	0	14 bits
0	1	1	1	15 bits
1	×	×	×	16 bits

Remark If the number of transfer bits is other than 8 or 16, prepare and use data stuffed from the LSB of the CB0TX and CB0RX registers.

Table 14-2. Addresses and Bits of Interrupt Control Registers (2/2)

Address	Register	Bit							
		<7>	<6>	5	4	3	2	1	0
FFFFF162H	Not used	–	–	–	–	–	–	–	–
FFFFF164H	Not used	–	–	–	–	–	–	–	–
FFFFF166H	Not used	–	–	–	–	–	–	–	–
FFFFF168H	UA0REIC	UA0REIF	UA0REMK	0	0	0	UA0REPR2	UA0REPR1	UA0REPR0
FFFFF16AH	UA0RIC	UA0RIF	UA0RMK	0	0	0	UA0RPR2	UA0RPR1	UA0RPR0
FFFFF16CH	UA0TIC	UA0TIF	UA0TMK	0	0	0	UA0TPR2	UA0TPR1	UA0TPR0
FFFFF16EH	CB0REIC	CB0REIF	CB0REMK	0	0	0	CB0REPR2	CB0REPR1	CB0REPR0
FFFFF170H	CB0RIC	CB0RIF	CB0RMK	0	0	0	CB0RPR2	CB0RPR1	CB0RPR0
FFFFF172H	CB0TIC	CB0TIF	CB0TMK	0	0	0	CB0TPR2	CB0TPR1	CB0TPR0
FFFFF174H	UA1REIC	UA1REIF	UA1REMK	0	0	0	UA1REPR2	UA1REPR1	UA1REPR0
FFFFF176H	UA1RIC	UA1RIF	UA1RMK	0	0	0	UA1RPR2	UA1RPR1	UA1RPR0
FFFFF178H	UA1TIC	UA1TIF	UA1TMK	0	0	0	UA1TPR2	UA1TPR1	UA1TPR0
FFFFF17AH	Not used	–	–	–	–	–	–	–	–
FFFFF17CH	Not used	–	–	–	–	–	–	–	–
FFFFF17EH	Not used	–	–	–	–	–	–	–	–
FFFFF180H	AD0IC	AD0IF	AD0MK	0	0	0	AD0PR2	AD0PR1	AD0PR0
FFFFF182H	AD1IC	AD1IF	AD1MK	0	0	0	AD1PR2	AD1PR1	AD1PR0
FFFFF184H	Not used	–	–	–	–	–	–	–	–
FFFFF186H	TM0EQIC0	TM0EQIF0	TM0EQMK0	0	0	0	TM0EQPR02	TM0EQPR01	TM0EQPR00

16.3.3 Low-voltage detector (LVI)

(1) Functions

The low-voltage detector (LVI) has the following functions.

- Compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}) and generates an interrupt request signal or internal reset signal when $V_{DD} < V_{LVI}$.
- The level of the supply voltage to be detected can be changed in two steps.
- An interrupt request signal or internal reset signal can be selected.
- Can operate in HALT/IDLE/STOP mode.
- Operation can be stopped by software.

(2) Configuration

The block diagram is shown below.

Figure 16-4. Block Diagram of Low-Voltage Detector