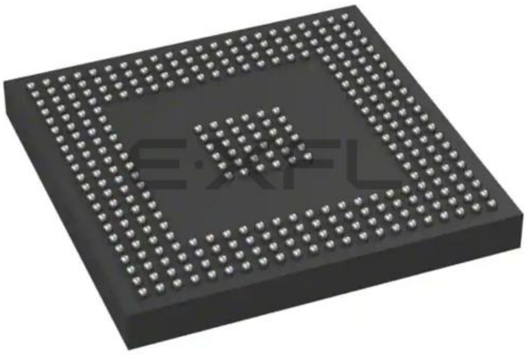
E·XFL Renesas Electronics America Inc - R7S721001VLBG#AC0 Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DVD, VDC
Ethernet	10/100Mbps (1), 100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.2V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	324-FBGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s721001vlbg-ac0

CHAPTER 1 INTRODUCTION

The V850ES/IE2 is one of the low-power operation products in the NEC Electronics V850 Series of single-chip microcontrollers designed for real-time control applications.

1.1 General

The V850ES/IE2 is a 32-bit single-chip microcontroller that includes the V850ES CPU core and peripheral functions such as ROM/RAM, a timer/counter, serial interfaces, a watchdog timer, and an A/D converter.

In addition to high real-time response characteristics and 1-clock-pitch basic instructions, the V850ES/IE2 features instructions such as multiply instructions, saturated operation instructions, and bit manipulation instructions realized by a hardware multiplier, as optimum instructions for digital servo control applications. Moreover, as a real-time control system, the V850ES/IE2 enables an extremely high cost-performance for applications such as motor inverter control.

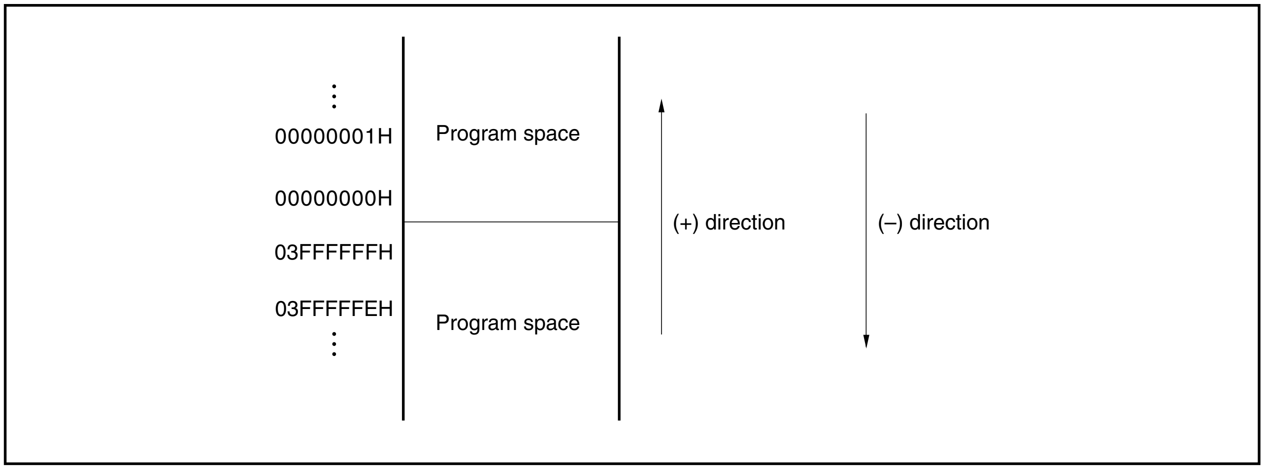
3.4.2 Wraparound of CPU address space

(1) Program space

Of the 32 bits of the program counter (PC), the higher 6 bits are fixed to 0 and only the lower 26 bits are valid. Even if a carry or borrow occurs from bit 25 to bit 26 as a result of branch address calculation, the higher 6 bits ignore this and remain 0.

Therefore, the upper-limit address of the program space, 03FFFFFFH, and the lower-limit address, 00000000H, are contiguous addresses, and the program space is wrapped around at the boundary of these addresses.

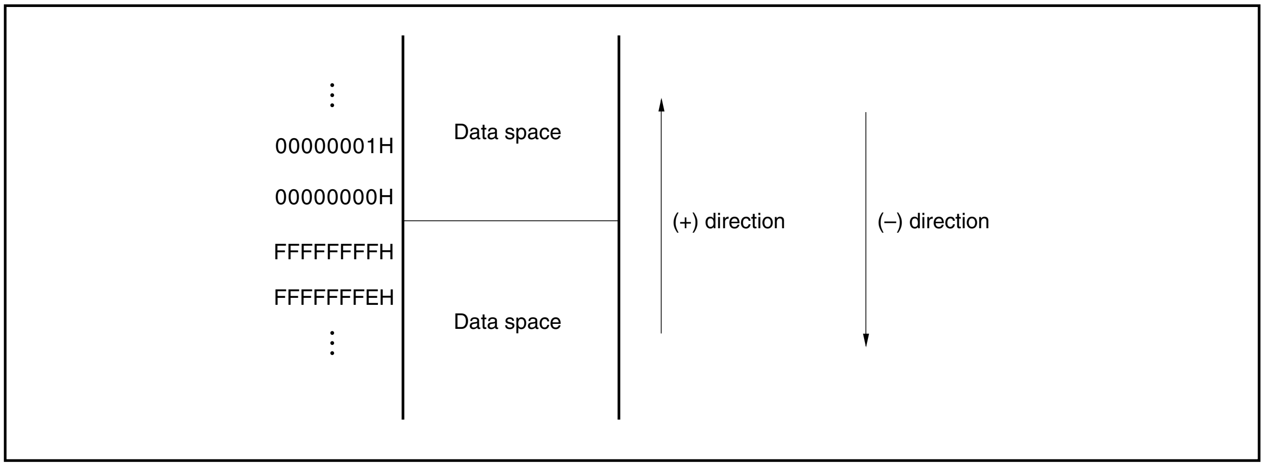
Caution No instructions can be fetched from the 4 KB area of 03FFF000H to 03FFFFFFH because this area is an on-chip peripheral I/O area. Therefore, do not execute any branch operation instructions in which the destination address will reside in any part of this area.



(2) Data space

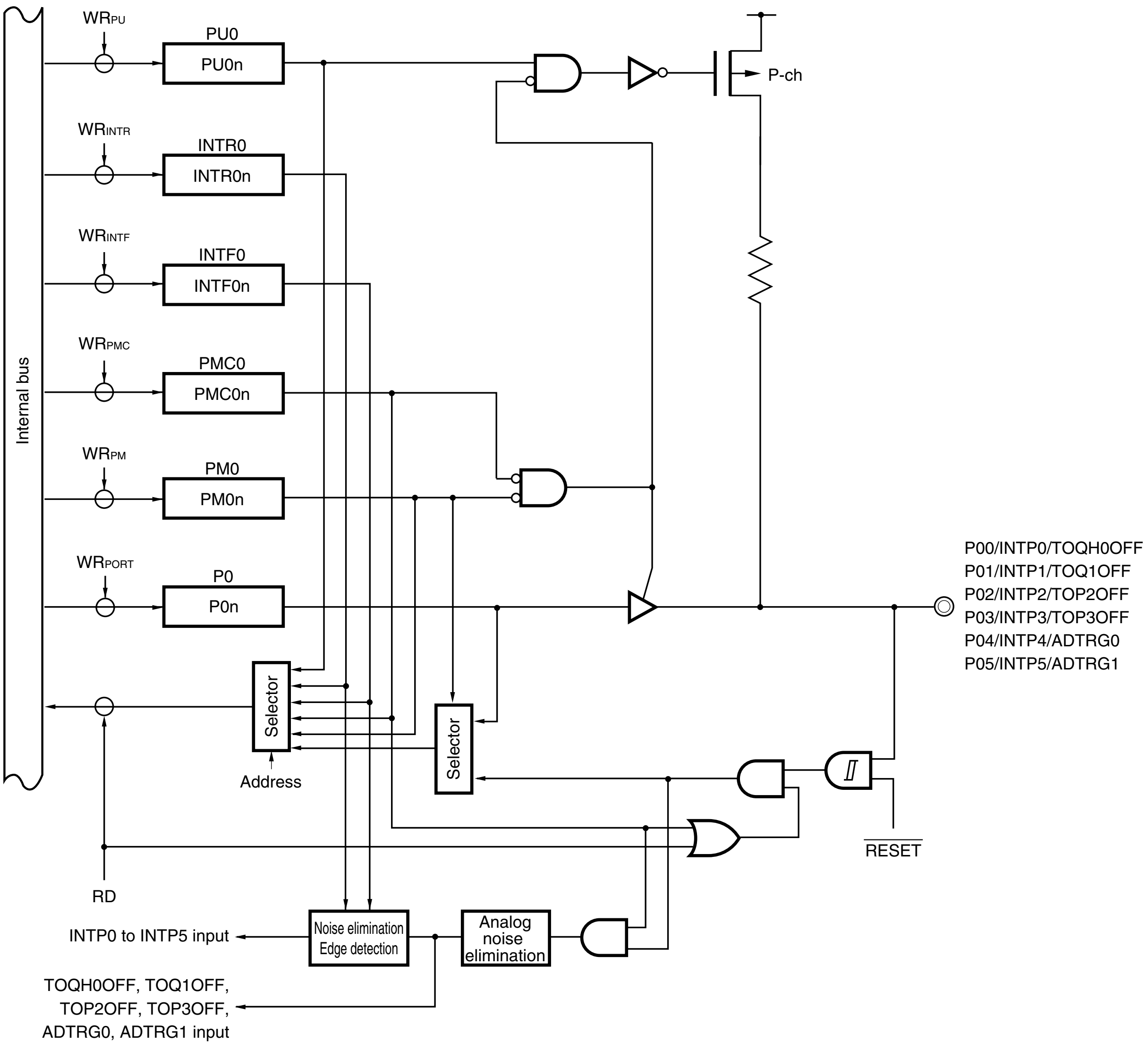
The result of an operand address calculation that exceeds 32 bits is ignored.

Therefore, the upper-limit address of the data space, FFFFFFFFH, and the lower-limit address, 00000000H, are contiguous addresses, and the data space is wrapped around at the boundary of these addresses.



(2) Block diagrams

Figure 4-3. Block Diagram of P00 to P05 Pins



Remark n = 0 to 5

(d) Pull-up resistor option register 2 (PU2)

After reset: 00H R/W Address: FFFFFC44H

	7	6	5	4	3	2	1	0
PU2	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20

PU2n	Control of on-chip pull-up resistor connection (n = 0 to 7)
0	Do not connect
1	Connect[Note]

Note An on-chip pull-up resistor can be connected only when the pins are in input mode in the port mode. Moreover, an on-chip pull-up resistor can only be connected to the TOQ1T1 to TOQ1T3, TOQ1B1 to TOQ1B3, and TOP31 pins when these pins go into a high-impedance state in the alternate-function mode due to the TOQ1OFF or TOP3OFF pin, or software processing. The resistor cannot be connected when the pin is in the output state.

(b) Batch write

In this mode, data is transferred all at once from the TPmCCR0 and TPmCCR1 registers to the CCR0 and CCR1 buffer registers during timer operation. This data is transferred upon a match between the value of the CCR0 buffer register and the value of the 16-bit counter. Transfer is enabled by writing to the TPmCCR1 register.

Whether to enable or disable the next transfer timing is controlled by writing or not writing to the TPmCCR1 register.

In order for the setting value when the TPmCCR0 and TPmCCR1 registers are rewritten to become the 16-bit counter comparison value (in other words, in order for this value to be transferred to the CCR0 and CCR1 buffer registers), it is necessary to rewrite the TPmCCR0 register and then write to the TPmCCR1 register before the 16-bit counter value and the CCR0 buffer register value match. Therefore, the values of the TPmCCR0 and TPmCCR1 registers are transferred to the CCR0 and CCR1 buffer registers upon a match between the count value of the 16-bit counter and the value of the CCR0 buffer register. Thus even when wishing only to rewrite the value of the TPmCCR0 register, also write the same value (same as preset value of the TPmCCR1 register) to the TPmCCR1 register.

When the TPnCE bit is set to 1, the value of the 16-bit counter is cleared from FFFFH to 0000H in synchronization with the count clock, and the counter starts counting. At this time, the output of the TOP00 pin is inverted. Additionally, the set value of the TPnCCR0 register is transferred to the CCR0 buffer register.

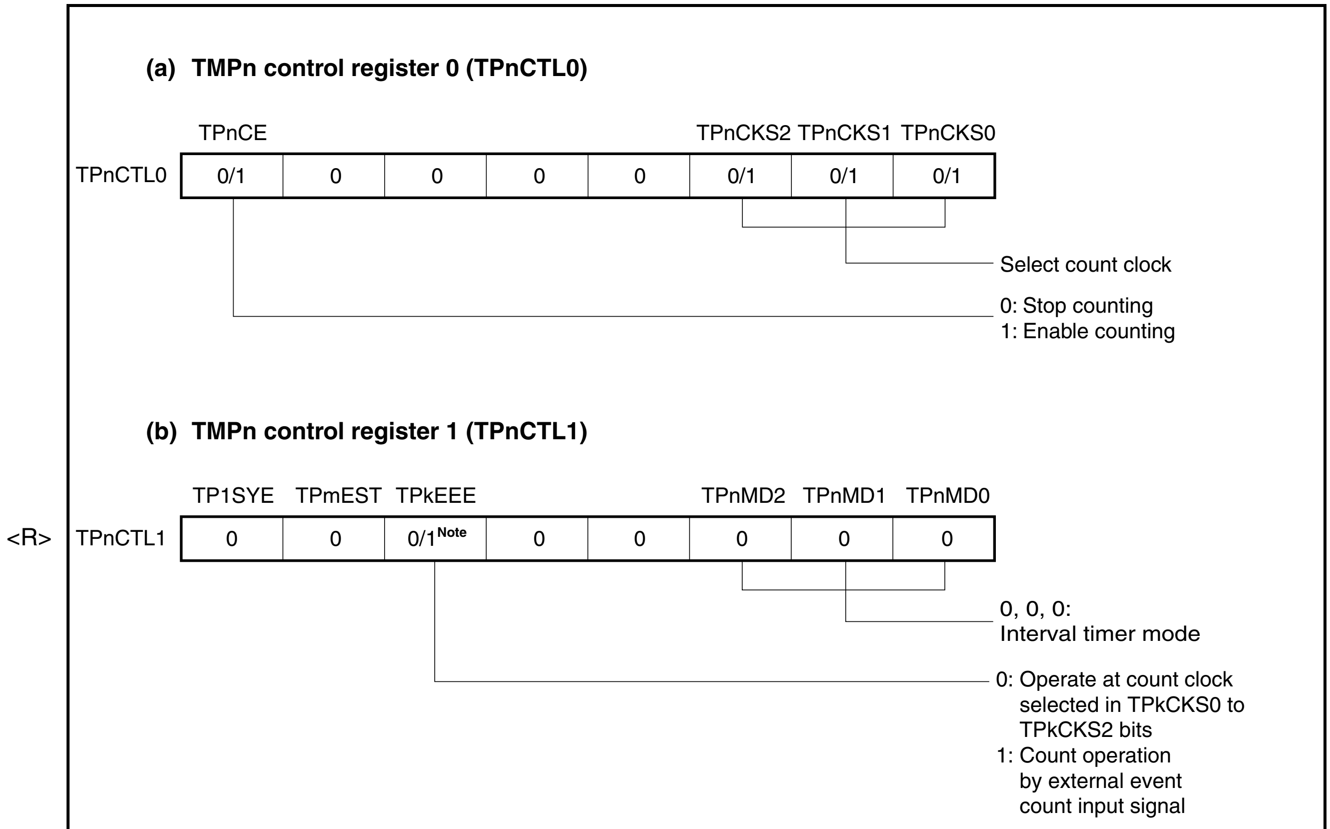
When the count value of the 16-bit counter matches the value of the CCR0 buffer register, the 16-bit counter is cleared to 0000H, the output of the TOP00 pin is inverted, and a compare match interrupt request signal (INTTPnCC0) is generated.

The interval can be calculated by the following expression.

Interval = (Set value of TPnCCR0 register + 1) × Count clock cycle

Remark n = 0 to 3

Figure 6-11. Register Setting for Interval Timer Mode Operation (1/3)



(a) TMPn control register 0 (TPnCTL0)

(b) TMPn control register 1 (TPnCTL1)

<R>
TP1SYE
TPmEST
TPkEEE
TPnMD2
TPnMD1
TPnMD0
TPnCTL1
0
0
0/1Note
0
0
0
0
0
0, 0, 0:
Interval timer mode
0: Operate at count clock selected in TPkCKS0 to TPkCKS2 bits
1: Count operation by external event count input signal

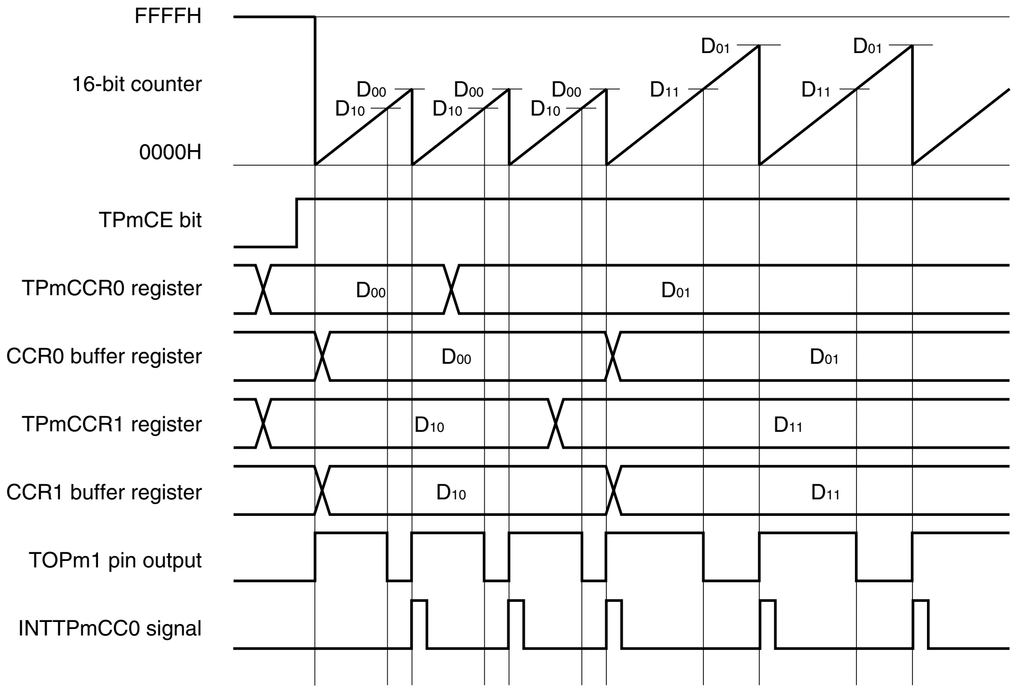
<R> **Note** Enable setting of the TPkEEE bit to 1 only when timer output (TOPk1) is used.
In this case, set the TPkCCR0 and TPkCCR1 registers to the same value.

(2) PWM output mode operation timing

(a) Changing pulse width during operation

To change the PWM waveform while the counter is operating, write the TPmCCR1 register last.

Rewrite the TPmCCRa register after writing the TPmCCR1 register after the INTTPmCC1 signal is detected.



To transfer data from the TPmCCRa register to the CCRa buffer register, the TPmCCR1 register must be written.

To change both the cycle and active level of the PWM waveform at this time, first set the cycle to the TPmCCR0 register and then set the active level to the TPmCCR1 register.

To change only the cycle of the PWM waveform, first set the cycle to the TPmCCR0 register, and then write the same value (same as preset value of the TPmCCR1 register) to the TPmCCR1 register.

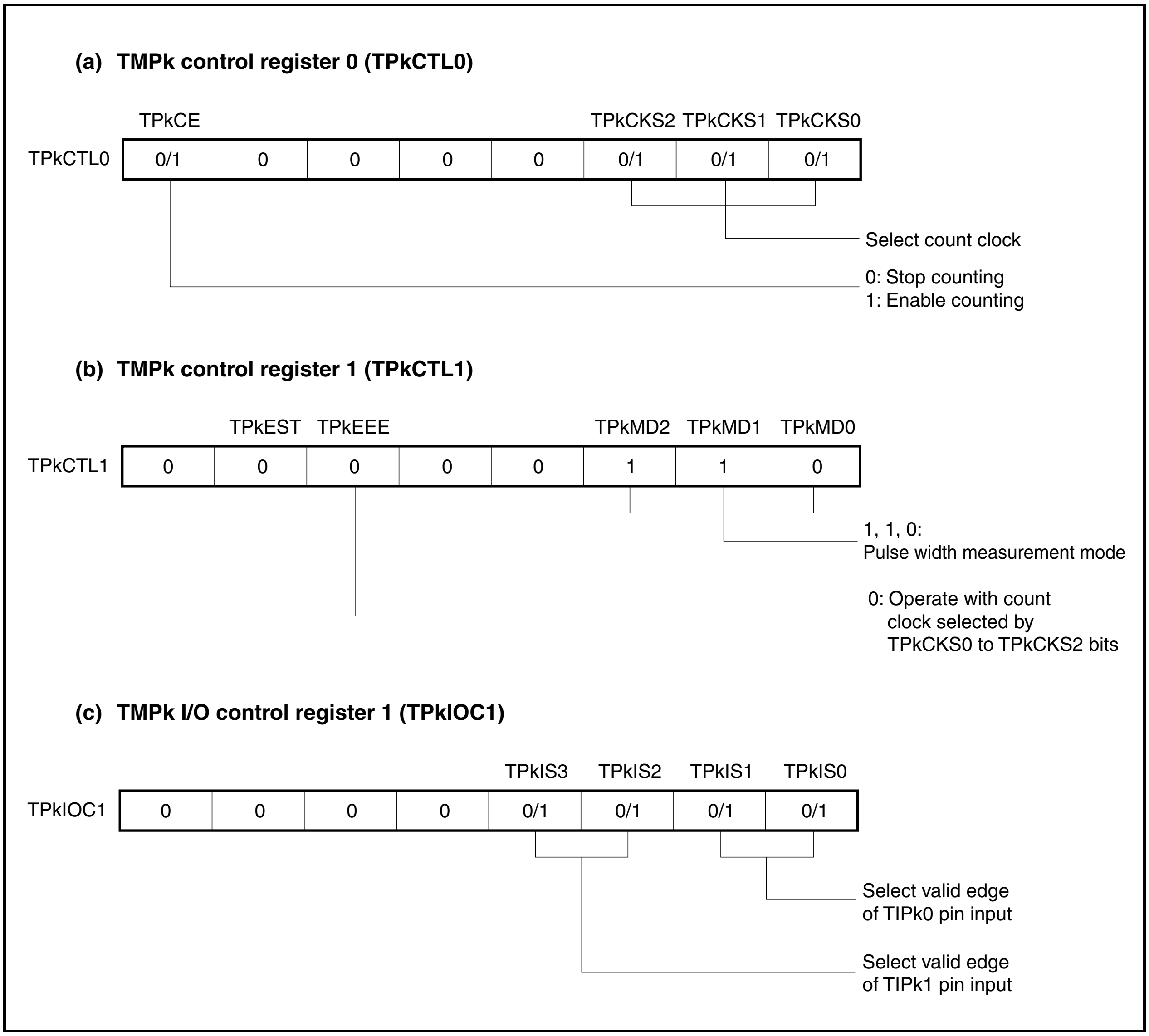
To change only the active level width (duty factor) of the PWM waveform, only the TPmCCR1 register has to be set.

After data is written to the TPmCCR1 register, the value written to the TPmCCRa register is transferred to the CCRa buffer register in synchronization with clearing of the 16-bit counter, and is used as the value compared with the 16-bit counter.

To write the TPmCCR0 or TPmCCR1 register again after writing the TPmCCR1 register once, do so after the INTTPmCC0 signal is generated. Otherwise, the value of the CCRa buffer register may become undefined because the timing of transferring data from the TPmCCRa register to the CCRa buffer register conflicts with writing the TPmCCRa register.

Remark m = 0, 2, 3
a = 0, 1

Figure 6-43. Register Setting in Pulse Width Measurement Mode (1/2)



(a) TMPk control register 0 (TPkCTL0)

<R>

	TPkCE					TPkCKS2	TPkCKS1	TPkCKS0
TPkCTL0	0/1	0	0	0	0	0/1	0/1	0/1

Select count clock
0: Stop counting
1: Enable counting

(b) TMPk control register 1 (TPkCTL1)

<R>

		TPkEST	TPkEEE			TPkMD2	TPkMD1	TPkMD0
TPkCTL1	0	0	0	0	0	1	1	0

1, 1, 0:
Pulse width measurement mode
0: Operate with count clock selected by TPkCKS0 to TPkCKS2 bits

(c) TMPk I/O control register 1 (TPkIOC1)

<R>

					TPkIS3	TPkIS2	TPkIS1	TPkIS0
TPkIOC1	0	0	0	0	0/1	0/1	0/1	0/1

Select valid edge of TIPk0 pin input
Select valid edge of TIPk1 pin input

When the TQ0CE bit is set to 1, the 16-bit counter is cleared from FFFFH to 0000H, starts counting, and outputs PWM waveform from the TOQ0b pin (TOQH0b).

The active level width, cycle, and duty factor of the PWM waveform can be calculated as follows.

Active level width = (Set value of TQ0CCRb register) × Count clock cycle
Cycle = (Set value of TQ0CCR0 register + 1) × Count clock cycle
Duty factor = (Set value of TQ0CCRb register)/(Set value of TQ0CCR0 register + 1)

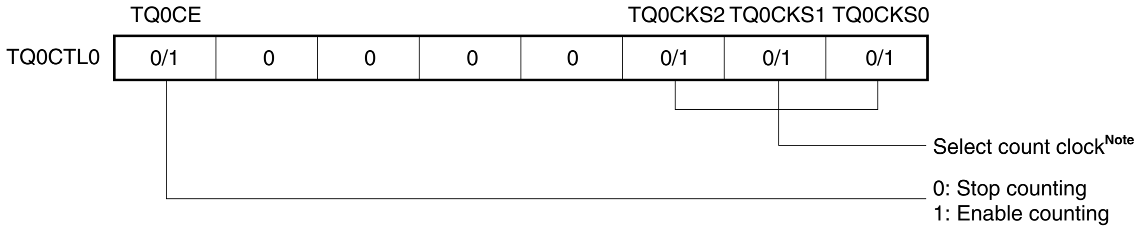
The PWM waveform can be changed by rewriting the TQ0CCRa register while the counter is operating. The newly written value is reflected when the count value of the 16-bit counter matches the value of the CCR0 buffer register and the 16-bit counter is cleared to 0000H.

The compare match interrupt request signal INTTQ0CC0 is generated when the 16-bit counter counts next time after its count value matches the value of the CCR0 buffer register, and the 16-bit counter is cleared to 0000H. The compare match interrupt request signal INTTQ0CCb is generated when the count value of the 16-bit counter matches the value of the CCRb buffer register.

Remark a = 0 to 3
b = 1 to 3

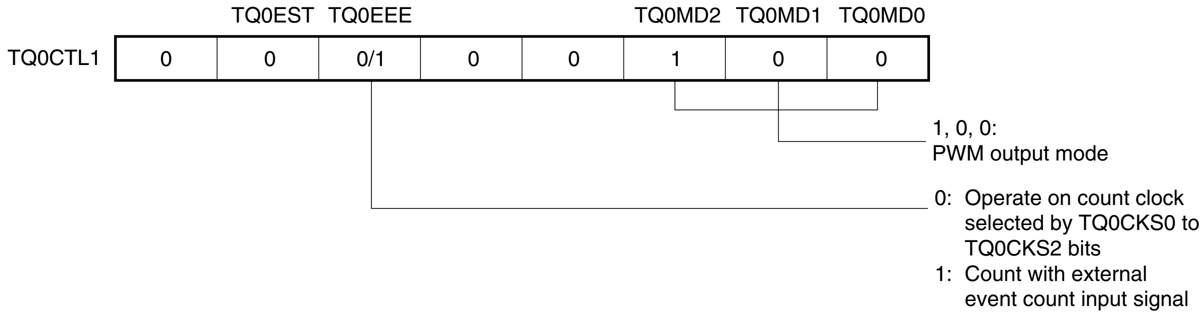
Figure 7-32. Register Setting in PWM Output Mode (1/3)

(a) TMQ0 control register 0 (TQ0CTL0)



Note The setting is invalid when the TQ0CTL1.TQ0EEE bit = 1.

(b) TMQ0 control register 1 (TQ0CTL1)


TQ0EST TQ0EEE
TQ0MD2 TQ0MD1 TQ0MD0
TQ0CTL1
0
0
0/1
0
0
1
0
0
1, 0, 0:
PWM output mode
0: Operate on count clock selected by TQ0CKS0 to TQ0CKS2 bits
1: Count with external event count input signal

To transfer data from the TQ0CCRa register to the CCRa buffer register, the TQ0CCR1 register must be written.

To change both the cycle and active level of the PWM waveform at this time, first set the cycle to the TQ0CCR0 register, set the active level width to the TQ0CCR2 and TQ0CCR3 registers, and then set an active level width to the TQ0CCR1 register.

To change only the cycle of the PWM waveform, first set a cycle to the TQ0CCR0 register, and then write the same value (same as preset value of the TQ0CCR1 register) to the TQ0CCR1 register.

To change only the active level width (duty factor) of PWM wave, first set the active level to the TQ0CCR2 and TQ0CCR3 registers, and then set an active level to the TQ0CCR1 register.

To change only the active level width (duty factor) of the PWM waveform output by the TOQ01 (TOQH01) pin, only the TQ0CCR1 register has to be set.

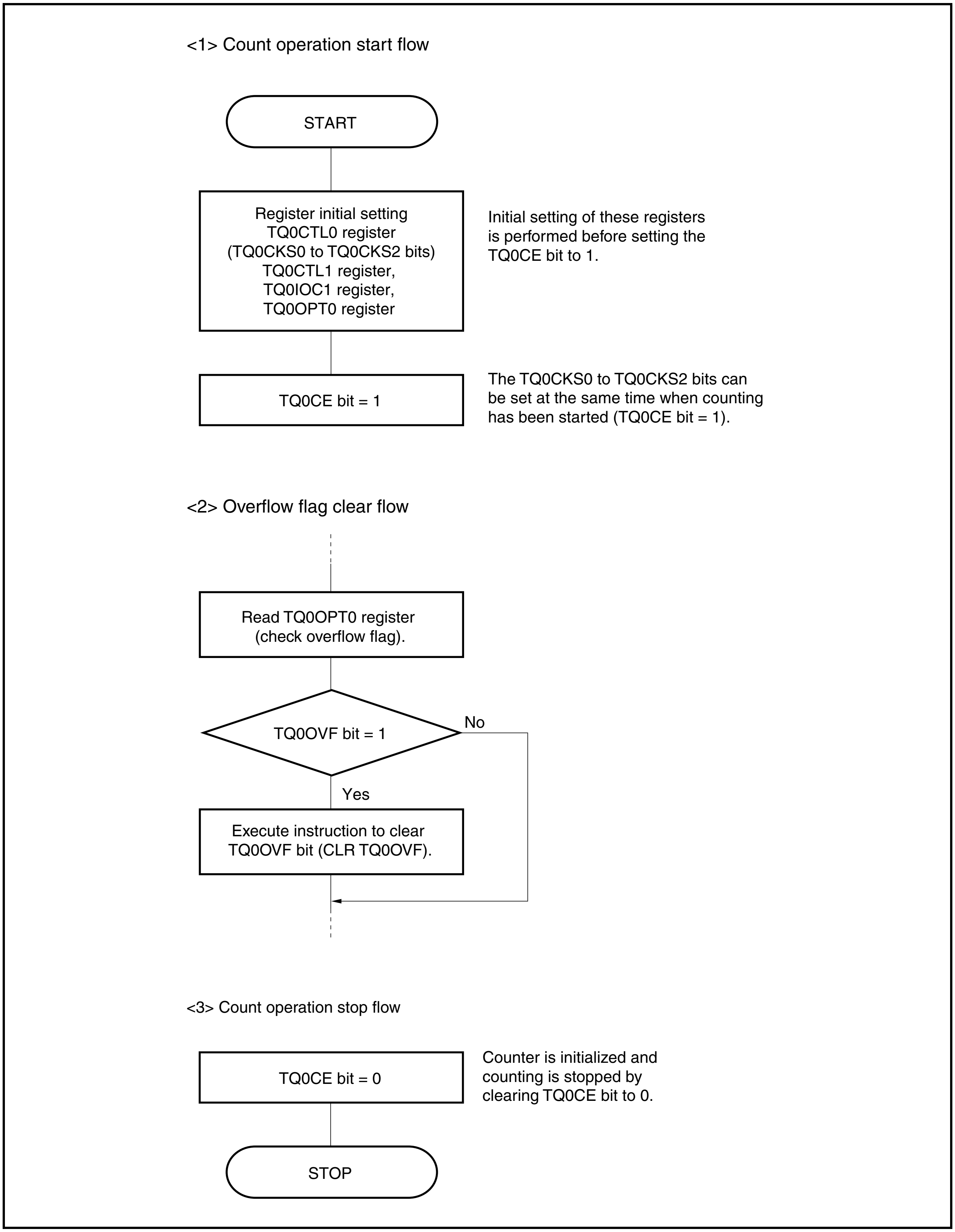
To change only the active level width (duty factor) of the PWM waveform output by the TOQ02 (TOQH02) and TOQ03 (TOQH03) pins, first set an active level width to the TQ0CCR2 and TQ0CCR3 registers, and then write the same value (same as preset value of the TQ0CCR1 register) to the TQ0CCR1 register.

After the TQ0CCR1 register is written, the value written to the TQ0CCRa register is transferred to the CCRa buffer register in synchronization with the timing of clearing the 16-bit counter, and is used as a value to be compared with the value of the 16-bit counter.

To write the TQ0CCR0 to TQ0CCR3 registers again after writing the TQ0CCR1 register once, do so after the INTTQ0CC0 signal is generated. Otherwise, the value of the CCRa buffer register may become undefined because the timing of transferring data from the TQ0CCRa register to the CCRa buffer register conflicts with writing the TQ0CCRa register.

Remark a = 0 to 3

Figure 7-39. Software Processing Flow in Free-Running Timer Mode (Capture Function) (2/2)



Initial setting of these registers is performed before setting the TQ0CE bit to 1.

The TQ0CKS0 to TQ0CKS2 bits can be set at the same time when counting has been started (TQ0CE bit = 1).

Counter is initialized and counting is stopped by clearing TQ0CE bit to 0.

8.3 Control Register

(1) TMM0 control register 0 (TM0CTL0)

The TM0CTL0 register is an 8-bit register that controls the TMM0 operation.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

The same value can always be written to the TM0CTL0 register by software.

After reset: 00H R/W Address: FFFFF540H

	<7>	6	5	4	3	2	1	0
TM0CTL0	TM0CE	0	0	0	0	TM0CKS2	TM0CKS1	TM0CKS0

TM0CE	Internal clock operation enable/disable specification
0	TMM0 operation disabled (16-bit counter reset asynchronously)
1	TMM0 operation enabled. Start operation clock supply. Start TMM0 operation.
The internal clock control and internal circuit reset for TMM0 are performed asynchronously with the TM0CE bit. When the TM0CE bit is cleared to 0, the internal clock of TMM0 is stopped (fixed to low level) and 16-bit counter is reset asynchronously.	

TM0CKS2	TM0CKS1	TM0CKS0	Count clock selection
0	0	0	f_{XX}
0	0	1	$f_{XX}/2$
0	1	0	$f_{XX}/4$
0	1	1	$f_{XX}/8$
1	0	0	$f_{XX}/16$
1	0	1	$f_{XX}/32$
1	1	0	$f_{XX}/64$
1	1	1	$f_{XX}/128$

Cautions 1. Set the TM0CKS2 to TM0CKS0 bits when the TM0CE bit = 0. However, when changing the value of TM0CE from 0 to 1, it is impossible to set the value of the TM0CKS2 to TM0CKS0 bits simultaneously.

2. Be sure to clear bits 3 to 6 to "0".

Remark f_{XX}: Peripheral clock frequency

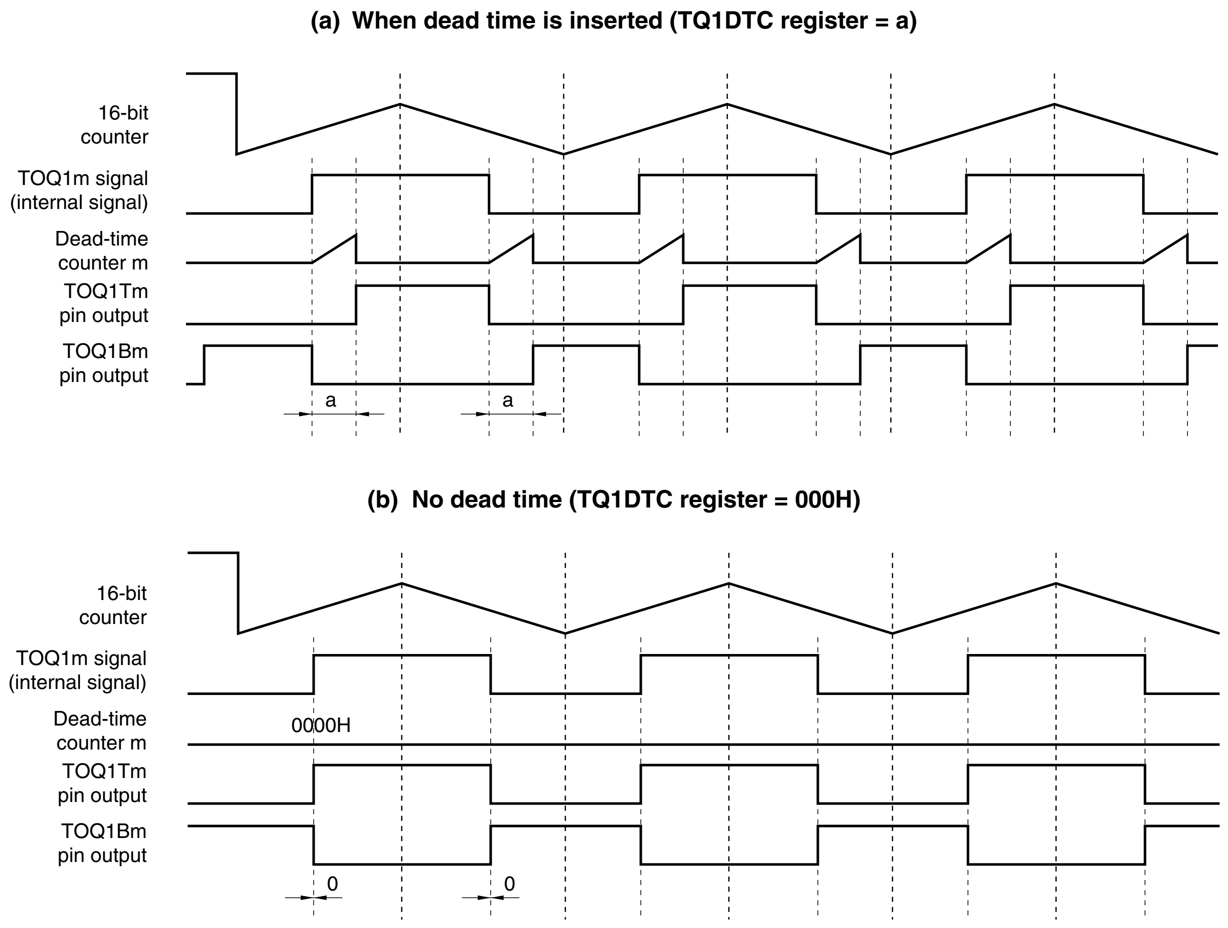
9.4.2 Dead-time control (generation of negative-phase wave signal)

(1) Dead-time control mechanism

In the 6-phase PWM output mode, compare registers 1 to 3 (TQ1CCR1, TQ1CCR2, and TQ1CCR3) are used to set the duty factor, and compare register 0 (TQ1CCR0) is used to set the cycle. By setting these four registers and by starting the operation of TMQ, three types of PWM output waves (basic 3-phase waves) with a variable duty factor are generated. These three PWM output waves are input to the timer Q option unit (TMQOP1) and their inverted signal with dead-time is created to generate three sets of (six) PWM waves.

The TMQOP1 unit consists of three 10-bit counters (dead-time counters 1 to 3) that operate in synchronization with the count clock of TMQ1, and a TMQ1 dead-time compare register (TQ1DTC) that specifies dead time. If “a” is set to the TQ1DTC register, the dead-time value is “a”, and interval “a” is created between a positive-phase wave and a negative-phase wave.

Figure 9-8. PWM Output Wave with Dead Time (1)


(a) When dead time is inserted (TQ1DTC register = a)
16-bit counter
TOQ1m signal (internal signal)
Dead-time counter m
TOQ1Tm pin output
TOQ1Bm pin output
a
a
(b) No dead time (TQ1DTC register = 000H)
16-bit counter
TOQ1m signal (internal signal)
Dead-time counter m
0000H
TOQ1Tm pin output
TOQ1Bm pin output
0
0

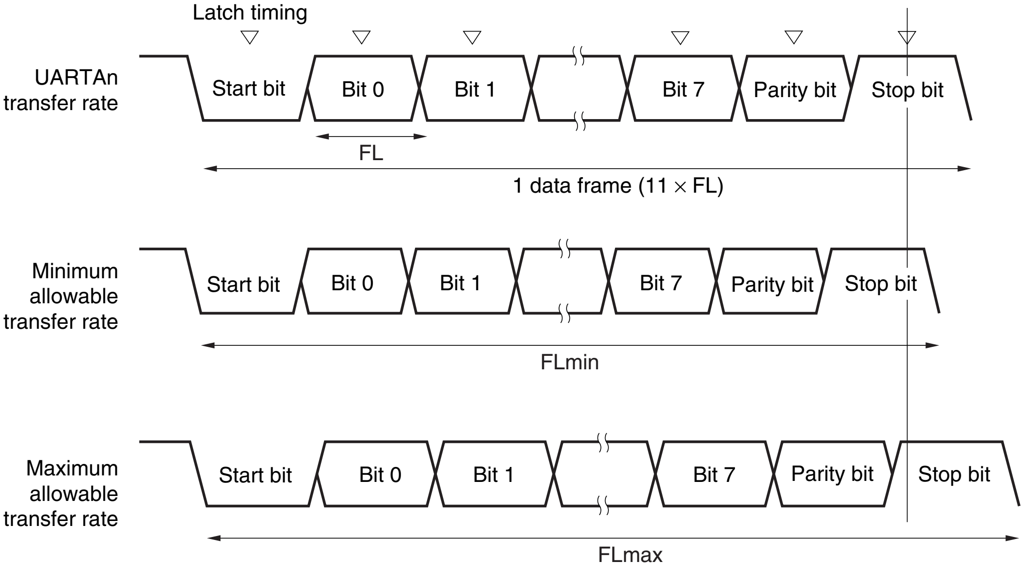
Remark m = 1 to 3

(7) Allowable baud rate range during reception

The baud rate error range at the destination that is allowable during reception is shown below.

Caution The baud rate error during reception must be set within the allowable error range using the following equation.

Figure 12-10. Allowable Baud Rate Range During Reception



Remark n = 0, 1

As shown in Figure 12-10, the receive data latch timing is determined by the counter set using the UAnCTL2 register following start bit detection. The transmit data can be normally received if up to the last data (stop bit) can be received in time for this latch timing.

When this is applied to 11-bit reception, the following is the theoretical result.

$\text{FL} = (\text{Brate})^{-1}$

Brate: UARTAn baud rate (n = 0, 1)
k: Setting value of UAnCTL2.UAnBRS7 to UAnCTL2.UAnBRS0 bits (n = 0, 1)
FL: 1-bit data length
Latch timing margin: 2 clocks

Minimum allowable transfer rate: $\text{FLmin} = 11 \times \text{FL} - \frac{k-2}{2k} \times \text{FL} = \frac{21k+2}{2k}\ \text{FL}$

CHAPTER 13 3-WIRE VARIABLE-LENGTH SERIAL I/O (CSIB)

The V850ES/IE2 incorporates CSIB0.

13.1 Features

- Transfer rate: 8 Mbps (using internal clock)
- Master mode and slave mode selectable
- 8-bit to 16-bit transfer, 3-wire serial interface
- Interrupt request signals (INTCB0RE, INTCB0T, INTCB0R)
- Serial clock and data phase switchable
- Transfer data length selectable in 1-bit units between 8 and 16 bits
- Transfer data MSB-first/LSB-first switchable
- 3-wire transfer SOB0: Serial data output
  SIB0: Serial data input
  $\overline{\text{SCKB0}}$: Serial clock I/O
  Transmission mode, reception mode, and transmission/reception mode specifiable

16.3 Operation

16.3.1 Reset operation via $\overline{\text{RESET}}$ pin

When a low level is input to the $\overline{\text{RESET}}$ pin, the system is reset, and each hardware unit is initialized.

When the level of the $\overline{\text{RESET}}$ pin is changed from low to high, the reset status is released.

If the reset status is released by $\overline{\text{RESET}}$ pin input, the oscillation stabilization time of the oscillator elapses (reset value of OSTS register: $2^{16}/f_X$) and then the CPU starts program execution.

Table 16-2. Hardware Status on $\overline{\text{RESET}}$ Pin Input

Item	During Reset Period	After Reset Release
Oscillator (f_X)	Oscillation stops	Oscillation starts
Internal oscillator	Oscillation stops	Oscillation starts
Peripheral clock (f_X to $f_X/2,048$)	Operation stops	Operation starts after securing oscillation stabilization time
Internal system clock (f_{CLK}), CPU clock (f_{CPU})	Operation stops	Operation starts after securing oscillation stabilization time (initialized to $f_{XX}/8$)
CPU	Initialized	Program execution starts after securing oscillation stabilization time[Note 1]
Internal RAM	Undefined in case of power-on reset or if writing data to RAM (by CPU) and reset conflict (data is damaged). Otherwise value immediately after reset is retained[Note 2].	
I/O lines (ports/alternate-function pins)	High impedance	
On-chip peripheral I/O registers	Initialized to specified status	
Other on-chip peripheral functions	Operation stops	Operation can be started after securing oscillation stabilization time

Notes 1. With the μPD70F3714, program execution is delayed by insertion of internal processing for boot switching.

2. The firmware of the μPD70F3714 uses part of the internal RAM (used RAM area: 3FFE000H to 3FFE095H, 3FFEFBAH to 3FFEFFFH) after the internal system reset operation has been released because it supports a boot switching function. Therefore, the contents of some RAM areas are not retained on power-on reset.

16.3.3 Low-voltage detector (LVI)

(1) Functions

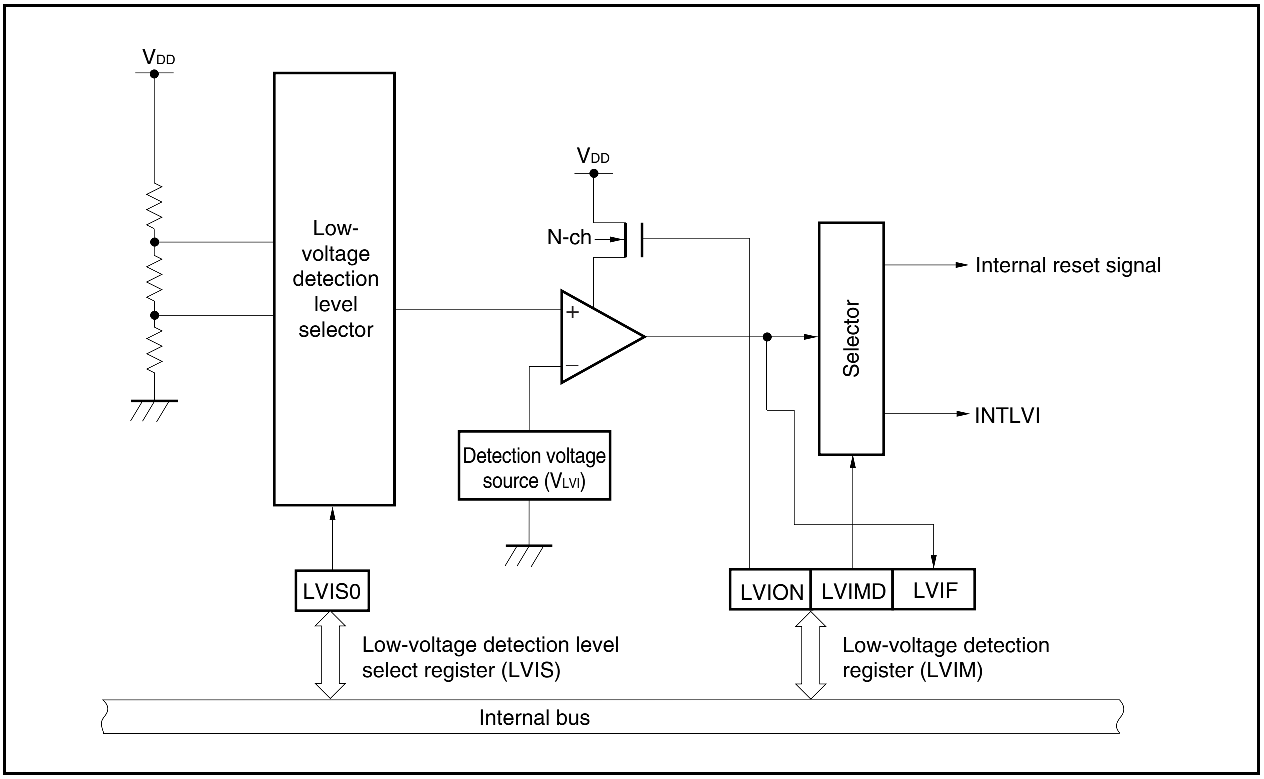
The low-voltage detector (LVI) has the following functions.

- Compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}) and generates an interrupt request signal or internal reset signal when $V_{DD} < V_{LVI}$.
- The level of the supply voltage to be detected can be changed in two steps.
- An interrupt request signal or internal reset signal can be selected.
- Can operate in HALT/IDLE/STOP mode.
- Operation can be stopped by software.

(2) Configuration

The block diagram is shown below.

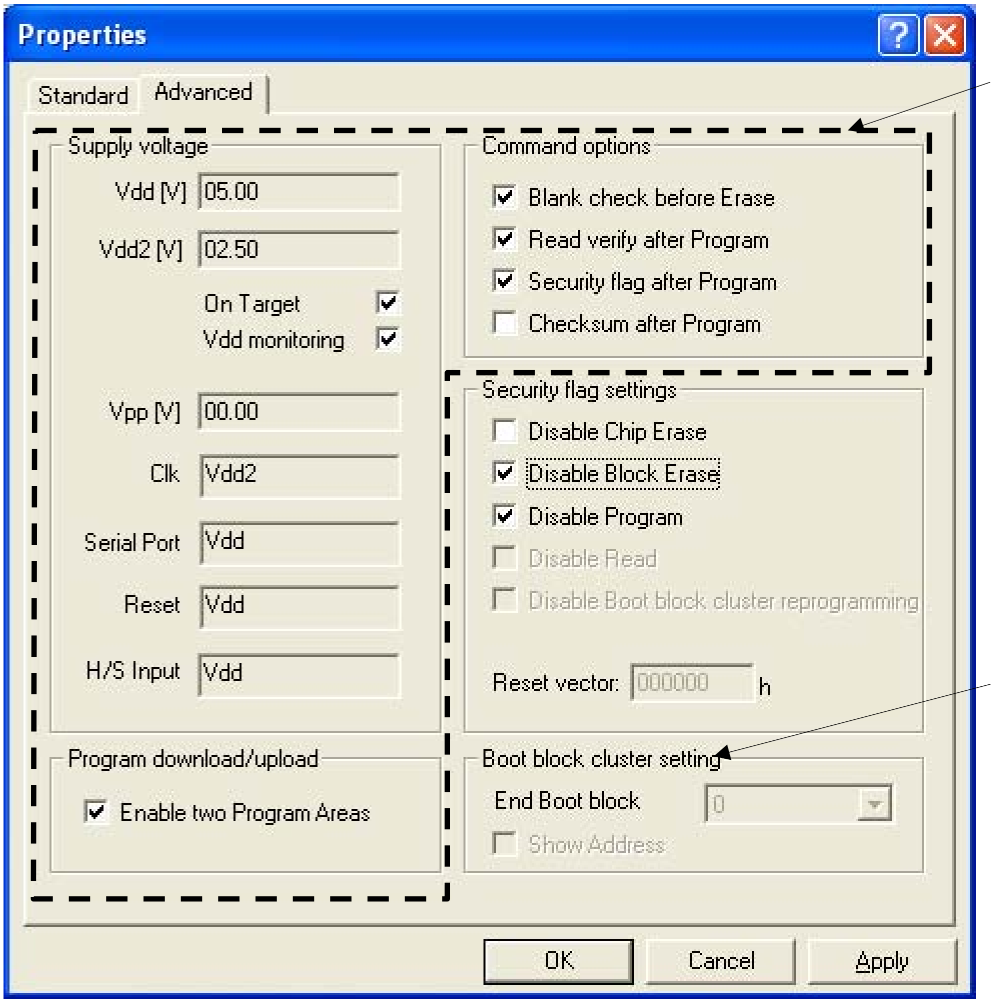
Figure 16-4. Block Diagram of Low-Voltage Detector


VDD
Low-voltage detection level selector
VDD
N-ch
+
–
Detection voltage source (VLVI)
Selector
Internal reset signal
INTLVI
LVIS0
LVION
LVIMD
LVIF
Low-voltage detection level select register (LVIS)
Low-voltage detection register (LVIM)
Internal bus

<R> **(1) Security setting by PG-FP4 and PG-FP5 (Security flag settings)**

When disabling the read command (Disable Read), to raise the security level, it is recommended to also disable the block erase command (Disable Block Erase) and program command (Disable Program).

Furthermore, when rewriting program is not necessary similarly to the mask ROM versions, additionally disable the chip erase command (Disable Chip Erase).



Note 1

Note 2

Properties

Supply voltage

Vdd [V] 05.00

Vdd2 [V] 02.50

On Target ☑

Vdd monitoring ☑

Vpp [V] 00.00

Clk Vdd2

Serial Port Vdd

Reset Vdd

H/S Input Vdd

Program download/upload

☑ Enable two Program Areas

Command options

☑ Blank check before Erase

☑ Read verify after Program

☑ Security flag after Program

☐ Checksum after Program

Security flag settings

☐ Disable Chip Erase

☑ Disable Block Erase

☑ Disable Program

☐ Disable Read

☐ Disable Boot block cluster reprogramming

Reset vector: 000000 h

Boot block cluster setting

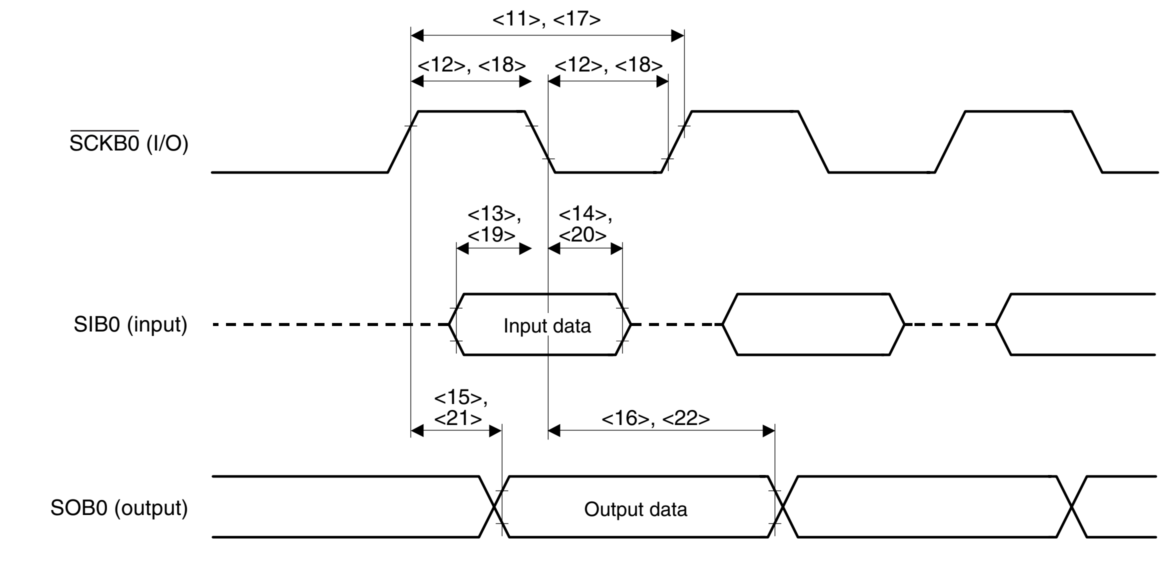
End Boot block 0

☐ Show Address

Notes 1. Set “Supply voltage”, “Program download/upload”, and “Command options” in broken lines in accordance with the use conditions.

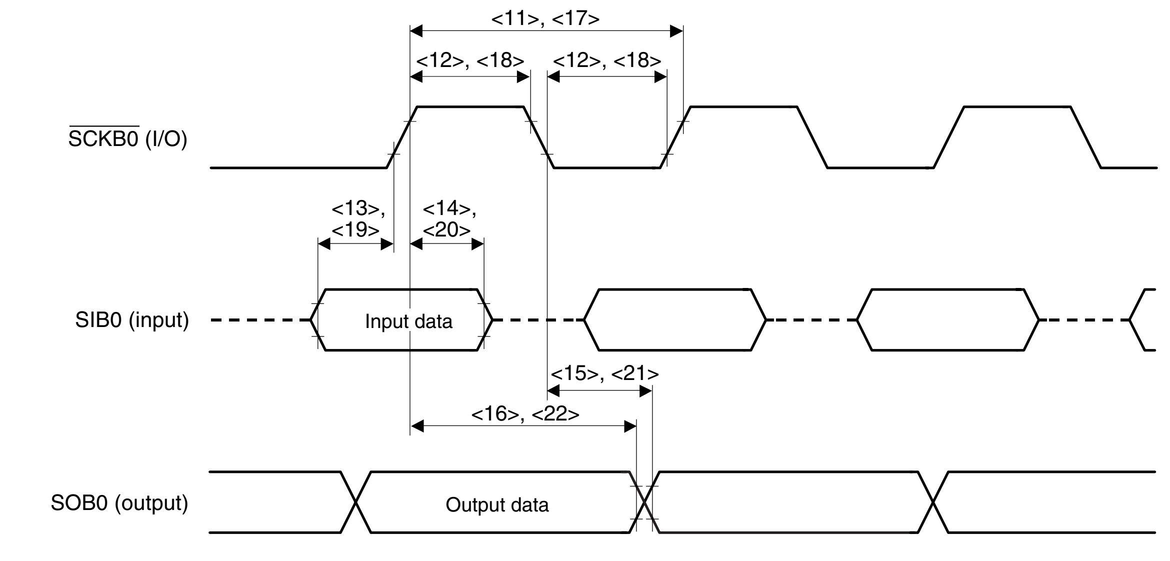
2. To disable rewriting the boot area (Boot block cluster setting), select “Disable Boot block cluster reprogramming” in “Security flag settings” and select the last block of the boot area for which rewriting is to be disabled.

CSIB Timing: CB0CTL1.CB0CKP, CB0CTL1.CB0DAP Bits = 10



Remark The broken lines indicate high impedance.

CSIB Timing: CB0CTL1.CB0CKP, CB0CTL1.CB0DAP Bits = 11



Remark The broken lines indicate high impedance.

(3/3)

Page	Description
p. 581	Addition of description to **15.2 (1) Power save control register (PSC)**
p. 587	Addition of description to **15.5.1 Setting and operation status**
p. 590	Addition of description to **16.2 (1) Reset source flag register (RESF)**
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