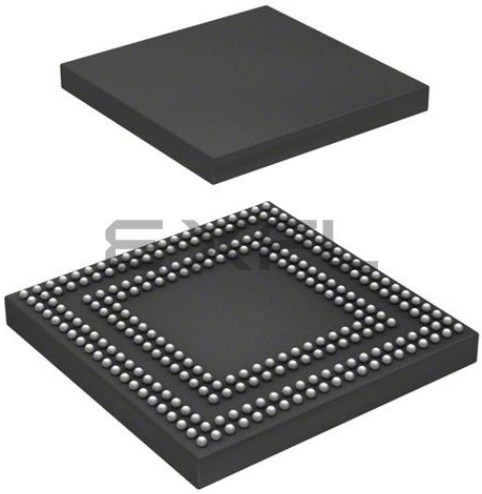
Renesas Electronics America Inc - R7S721010VCBG#AC0 Datasheet



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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DVD, VDC
Ethernet	10/100Mbps (1), 100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.2V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-LFBGA
Supplier Device Package	256-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s721010vcbg-ac0

(2) Non-port pins

(1/2)

Pin Name	Pin No.	I/O	Function	Alternate Function
ADTRG0	13	Input	External trigger input for A/D converters 0, 1	INTP4/P04
ADTRG1	12	Input		INTP5/P05
ANI00	1	Input	Analog input to A/D converters 0, 1	–
ANI01	2	Input		–
ANI02	3	Input		–
ANI03	4	Input		–
ANI10	58	Input		–
ANI11	57	Input		–
ANI12	56	Input		–
ANI13	55	Input		–
AV_{DD0}	63	–	Positive power supply for A/D converters 0, 1 (same potential as V_{DD})	–
AV_{DD1}	60	–		–
AV_{REF0}	64	–	Reference voltage input for A/D converters 0, 1 (same potential as AV_{DD0} and AV_{DD1})	–
AV_{REF1}	59	–		–
AV_{SS0}	62	–	Ground potential for A/D converters 0, 1 (same potential as V_{SS})	–
AV_{SS1}	61	–		–
EV_{DD}	26, 47	–	Positive power supply for external pin	–
EV_{SS}	27, 48	–	Ground potential for external pin	–
EVTQ0	20	Input	External event count input of TMQ0	TOQH03/P14
FLMD0	25	Input	Pin for setting flash memory programming mode	–
FLMD1	30	Input		PDL5
INTP0	17	Input	External maskable interrupt request input	TOQH0OFF/P00
INTP1	16			TOQ1OFF/P01
INTP2	15			TOP2OFF/P02
INTP3	14			TOP3OFF/P03
INTP4	13			ADTRG0/P04
INTP5	12			ADTRG1/P05
INTP6	11			P06
REGC	10	–	Regulator output stabilization capacitance connection	–
$\overline{\text{RESET}}$	5	Input	System reset input	–
RXDA0	44	Input	Serial receive data input of UARTA0, UARTA1	P30
RXDA1	42			P32
$\overline{\text{SCKB0}}$	38	I/O	Serial clock I/O of CSIB0	P42
SIB0	40	Input	Serial receive data input of CSIB0	P40
SOB0	39	Output	Serial transmit data output of CSIB0	P41

3.4.5 Recommended use of address space

The architecture of the V850ES/IE2 requires that a register that serves as a pointer be secured for address generation when operand data in the data space is accessed. The ±32 KB area of addresses stored in this pointer can be directly accessed by an instruction for operand data. Because the number of general-purpose registers that can be used as a pointer is limited, however, by keeping the performance from dropping during address calculation when a pointer value is changed, as many general-purpose registers as possible can be secured for variables, and the program size can be reduced.

(1) Program space

Of the 32 bits of the PC (program counter), the higher 6 bits are fixed to 0, and only the lower 26 bits are valid. Regarding the program space, therefore, a 64 MB space of contiguous addresses starting from 00000000H unconditionally corresponds to the memory map.

To use the internal RAM area as the program space, access addresses 3FFD800H to 3FFEFFFH (6 KB).

Caution When a branch instruction is positioned at the upper limit of the internal RAM area, a prefetch operation (invalid fetch) that will be located in the on-chip peripheral I/O area is not generated.

(2) Data space

With the V850ES/IE2 it seems that there are sixty-four 64 MB address spaces on the 4 GB CPU address space. Therefore, the least significant bit (bit 25) of a 26-bit address is sign-extended to 32 bits and allocated as an address.

The operating conditions of the PRERR flag are shown below. For the operating conditions of the PRERR2 flag, read PRCMD and SYS as PRCMD2 and SYS2 in the following explanation.

(i) Set condition (PRERR flag = 1)

- When data is written to a special register without writing anything to the PRCMD register (when <3> is executed without executing <2> in **3.4.7 (1) Setting data to special registers**)
- When data is written to an on-chip peripheral I/O register other than a special register (including execution of a bit manipulation instruction) after writing data to the PRCMD register (if <3> in **3.4.7 (1) Setting data to special registers** is not the setting of a special register)

Remark Even if an on-chip peripheral I/O register is read (excluding execution of a bit manipulation instruction) between a write access to the PRCMD register and a write access to a special register (such as an access to the internal RAM), the PRERR flag is not set and data can be written to the special register.

(ii) Clear condition (PRERR flag = 0)

- When 0 is written to the PRERR flag
- When the system is reset

Cautions 1. If 0 is written to the PRERR bit of the SYS register which is not a special register, immediately after a write access to the PRCMD register, the PRERR bit is cleared to 0 (the write access takes precedence).

2. If data is written to the PRCMD register, which is not a special register, immediately after a write access to the PRCMD register, the PRERR bit is set to 1.

4.3.4 Port 3

Port 3 can be set to the input or output mode in 1-bit units.

Port 3 has an alternate function as the following pins.

Table 4-7. Alternate-Function Pins of Port 3

Pin Name	Pin No.	Alternate-Function Pin	I/O	Pull-Up[Note 1]
P30[Note 2]	44	RXDA0	Input	Provided
P31	43	TXDA0	Output	
P32[Note 2]	42	RXDA1	Input	
P33	41	TXDA1	Output	

Notes 1. Software pull-up function

2. These pins operate as Schmitt trigger inputs when they are read in the port mode.

(1) Registers

(a) Port 3 register (P3)

After reset: Undefined R/W Address: FFFFF406H

	7	6	5	4	3	2	1	0
P3	0	0	0	0	P33	P32	P31	P30

P3n	Control of output data (in output mode) (n = 0 to 3)
0	Output 0.
1	Output 1.

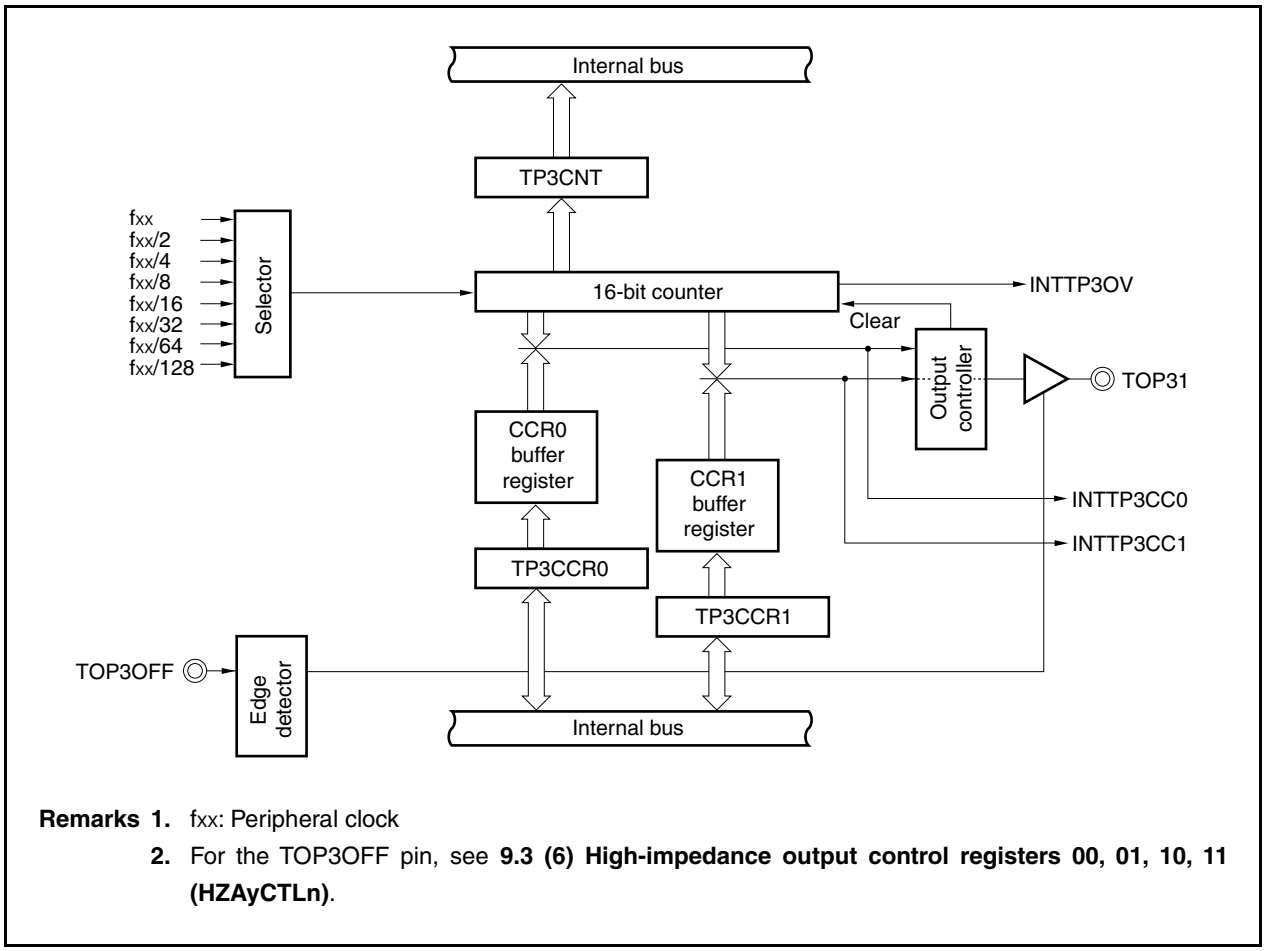
(b) Port 3 mode register (PM3)

After reset: FFH R/W Address: FFFFF426H

	7	6	5	4	3	2	1	0
PM3	1	1	1	1	PM33	PM32	PM31	PM30

PM3n	Control of input/output mode (in port mode) (n = 0 to 3)
0	Output mode
1	Input mode

Figure 6-4. TMP3 Block Diagram



Remarks 1. fxx: Peripheral clock

2. For the TOP3OFF pin, see **9.3 (6) High-impedance output control registers 00, 01, 10, 11 (HZAyCTLn)**.

(1) 16-bit counter

This 16-bit counter can count internal clocks or external events.

The count value of this counter can be read by using the TPnCNT register.

When the TPnCTL0.TPnCE bit = 0, the value of the 16-bit counter is FFFFH. If the TPnCNT register is read at this time, 0000H is read.

The TPnCE bit is cleared to 0 after reset.

(2) CCR0 buffer register

This is a 16-bit compare register that compares the count value of the 16-bit counter.

When the TPnCCR0 register is used as a compare register, the value written to the TPnCCR0 register is transferred to the CCR0 buffer register. When the count value of the 16-bit counter matches the value of the CCR0 buffer register, a compare match interrupt request signal (INTTPnCC0) is generated.

The CCR0 buffer register cannot be read or written directly.

The TPnCCR0 register is cleared to 0000H after reset, and the CCR0 buffer register is cleared to 0000H.

Figure 6-11. Register Setting for Interval Timer Mode Operation (3/3)

(g) TMPn capture/compare register 1 (TPnCCR1)

The TPnCCR1 register is not used in the interval timer mode. However, the set value of the TPnCCR1 register is transferred to the CCR1 buffer register. When the count value of the 16-bit counter matches the value of the CCR1 buffer register, the TOPm1 pin output is inverted and a compare match interrupt request signal (INTTPnCC1) is generated.

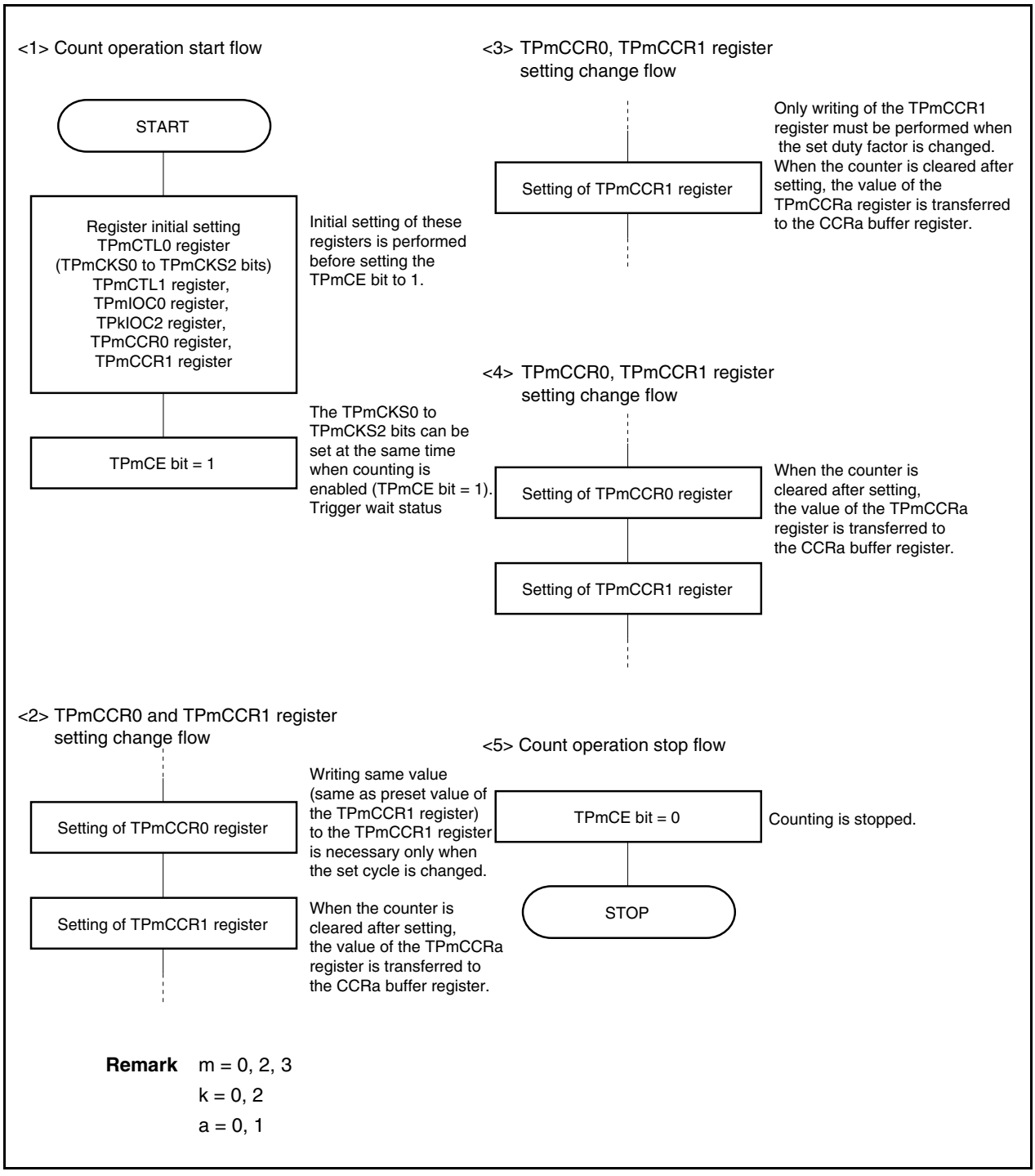
By setting this register to the same value as the value set in the TPmCCR0 register, a PWM waveform with a duty factor of 50% can be output from the TOPm1 pin.

When the TPnCCR1 register is not used, it is recommended to set its value to FFFFH. Also mask the register by the interrupt mask flag (TPnCCIC1.TPnCCMK1).

<R> **Remarks 1.** TMPk I/O control register 1 (TPkIOC1) and TMPn option register 0 (TPnOPT0) are not used in the interval timer mode.

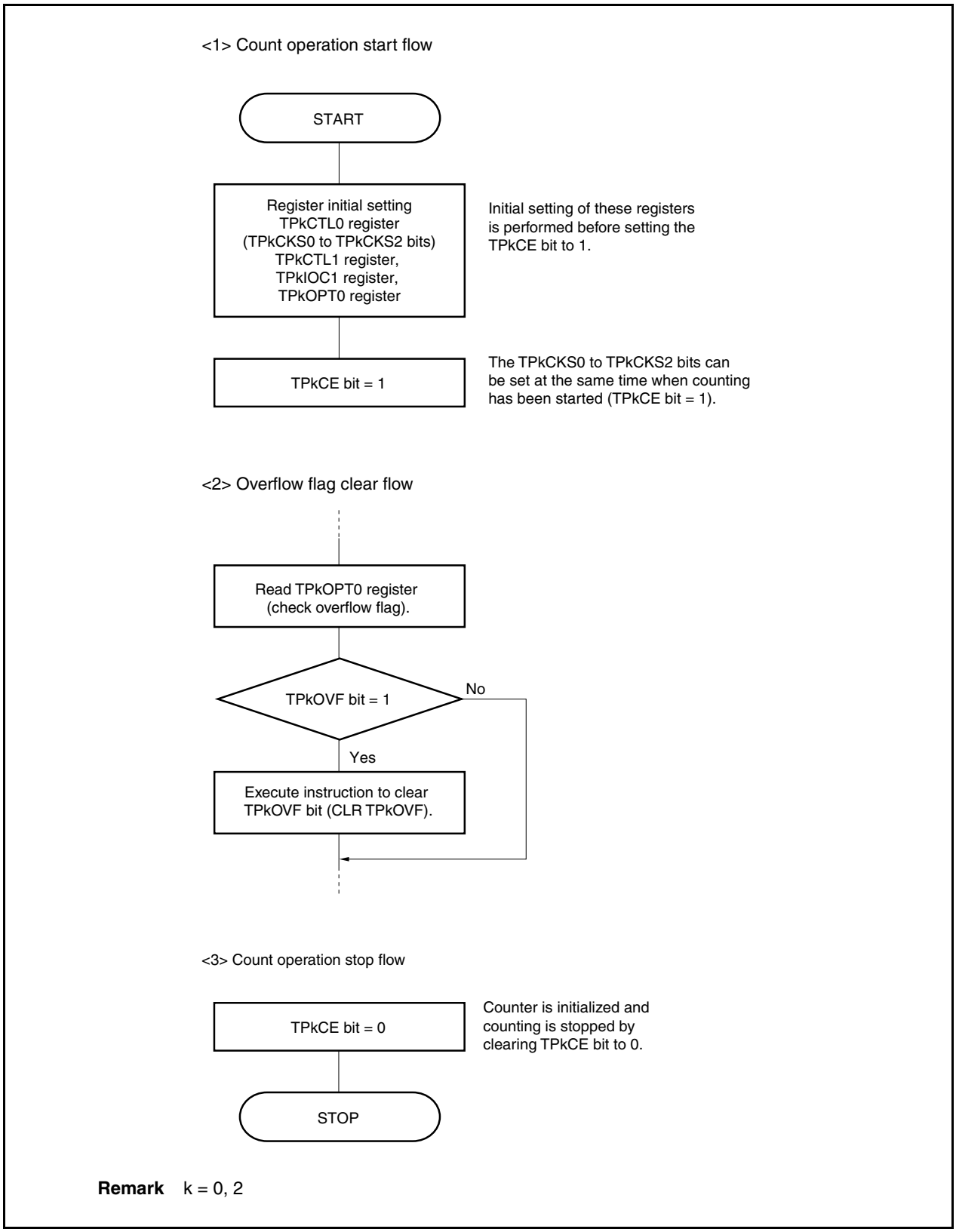
2. n = 0 to 3,
m = 0, 2, 3
k = 0, 2

Figure 6-26. Software Processing Flow in External Trigger Pulse Output Mode (2/2)



Remark m = 0, 2, 3
k = 0, 2
a = 0, 1

Figure 6-40. Software Processing Flow in Free-Running Timer Mode (Capture Function) (2/2)



Remark k = 0, 2

(9) TMQn capture/compare register 2 (TQnCCR2)

The TQ0CCR2 register is a 16-bit register that can be used as a capture register or a compare register depending on the mode. The TQ1CCR2 register is a 16-bit register that can only be used as a compare register.

The TQ0CCR2 register can be used as a capture register or a compare register only in the free-running timer mode, depending on the setting of the TQ0OPT0.TQ0CCS2 bit. In the pulse width measurement mode, the TQ0CCR2 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TQnCCR2 register can be read or written during operation.

This register can be read or written in 16-bit units.

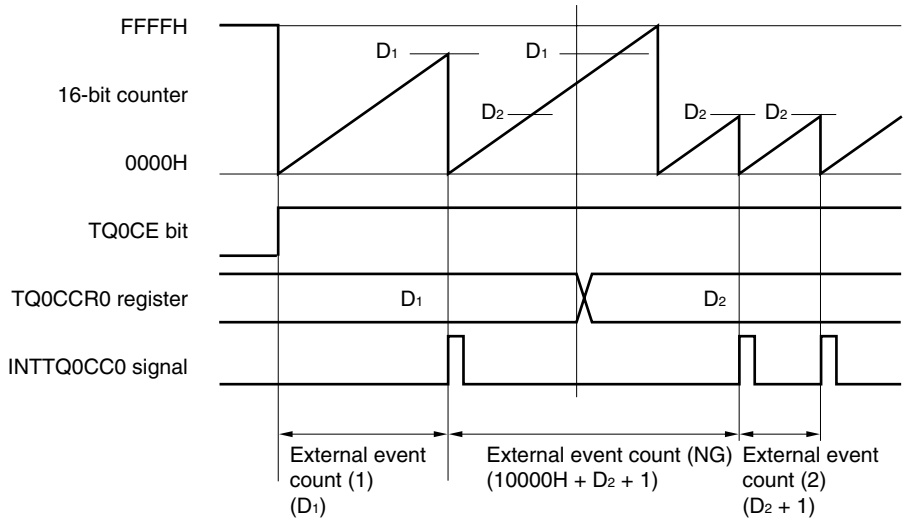
Reset sets this register to 0000H.

After reset: 0000H R/W Address: TQ0CCR2 FFFFF5CAH, TQ1CCR2 FFFFF60AH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TQnCCR2 (n = 0, 1)																

(b) Notes on rewriting the TQ0CCR0 register

If the value of the TQ0CCR0 register is rewritten to a smaller value during counting, the 16-bit counter may overflow. When the overflow may occur, stop counting once and then change the set value.



If the value of the TQ0CCR0 register is changed from D_1 to D_2 while the count value is greater than D_2 but less than D_1, the count value is transferred to the CCR0 buffer register as soon as the TQ0CCR0 register has been rewritten. Consequently, the value that is compared with the 16-bit counter is D_2.

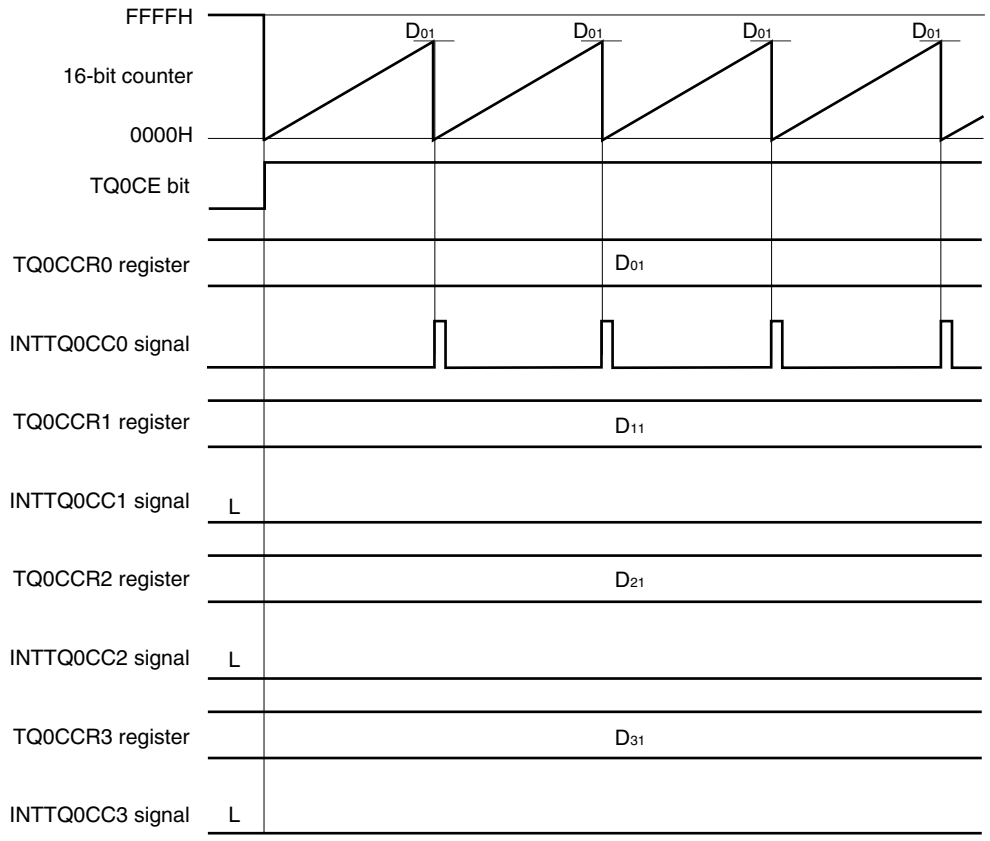
Because the count value has already exceeded D_2, however, the 16-bit counter counts up to FFFFH, overflows, and then counts up again from 0000H. When the count value matches D_2, the INTTQ0CC0 signal is generated.

Therefore, the INTTQ0CC0 signal may not be generated at the valid edge count of "(D_1 + 1) times" or "(D_2 + 1) times" originally expected, but may be generated at the valid edge count of "(10000H + D_2 + 1) times".

If the set value of the TQ0CCRb register is greater than the set value of the TQ0CCR0 register, the INTTQ0CCb signal is not generated because the count value of the 16-bit counter and the value of the TQ0CCRb register do not match.

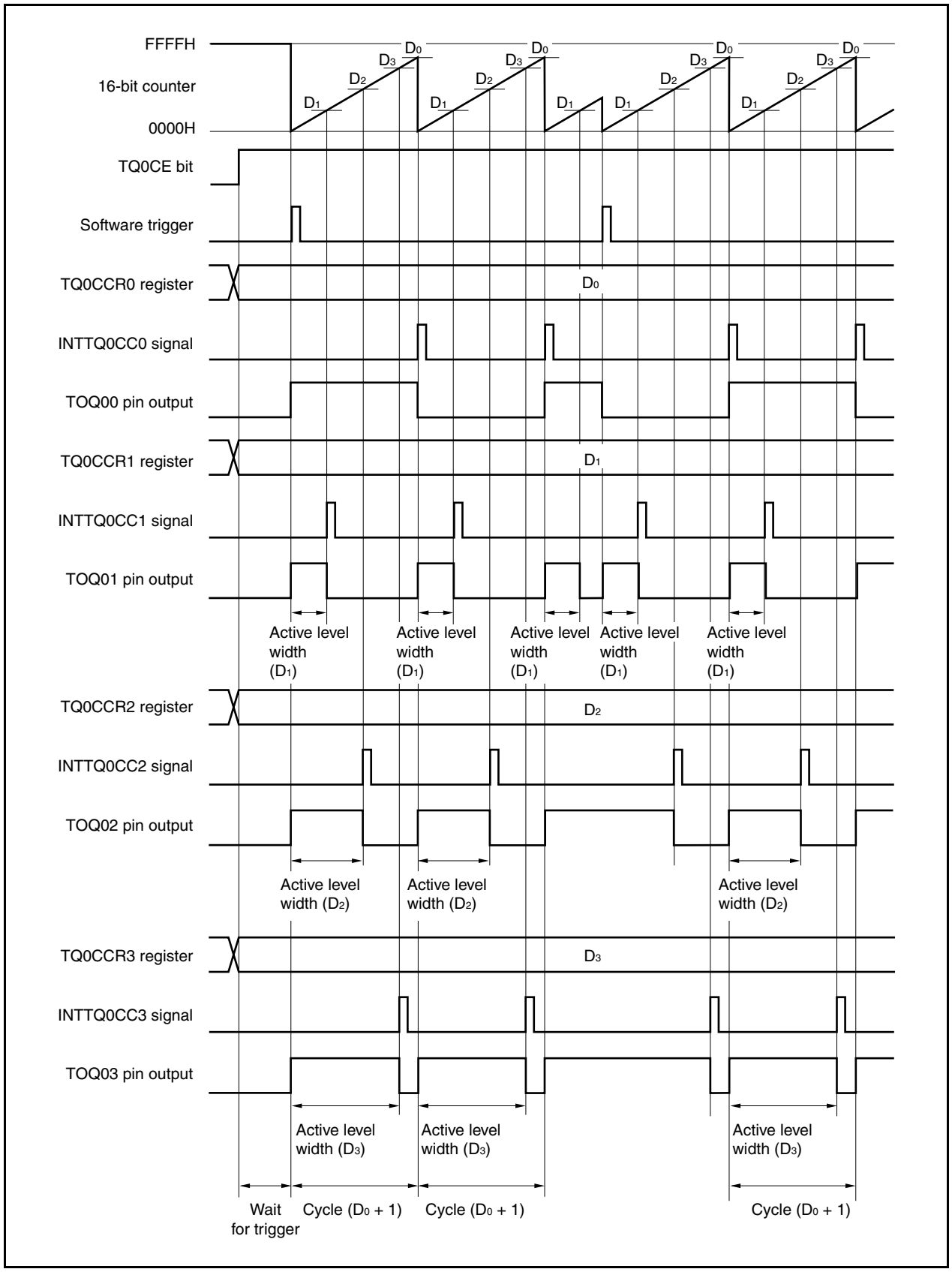
When the TQ0CCRb register is not used, it is recommended to set its value to FFFFH.

Figure 7-21. Timing Chart When $D_{01} < D_{b1}$

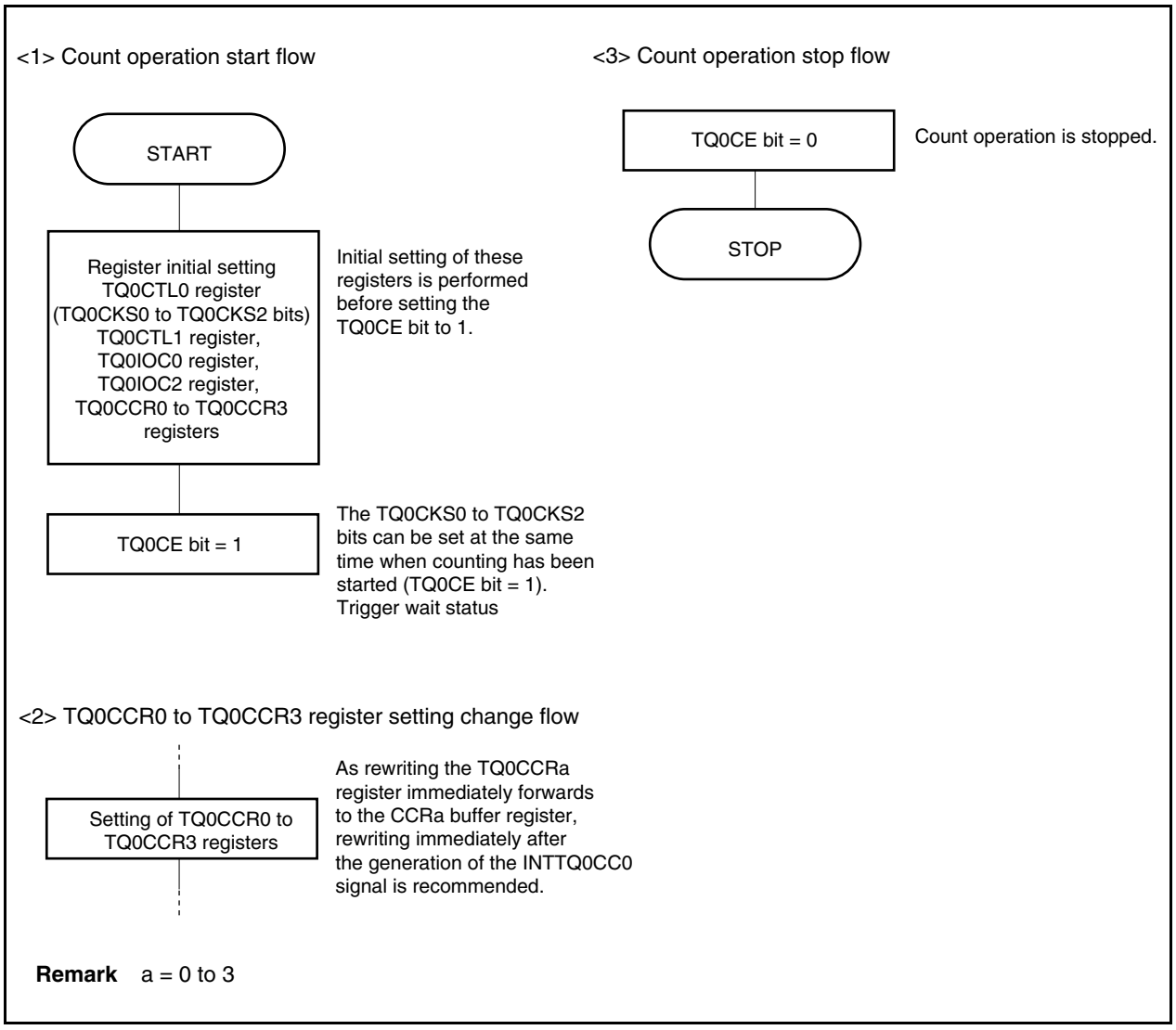


Remark b = 1 to 3

Figure 7-23. Basic Timing in External Trigger Pulse Output Mode

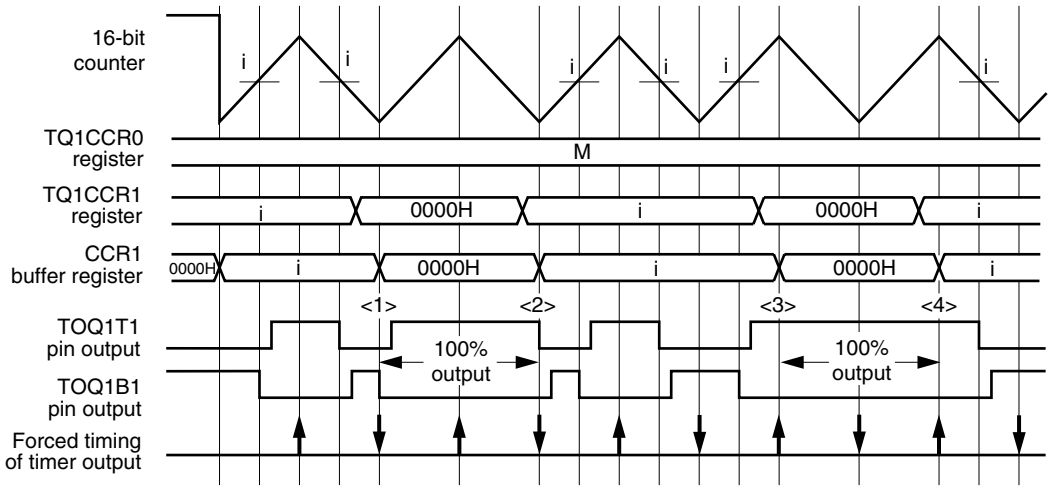


<R> **Figure 7-29. Software Processing Flow in One-Shot Pulse Output Mode (2/2)**



Remark a = 0 to 3

<R> **Figure 9-10. 100% PWM Output Waveform (with Dead Time)**



<1> 100% output is selected by the valley interrupt (with a match with the 16-bit counter).
The valley interrupt forcibly lowers the timer output, but raising the timer output takes precedence when the value of the TQ1CCRm register matches the value of the 16-bit counter. As a result, the 100% output is produced.

<2> 100% output is canceled by the valley interrupt (without a match with the 16-bit counter).
The valley interrupt forcibly lowers the timer output. This cancels the 100% output.

<3> 100% output is selected by the crest interrupt (without a match with the 16-bit counter).
The crest interrupt forcibly raises the timer output. This produces the 100% output.

<4> 100% output is canceled by the crest interrupt (without a match with the 16-bit counter).
The crest interrupt forcibly raises the timer output. This cancels the 100% output.

Remark ↑ means forced raising and ↓ means forced lowering.

(13) AV_{SS0} and AV_{SS1} pins

These pins are the ground pins of A/D converters 0 and 1. Always make the potential at the AV_{SSn} pin the same as that at the EV_{SS} pin even when A/D converters 0 and 1 are not used.

(14) AV_{DD0} and AV_{DD1} pins

These pins are the analog power supply pins of A/D converters 0 and 1.

Supply the same potential to the AV_{DD0} and AV_{DD1} pins.

Always make the potential at the AV_{DDn} pin the same as that at the EV_{DD} pin even when A/D converters 0 and 1 are not used.

The operating voltage range of the AV_{DDn} pin is $V_{DD} = EV_{DD} = AV_{REFn} = AV_{DDn} = 4.5$ to 5.5 V.

(15) Controller

This circuit executes control, such as enabling/disabling A/D converters 0 and 1 and selecting the operation mode and trigger mode.

11.3 Control Registers

A/D converters 0 and 1 are controlled by the following registers.

- A/D converter n mode registers 0 to 2 (ADAnM0 to ADAnM2)
- A/D converter n channel specification register (ADAnS)

The following registers are also used.

- A/Dn conversion result registers 0 to 3 (ADAnCR0 to ADAnCR3)
- A/Dn conversion result registers 0H to 3H (ADAnCR0H to ADAnCR3H)

(1) A/D converter n mode register 0 (ADAnM0)

The ADAnM0 register is an 8-bit register that specifies the operation mode and controls conversion operations.

This register can be read or written in 8-bit or 1-bit units. However, bit 0 is read-only. Writing executed to bit 0 is ignored.

Reset sets this register to 00H.

11.7 Operation in External Trigger Mode

In the external trigger mode, the analog input pins (ANIn0 to ANIn3) are A/D converted at the ADTRGn pin input timing.

The ADTRG0 pin has an alternate function as the P04/INTP4 pin and the ADTRG1 pin has an alternate function as the P05/INTP5 pin. To set the external trigger mode, set the PMC04 bit of port mode control register 0 (PMC0) to 1 and the ADA0M2.ADA0TMD1 bit to 0 with A/D converter 0. With A/D converter 1, set the PMC05 bit of port mode control register 0 (PMC0) to 1 and the ADA1M2.ADA1TMD1 bit to 0.

For the valid edge of the external input signal in the external trigger mode, the rising edge, falling edge, or both rising and falling edges can be specified by setting the ADAnM0.ADAnETS1 and ADAnM0.ADAnETS0 bits.

When the ADAnM0.ADAnCE bit is set (1), the A/D converter waits for a trigger and, when the trigger is input from the ADTRGn pin, starts A/D conversion.

After the end of A/D conversion, the conversion result is stored in A/Dn conversion result register m (ADAnCRm) and, at the same time, the A/Dn conversion end interrupt request signal (INTADn) is generated.

After the end of A/D conversion, the A/D converter waits for a trigger regardless of the operation mode set by the ADAnM0.ADAnMD1 and ADAnM0.ADAnMD0 bits.

When conversion is started, the ADAnM0.ADAnEF bit is set to 1 (conversion in progress). However, while the A/D converter is waiting for a trigger, the ADAnEF bit = 0 (conversion stopped).

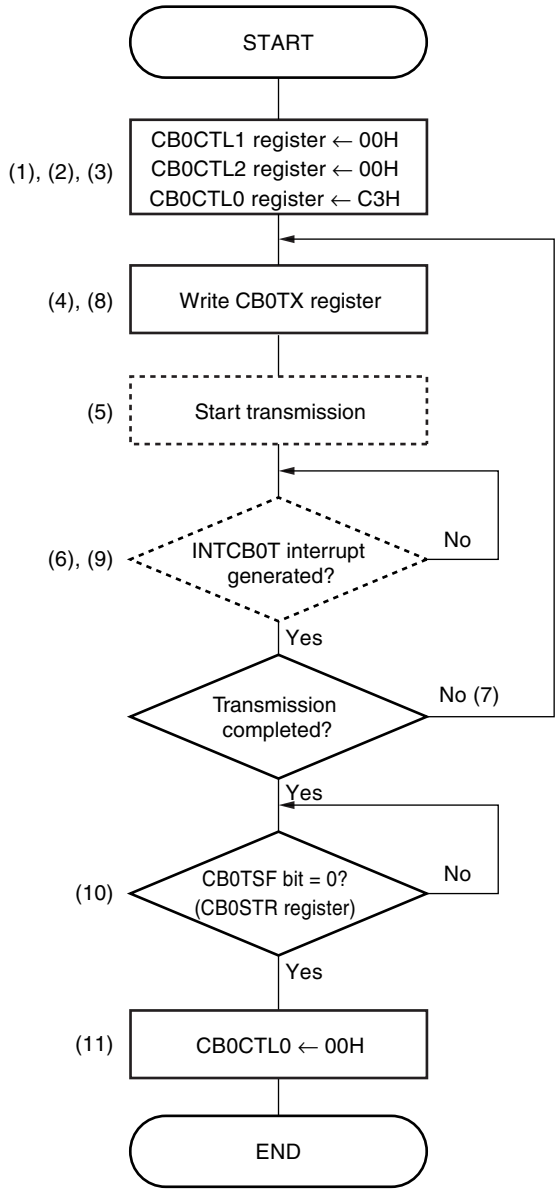
If a valid trigger is input during A/D conversion, the conversion operation is stopped and started again from the beginning. If the ADAnM0, ADAnM2, and ADAnS registers are written during A/D conversion, the conversion is stopped and the A/D converter waits for a trigger again.

Remark n = 0, 1
m = 0 to 3

13.4.7 Continuous transfer mode (master mode, transmission mode)

MSB first (CB0CTL0.CB0DIR bit = 0), communication type 1 (CB0CTL1.CB0CKP and CB0CTL1.CB0DAP bits = 00), communication clock (f_{CCLK}) = f_{XX}/2 (CB0CTL1.CB0CKS2 to CB0CTL1.CB0CKS0 bits = 000), transfer data length = 8 bits (CB0CTL2.CB0CL3 to CB0CTL2.CB0CL0 bits = 0000)

(1) Operation flow



Remarks 1. The broken lines indicate the hardware processing.

2. The numbers in this figure correspond to the processing numbers in **(2) Operation timing**.

(2) Generation of exception in servicing program

Servicing program of maskable interrupt or exception

... ... • EIPC saved to memory or register • EIPSW saved to memory or register ... • TRAP instruction ... • Saved value restored to EIPSW • Saved value restored to EIPC • RETI instruction	← Exception such as TRAP instruction acknowledged.

The priority order for multiple interrupt servicing control has 8 levels, from 0 to 7 for each maskable interrupt request signal (0 is the highest priority), but it can be set as desired via software. The priority order is set using the xxPRn0 to xxPRn2 bits of the interrupt control request register (xxICn), provided for each maskable interrupt request signal. After system reset, an interrupt request signal is masked by the xxMKn bit and the priority order is set to level 7 by the xxPRn0 to xxPRn2 bits.

The priority order of maskable interrupts is as follows.

(High) Level 0 > Level 1 > Level 2 > Level 3 > Level 4 > Level 5 > Level 6 > Level 7 (Low)

Interrupt servicing that has been suspended as a result of multiple servicing control is resumed after the servicing of the higher priority interrupt has been completed and the RETI instruction has been executed.
A pending interrupt request signal is acknowledged after the current interrupt servicing has been completed and the RETI instruction has been executed.

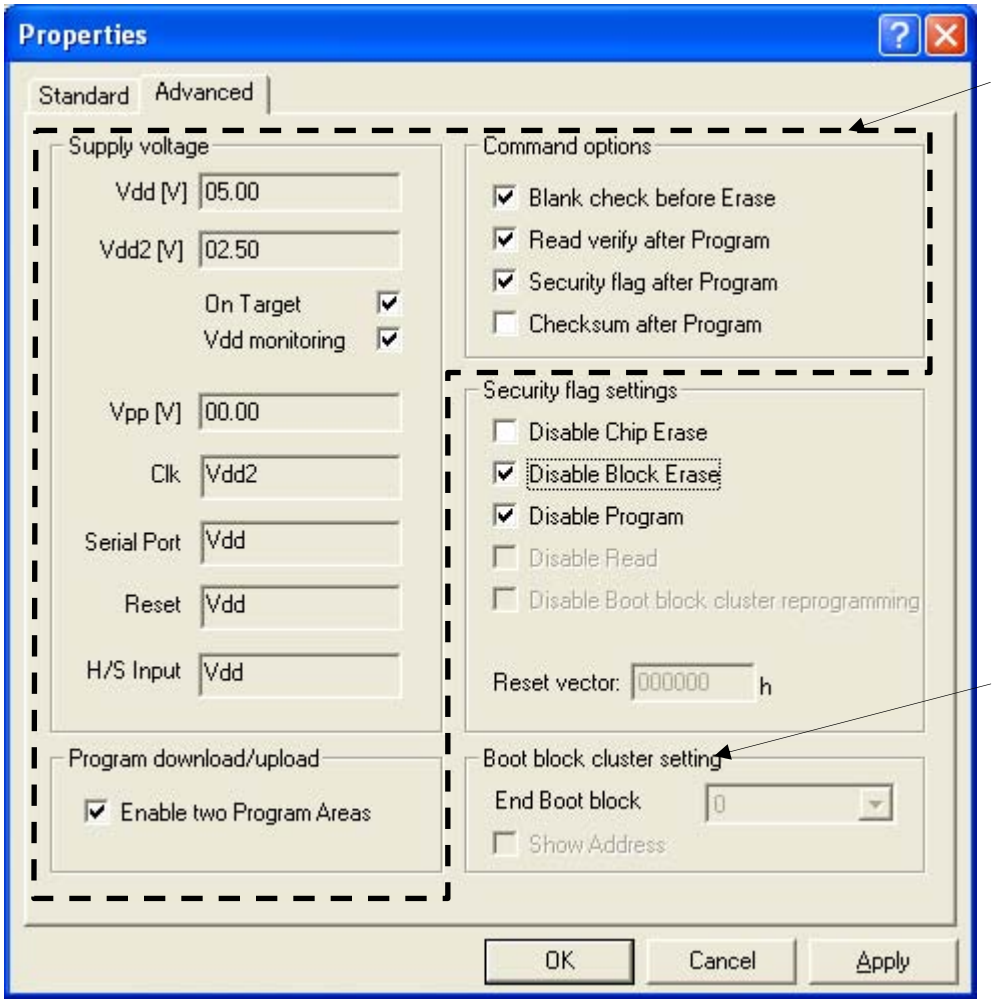
Caution In a non-maskable interrupt servicing routine (time until the RETI instruction is executed), maskable interrupts are suspended and not acknowledged.

Remark xx: Identification name of each peripheral unit (see **Table 14-2**)
n: Peripheral unit number (see **Table 14-2**)

<R> **(1) Security setting by PG-FP4 and PG-FP5 (Security flag settings)**

When disabling the read command (Disable Read), to raise the security level, it is recommended to also disable the block erase command (Disable Block Erase) and program command (Disable Program).

Furthermore, when rewriting program is not necessary similarly to the mask ROM versions, additionally disable the chip erase command (Disable Chip Erase).



Notes 1. Set “Supply voltage”, “Program download/upload”, and “Command options” in broken lines in accordance with the use conditions.

2. To disable rewriting the boot area (Boot block cluster setting), select “Disable Boot block cluster reprogramming” in “Security flag settings” and select the last block of the boot area for which rewriting is to be disabled.

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