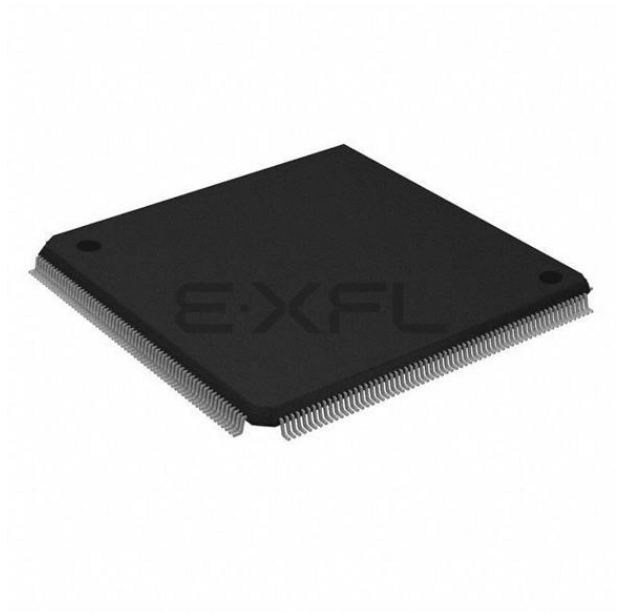
# Renesas Electronics America Inc - R7S721010VCFP#AA0 Datasheet



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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-A9 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | Multimedia; NEON™ MPE |
| RAM Controllers | SDRAM, SRAM |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | DVD, VDC |
| Ethernet | 10/100Mbps (1), 100Mbps (1) |
| SATA | - |
| USB | USB 2.0 (2) |
| Voltage - I/O | 1.2V, 3.3V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | - |
| Package / Case | 256-LQFP |
| Supplier Device Package | 256-LQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s721010vcfp-aa0 |

**(e) Pull-up resistor option register 3 (PU3)**

After reset: 00H R/W Address: FFFFFC46H

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PU3 | 0 | 0 | 0 | 0 | PU33 | PU32 | PU31 | PU30 |

| PU3n | Control of on-chip pull-up resistor connection (n = 0 to 3) |
|---|---|
| 0 | Do not connect |
| 1 | Connect[Note] |

**Note** An on-chip pull-up resistor can be connected only when the pins are in input mode in the port mode or when the pins function as input pins in the alternate-function mode. The resistor cannot be connected when the pin is in the output state.

### (2) TMPn control register 1 (TPnCTL1)

The TPnCTL1 register is an 8-bit register that controls the TMPn operation.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

(1/2)

After reset: 00H R/W Address: TP0CTL1 FFFFF641H, TP1CTL1 FFFFF661H, TP2CTL1 FFFFF681H, TP3CTL1 FFFFF6A1H

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TPnCTL1 | TP1SYE[Note 1] | TPmEST[Note 2] | TPkEEE[Note 3] | 0 | 0 | TPnMD2 | TPnMD1 | TPnMD0 |

(n = 0 to 3
m = 0, 2, 3
k = 0, 2)

| TP1SYE[Note 1] | Operation mode selection |
|---|---|
| 0 | TMP1 single mode |
| 1 | Tuning operation mode (see **9.4.5**) |
| TMP1 can be used only as an A/D conversion start trigger factor of A/D converters 0 and 1 during the tuning operation. In the tuning operation mode, this bit always operates in synchronization with TMQ1. | |

| TPmEST[Note 2] | Software trigger control |
|---|---|
| 0 | – |
| 1 | Generate a valid signal for external trigger input.<br>• In one-shot pulse output mode:<br>A one-shot pulse is output with writing 1 to the TPmEST bit as the trigger.<br>• In external trigger pulse output mode:<br>A PWM waveform is output with writing 1 to the TPmEST bit as the trigger. |
| Read value of the TPmEST bit is always 0. | |

| TPkEEE[Note 3] | Count clock selection |
|---|---|
| 0 | Disable operation with external event count input (TIPk0 pin).<br>(Perform counting with the count clock selected by the TPkCTL0.TPkCKS0 to TPkCTL0.TPkCKS2 bits.) |
| 1 | Enable operation with external event count input (TIPk0 pin)[Note 4].<br>(Perform counting at the valid edge of the external event count input signal.) |
| The TPkEEE bit selects whether counting is performed with the internal count clock or the valid edge of the external event count input. | |

**Notes 1.** This bit can only be set in TMP1. Be sure to clear bit 7 of TMP0, TMP2, and TMP3 to 0. For details of tuning operation mode, see **CHAPTER 9 MOTOR CONTROL FUNCTION**.

**2.** This bit can only be set in TMP0, TMP2, and TMP3. Be sure to clear bit 6 of TMP1 to 0.

**3.** This bit can only be set in TMP0 and TMP2. Be sure to clear bit 5 of TMP1 and TMP3 to 0.

**4.** Set the valid edge selection of capture trigger input (TIPk0 pin) to “No edge detection”.

**Figure 6-11. Register Setting for Interval Timer Mode Operation (3/3)**

**(g) TMPn capture/compare register 1 (TPnCCR1)**

The TPnCCR1 register is not used in the interval timer mode. However, the set value of the TPnCCR1 register is transferred to the CCR1 buffer register. When the count value of the 16-bit counter matches the value of the CCR1 buffer register, the TOPm1 pin output is inverted and a compare match interrupt request signal (INTTPnCC1) is generated.

By setting this register to the same value as the value set in the TPmCCR0 register, a PWM waveform with a duty factor of 50% can be output from the TOPm1 pin.

When the TPnCCR1 register is not used, it is recommended to set its value to FFFFH. Also mask the register by the interrupt mask flag (TPnCCIC1.TPnCCMK1).

<R> **Remarks 1.** TMPk I/O control register 1 (TPkIOC1) and TMPn option register 0 (TPnOPT0) are not used in the interval timer mode.

**2.** n = 0 to 3,
m = 0, 2, 3
k = 0, 2

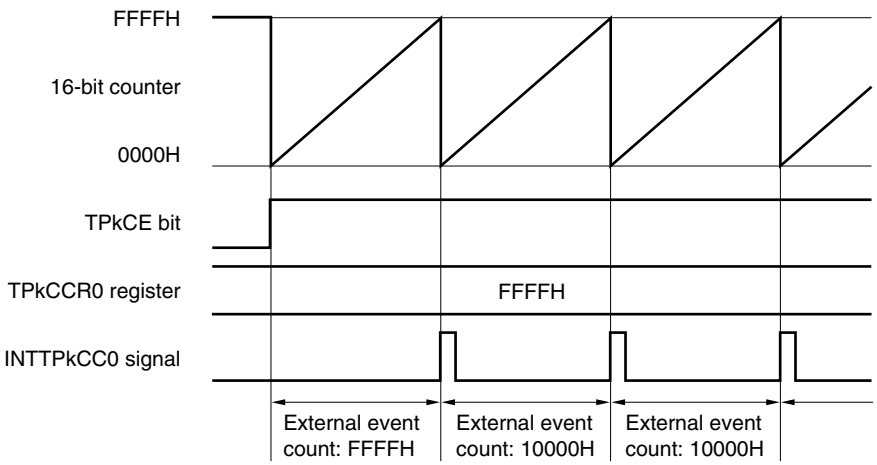
### (2) Operation timing in external event count mode

**Cautions 1. In the external event count mode, the TPkCCR0 and TPkCCR1 registers must not be cleared to 0000H.**

<R> **2. In the external event count mode, use of the timer output (TOP00, TOPk1) is disabled. If using timer output (TOPk1) with external event count input (TIPk0), set the interval timer mode, and enable the count clock operation with the external event count input (TPkCTL1.TPkEEE bit = 1) (see 6.6.1 (3) Operation by external event count input (TIPk0)).**

#### (a) Operation if TPkCCR0 register is set to FFFFH

If the TPkCCR0 register is set to FFFFH, the 16-bit counter counts to FFFFH each time the valid edge of the external event count signal has been detected. The 16-bit counter is cleared to 0000H in synchronization with the next count-up timing, and the INTTPkCC0 signal is generated. At this time, the TPkOPT0.TPkOVF bit is not set.

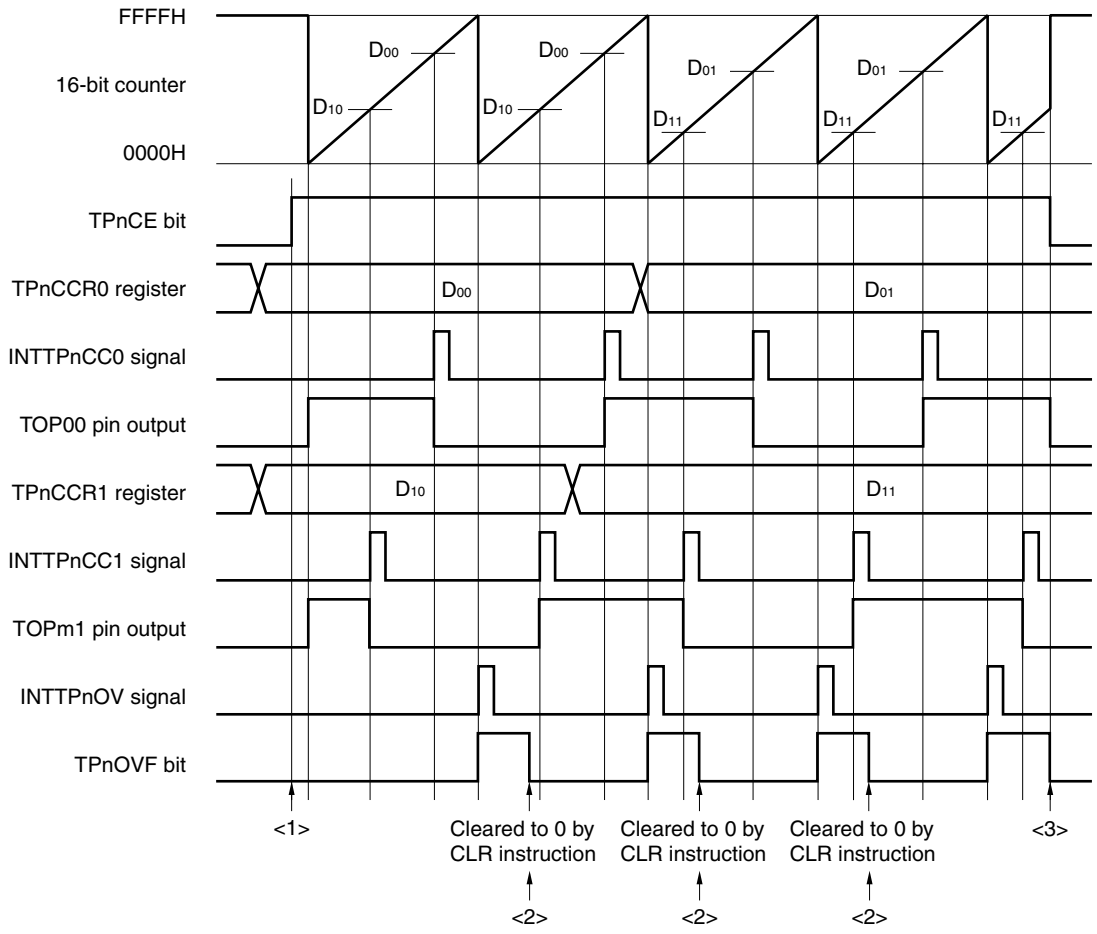



**Remark** k = 0, 2

### (1) Operation flow in free-running timer mode

#### (a) When using capture/compare register as compare register

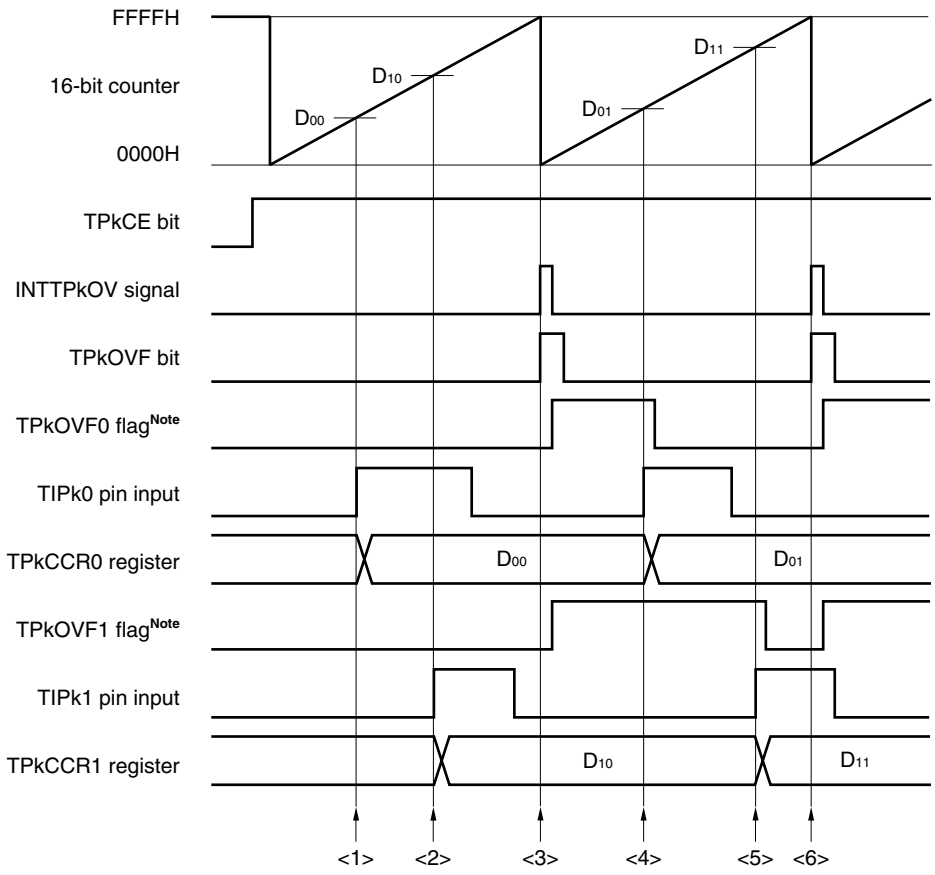
**Figure 6-39. Software Processing Flow in Free-Running Timer Mode (Compare Function) (1/2)**




**Remark** n = 0 to 3
m = 0, 2, 3

(1/2)

**Example when two capture registers are used (using overflow interrupt)**

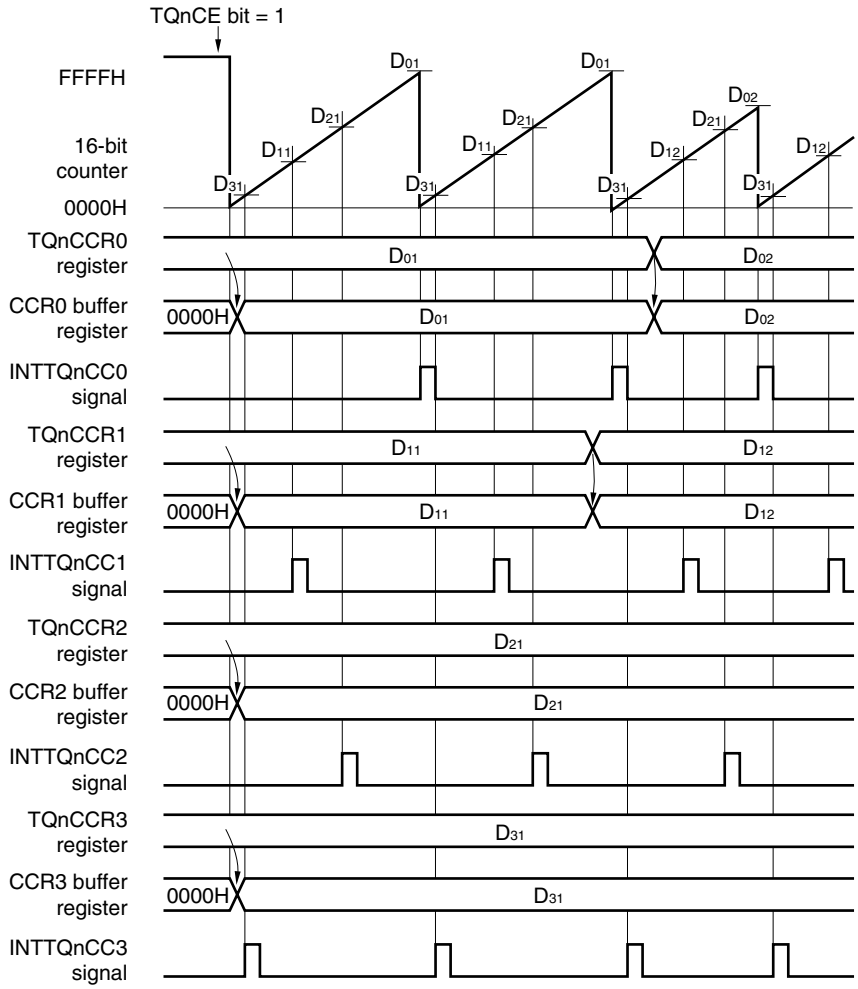



**Note** The TPkOVF0 and TPkOVF1 flags are set on the internal RAM by software.

<1> Read the TPkCCR0 register (setting of the default value of the TIk0 pin input).
<2> Read the TPkCCR1 register (setting of the default value of the TIPk1 pin input).
<3> An overflow occurs. Set the TPkOVF0 and TPkOVF1 flags to 1 in the overflow interrupt servicing, and clear the overflow flag to 0.
<4> Read the TPkCCR0 register.
Read the TPkOVF0 flag. If the TPkOVF0 flag is 1, clear it to 0.
Because the TPkOVF0 flag is 1, the pulse width can be calculated by (10000H + $D_{01} - D_{00}$).
<5> Read the TPkCCR1 register.
Read the TPkOVF1 flag. If the TPkOVF1 flag is 1, clear it to 0 (the TPkOVF0 flag is cleared in <4>, and the TPkOVF1 flag remains 1).
Because the TPkOVF1 flag is 1, the pulse width can be calculated by (10000H + $D_{11} - D_{10}$) (correct).
<6> Same as <3>

**Remark** k = 0, 2

**Figure 7-5. Timing of Anytime Write**




**Remarks 1.** $D_{01}$, $D_{02}$: Setting values of TQnCCR0 register

$D_{11}$, $D_{12}$: Setting values of TQnCCR1 register

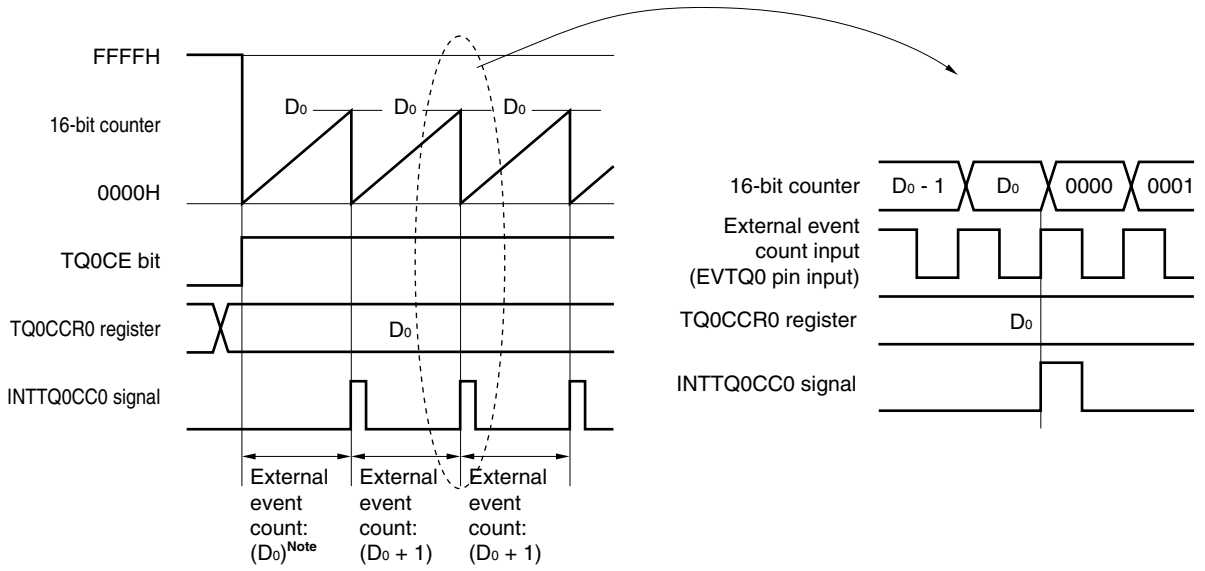
$D_{21}$: Setting value of TQnCCR2 register

$D_{31}$: Setting value of TQnCCR3 register

**2.** The above timing chart illustrates an example of the operation in the interval timer mode.

**3.** n = 0, 1

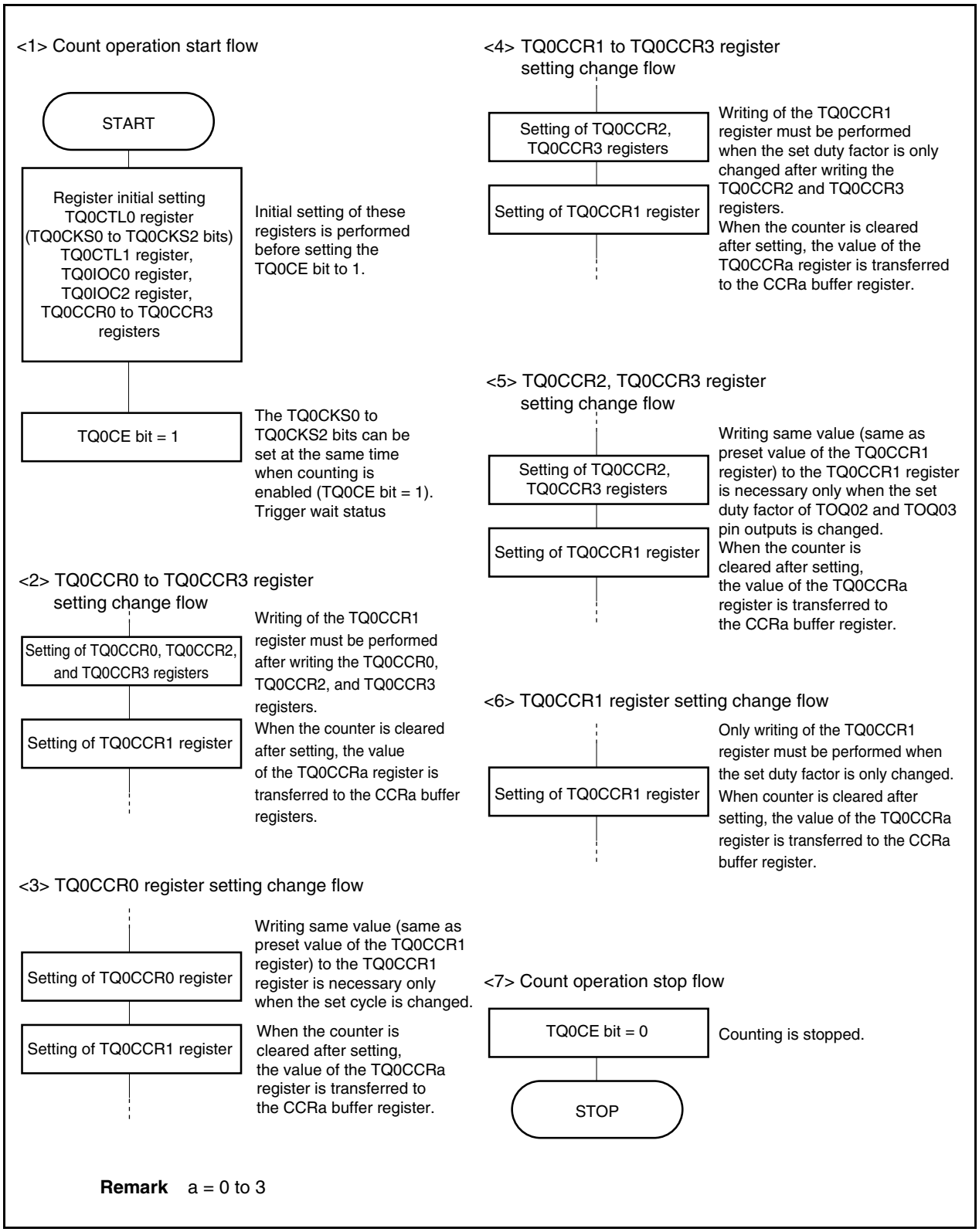
**Figure 7-16. Basic Timing in External Event Count Mode**




**Note** In the external event count mode, when the TQ0CTL0.TQ0CE bit is set to 1 (operation starts), the 16-bit counter is cleared from FFFFH to 0000H at the same time. The first count operation starts from 0001H every time the valid edge of the external event count input is detected. Therefore, the count of the first count operation is one number smaller than the count of second or subsequent count operation.

**Remark** This figure shows the basic timing when the rising edge is specified as the valid edge of the external event count input.

**Figure 7-25. Software Processing Flow in External Trigger Pulse Output Mode (2/2)**




**Remark** a = 0 to 3

## 8.3 Control Register

**(1) TMM0 control register 0 (TM0CTL0)**

The TM0CTL0 register is an 8-bit register that controls the TMM0 operation.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

The same value can always be written to the TM0CTL0 register by software.

After reset: 00H R/W Address: FFFFF540H

| | <7> | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TM0CTL0 | TM0CE | 0 | 0 | 0 | 0 | TM0CKS2 | TM0CKS1 | TM0CKS0 |

| TM0CE | Internal clock operation enable/disable specification |
|---|---|
| 0 | TMM0 operation disabled (16-bit counter reset asynchronously) |
| 1 | TMM0 operation enabled. Start operation clock supply. Start TMM0 operation. |
| The internal clock control and internal circuit reset for TMM0 are performed asynchronously with the TM0CE bit. When the TM0CE bit is cleared to 0, the internal clock of TMM0 is stopped (fixed to low level) and 16-bit counter is reset asynchronously. | |

| TM0CKS2 | TM0CKS1 | TM0CKS0 | Count clock selection |
|---|---|---|---|
| 0 | 0 | 0 | $f_{XX}$ |
| 0 | 0 | 1 | $f_{XX}/2$ |
| 0 | 1 | 0 | $f_{XX}/4$ |
| 0 | 1 | 1 | $f_{XX}/8$ |
| 1 | 0 | 0 | $f_{XX}/16$ |
| 1 | 0 | 1 | $f_{XX}/32$ |
| 1 | 1 | 0 | $f_{XX}/64$ |
| 1 | 1 | 1 | $f_{XX}/128$ |

**Cautions 1. Set the TM0CKS2 to TM0CKS0 bits when the TM0CE bit = 0. However, when changing the value of TM0CE from 0 to 1, it is impossible to set the value of the TM0CKS2 to TM0CKS0 bits simultaneously.**

**2. Be sure to clear bits 3 to 6 to "0".**

**Remark** $f_{XX}$: Peripheral clock frequency

(2/2)

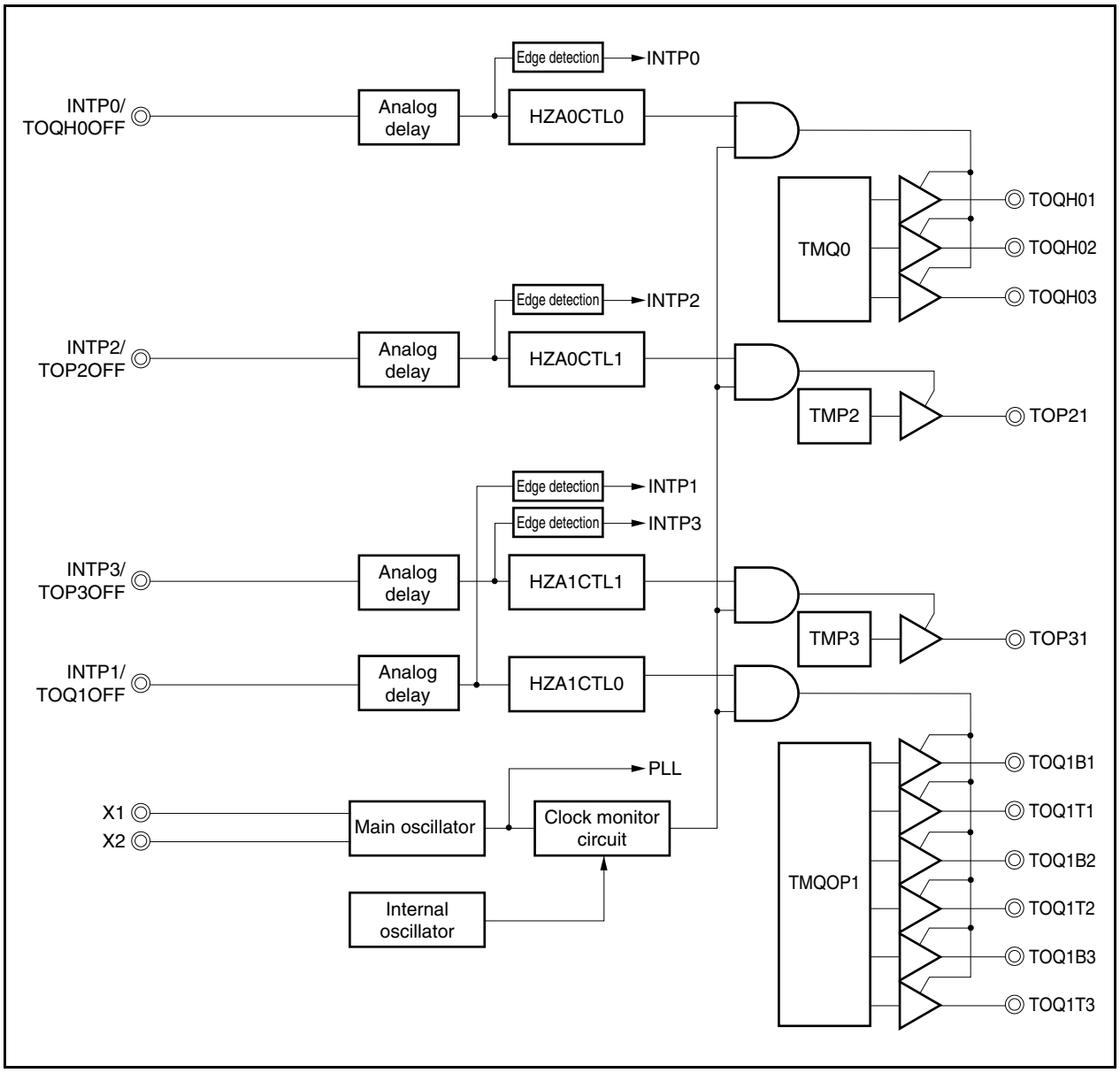
| HZAyDCCn | High-impedance output control clear bit |
|---|---|
| 0 | No operation |
| 1 | Pins that have gone into a high-impedance state are output-enabled by software and the HZAyDCFn bit is cleared to 0. |

- Pins can function as output pins when the HZAyDCM bit = 0, regardless of the status of the external pin[Note].
- If an edge indicating abnormality is input to the external pin[Note] (which is set by the HZAyDCNn and HZAyDCPn bits) when the HZAyDCM bit = 1, the HZAyDCCn bit is invalid even if it is set to 1.
- The HZAyDCCn bit is always 0 when it is read.
- The HZAyDCCn bit is invalid even if it is set to 1 when the HZAyDCEn bit = 0.
- Simultaneously setting the HZAyDCTn and HZAyDCCn bits to 1 is prohibited.

| HZAyDCFn | High-impedance output status flag |
|---|---|
| 0 | Indicates that output of the pin is enabled.<br>• This bit is cleared to 0 when the HZAyDCEn bit = 0.<br>• This bit is cleared to 0 when the HZAyDCCn bit = 1. |
| 1 | Indicates that the pin goes into a high-impedance state.<br>• This bit is set to 1 when the HZAyDCTn bit = 1.<br>• This bit is set to 1 when an edge indicating abnormality is input to the external pin[Note] (which is detected according to the setting of the HZAyDCNn and HZAyDCPn bits). |

**Note** HZA0CTL0: TOQH0OFF pin, HZA0CTL1: TOP2OFF pin, HZA1CTL0: TOQ1OFF pin, HZA1CTL1: TOP3OFF pin

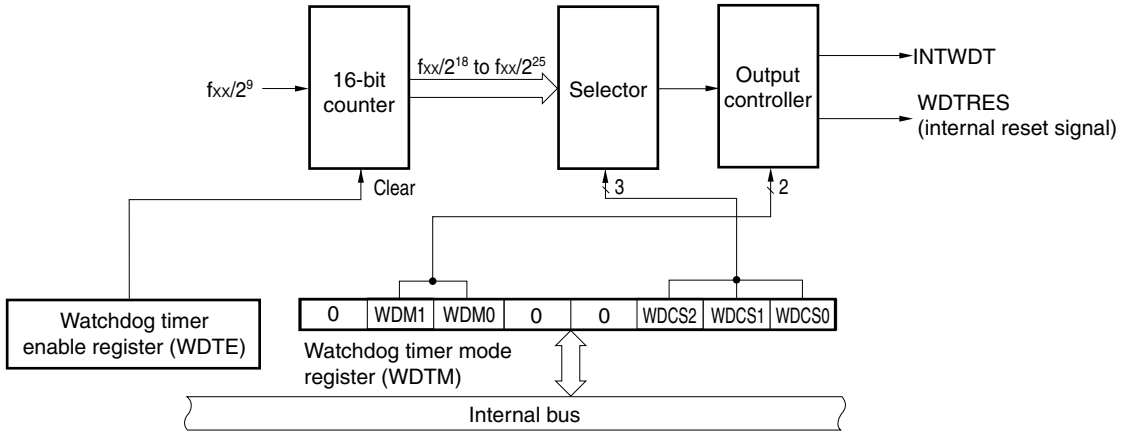
**Figure 9-4. High-Impedance Output Controller Configuration**



## 10.2 Configuration

The block diagram of the watchdog timer is shown below.

**Figure 10-1. Block Diagram of Watchdog Timer**




**Remark** $f_{XX}/2^9$: Watchdog timer clock
$f_{XX}$: Peripheral clock
INTWDT: Non-maskable interrupt request signal upon overflow of watchdog timer
WDTRES: Reset signal upon overflow of watchdog timer

The watchdog timer includes the following hardware.

**Table 10-1. Configuration of Watchdog Timer**

| Item | Configuration |
|---|---|
| Control registers | Watchdog timer mode register (WDTM)<br>Watchdog timer enable register (WDTE) |

# CHAPTER 11 A/D CONVERTERS 0 AND 1

## 11.1 Features

- Two 10-bit resolution A/D converter circuits (A/D converters 0 and 1)
  Simultaneous sampling of two circuits possible
- Analog input
  Two circuits, total of eight channels
  A/D converter 0: ANI00 to ANI03 (4 channels)
  A/D converter 1: ANI10 to ANI13 (4 channels)
- A/D conversion result registers 0m and 1m (ADA0CRm and ADA1CRm)
  10 bits × 4 × 2
- A/D conversion trigger mode
  - Software trigger mode
  - Hardware trigger mode
    External trigger mode
    Timer trigger mode
- A/D conversion operation mode
  Continuous select mode
  Continuous scan mode
  One-shot select mode
  One-shot scan mode
- Buffer mode
  1-buffer mode
  4-buffer mode
- Successive approximation method
- Operating voltage range
  $V_{DD} = EV_{DD} = AV_{DDn} = AV_{REFn}$ = 4.5 to 5.5 V

**Remark** m = 0 to 3
n = 0, 1

**(2) UARTAn control register 1 (UAnCTL1)**

The UAnCTL1 register is an 8-bit register that selects the UARTAn base clock.

This register can be read or written in 8-bit units.

Reset sets this register to 00H.

**Caution Clear the UAnCTL0.UAnPWR bit to 0 before rewriting the UAnCTL1 register.**

After reset: 00H R/W Address: UA0CTL1 FFFFFA01H, UA1CTL1 FFFFFA11H

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| UAnCTL1 (n = 0, 1) | 0 | 0 | 0 | 0 | UAnCKS3 | UAnCKS2 | UAnCKS1 | UAnCKS0 |

| UAnCKS3 | UAnCKS2 | UAnCKS1 | UAnCKS0 | Base clock ($f_{UCLK}$) selection |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | fxx |
| 0 | 0 | 0 | 1 | fxx/2 |
| 0 | 0 | 1 | 0 | fxx/4 |
| 0 | 0 | 1 | 1 | fxx/8 |
| 0 | 1 | 0 | 0 | fxx/16 |
| 0 | 1 | 0 | 1 | fxx/32 |
| 0 | 1 | 1 | 0 | fxx/64 |
| 0 | 1 | 1 | 1 | fxx/128 |
| 1 | 0 | 0 | 0 | fxx/256 |
| 1 | 0 | 0 | 1 | fxx/512 |
| 1 | 0 | 1 | 0 | fxx/1,024 |
| 1 | 0 | 1 | 1 | fxx/2,048 |
| Other than above | | | | Setting prohibited |

**Remark** fxx: Peripheral clock frequency

### 14.3.7 Maskable interrupt status flag (ID)

The ID flag controls the maskable interrupt's operating state, and stores control information regarding enabling or disabling of interrupt requests. The ID flag is allocated to the PSW.

This flag is set to 00000020H after reset.

After reset: 00000020H

| | 31 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| PSW | 0 | | NP | EP | ID | SAT | CY | OV | S | Z |

| ID | Maskable interrupt servicing specification[Note] |
|---|---|
| 0 | Maskable interrupt request signal acknowledgment enabled |
| 1 | Maskable interrupt request signal acknowledgment disabled (pending) |

**Note** Interrupt disable flag (ID) function

ID is set (1) by the DI instruction and cleared (0) by the EI instruction. Its value is also modified by the RETI instruction or LDSR instruction when referencing the PSW.

Non-maskable interrupt signals and exceptions are acknowledged regardless of this flag. When a maskable interrupt signal is acknowledged, the ID flag is automatically set (1) by hardware.

An interrupt request signal generated during the acknowledgment disabled period (ID flag = 1) can be acknowledged when the xxICn.xxIFn bit is set (1), and the ID flag is cleared (0).

**(2) Restore**

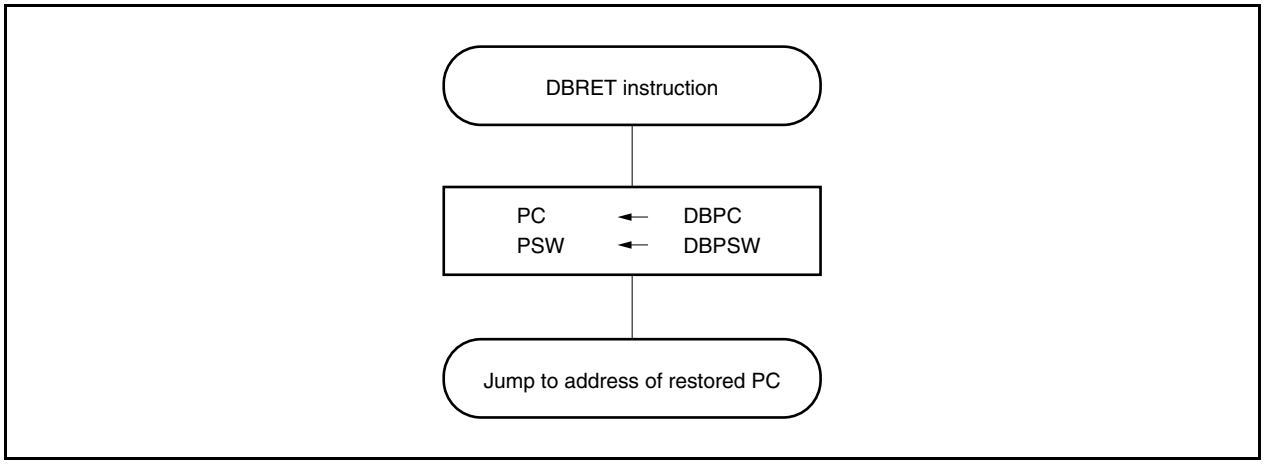
Recovery from a debug trap is carried out by the DBRET instruction. By executing the DBRET instruction, the CPU carries out the following processing and controls the address of the restored PC.

<1> Loads the restored PC and PSW from DBPC and DBPSW.
<2> Transfers control to the address indicated by the restored PC and PSW.

**Caution DBPC and DBPSW can be accessed during the period between when the DBTRAP is executed and when the DBRET instruction is executed.**

The restore processing from a debug trap is shown below.

**Figure 14-12. Restore Processing from Debug Trap**



**Characteristics of A/D Converters 0, 1**

**($T_A$ = –40 to +85°C, $V_{DD}$ = $EV_{DD}$ = 4.5 to 5.5 V, $AV_{DD0}$ = $AV_{DD1}$ = 4.5 to 5.5 V, $V_{SS}$ = $EV_{SS}$ = $AV_{SS0}$ = $AV_{SS1}$ = 0 V, $C_L$ = 50 pF)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | | | 10 | 10 | 10 | bit |
| Overall error[Note 1] | | | | | ±4.0 | LSB |
| Conversion time | $t_{CONV}$ | | 2 | | 10 | μs |
| Zero-scale error[Note 1] | | | | | ±4.0 | LSB |
| Full-scale error[Note 1] | | | | | ±4.0 | LSB |
| Integral linearity error[Note 1] | | | | | ±4.0 | LSB |
| Differential linearity error[Note 1] | | | | | –1 to +2 | LSB |
| Analog reference voltage | $AV_{REF}$ | $AV_{REF0}$ = $AV_{REF1}$ = $AV_{DD0}$ = $AV_{DD1}$ | 4.5 | | 5.5 | V |
| Analog input voltage | $V_{IAN}$ | | $AV_{SS}$ | | $AV_{DD}$ | V |
| $AV_{DD0}$, $AV_{DD1}$ supply current[Note 2] | $AI_{DD}$ | During operation | | 6 | 10 | mA |
| <R> | $AI_{DDS}$ | In STOP mode[Note 3] | | 0.5 | 25 | μA |

**Notes 1.** Excluding quantization error (±0.5 LSB).

**2.** This value is one cycle of A/D converter 0 or A/D converter 1.

**3.** Stop the operation of A/D converters 0 and 1 (ADAnM0.ADAnCE bit = 0) before setting to the STOP mode.

**Remarks 1.** LSB: Least Significant Bit

**2.** n = 0, 1

<R>

# CHAPTER 21 RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.
For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

**Table 21-1. Surface Mounting Type Soldering Conditions**

$\mu$PD70F3713GC-8BS-A: 64-pin plastic LQFP (14 × 14)
$\mu$PD70F3714GC-8BS-A: 64-pin plastic LQFP (14 × 14)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 to 72 hours) | IR60-203-3 |
| Wave soldering | For details, contact an NEC Electronics sales representative. | – |
| Partial heating | Pin temperature: 350°C max., Time: 3 seconds max. (per pin row) | – |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Remarks 1.** Products with -A at the end of the part number are lead-free products.

**2.** For soldering methods and conditions other than those recommended above, please contact an NEC Electronics sales representative.

# APPENDIX B REGISTER INDEX

(1/5)

| Symbol | Name | Unit | Page |
|---|---|---|---|
| AD0IC | Interrupt control register | INTC | 559 |
| AD1IC | Interrupt control register | INTC | 559 |
| ADA0CR0 | A/D0 conversion result register 0 | ADC0 | 436 |
| ADA0CR0H | A/D0 conversion result register 0H | ADC0 | 436 |
| ADA0CR1 | A/D0 conversion result register 1 | ADC0 | 436 |
| ADA0CR1H | A/D0 conversion result register 1H | ADC0 | 436 |
| ADA0CR2 | A/D0 conversion result register 2 | ADC0 | 436 |
| ADA0CR2H | A/D0 conversion result register 2H | ADC0 | 436 |
| ADA0CR3 | A/D0 conversion result register 3 | ADC0 | 436 |
| ADA0CR3H | A/D0 conversion result register 3H | ADC0 | 436 |
| ADA0M0 | A/D converter 0 mode register 0 | ADC0 | 431 |
| ADA0M1 | A/D converter 0 mode register 1 | ADC0 | 433 |
| ADA0M2 | A/D converter 0 mode register 2 | ADC0 | 435 |
| ADA0S | A/D converter 0 channel specification register | ADC0 | 434 |
| ADA1CR0 | A/D1 conversion result register 0 | ADC1 | 436 |
| ADA1CR0H | A/D1 conversion result register 0H | ADC1 | 436 |
| ADA1CR1 | A/D1 conversion result register 1 | ADC1 | 436 |
| ADA1CR1H | A/D1 conversion result register 1H | ADC1 | 436 |
| ADA1CR2 | A/D1 conversion result register 2 | ADC1 | 436 |
| ADA1CR2H | A/D1 conversion result register 2H | ADC1 | 436 |
| ADA1CR3 | A/D1 conversion result register 3 | ADC1 | 436 |
| ADA1CR3H | A/D1 conversion result register 3H | ADC1 | 436 |
| ADA1M0 | A/D converter 1 mode register 0 | ADC1 | 431 |
| ADA1M1 | A/D converter 1 mode register 1 | ADC1 | 433 |
| ADA1M2 | A/D converter 1 mode register 2 | ADC1 | 435 |
| ADA1S | A/D converter 1 channel specification register | ADC1 | 434 |
| CB0CTL0 | CSIB0 control register 0 | CSIB0 | 503 |
| CB0CTL1 | CSIB0 control register 1 | CSIB0 | 506 |
| CB0CTL2 | CSIB0 control register 2 | CSIB0 | 507 |
| CB0REIC | Interrupt control register | INTC | 559 |
| CB0RIC | Interrupt control register | INTC | 559 |
| CB0RX | CSIB0 receive data register | CSIB0 | 502 |
| CB0RXL | CSIB0 receive data register L | CSIB0 | 502 |
| CB0STR | CSIB0 status register | CSIB0 | 509 |
| CB0TIC | Interrupt control register | INTC | 559 |
| CB0TX | CSIB0 transmit data register | CSIB0 | 502 |
| CB0TXL | CSIB0 transmit data register L | CSIB0 | 502 |
| CKC | Clock control register | CG | 125 |
| CLM | Clock monitor mode register | CG | 129 |
| HZA0CTL0 | High-impedance output control register 00 | Timer | 372 |
| HZA0CTL1 | High-impedance output control register 01 | Timer | 372 |