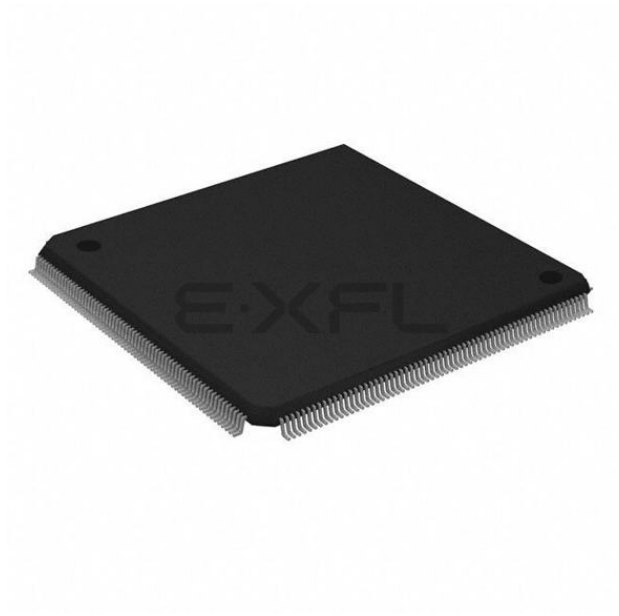
Renesas Electronics America Inc - R7S721010VLFP#AA0 Datasheet



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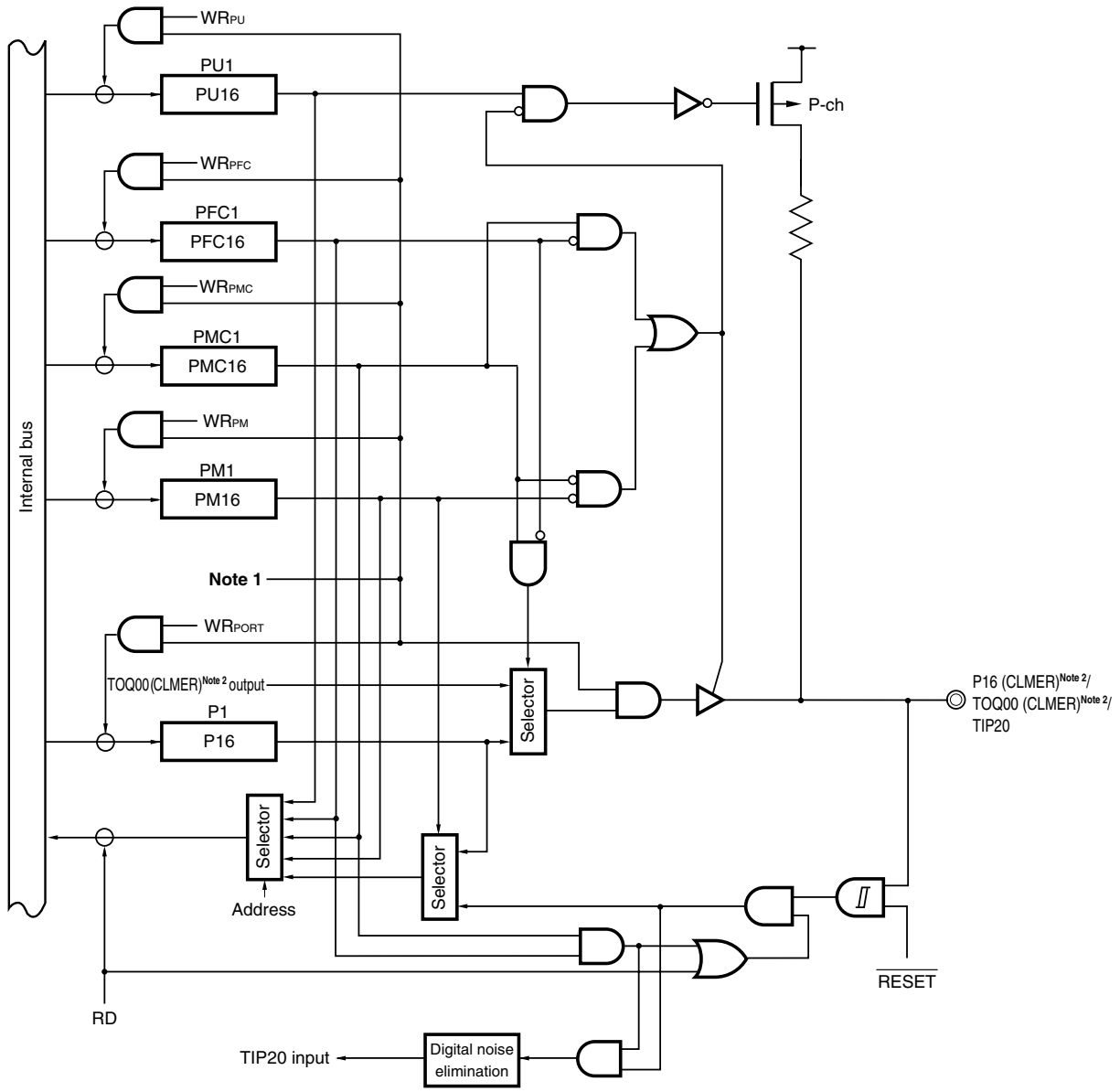
Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DVD, VDC
Ethernet	10/100Mbps (1), 100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.2V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-LQFP
Supplier Device Package	256-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s721010vlfp-aa0

Figure 4-9. Block Diagram of P16 Pin



Notes 1. Output of clock stop detection signal from clock monitor

2. When P16 is set as the output port or TOQ00 output function, if an error (oscillator stop) is detected by the clock monitor, the CLMER signal (low level) is output from P16. Low-level output is released by reset signal. For details, see **Table 4-5 Alternate-Function Pins of Port 1**.

Table 4-11. Using Port Pin as Alternate-Function Pin (2/3)

Pin Name	Alternate Pin		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCEnx Bit of PFCEn Register	PFCnx Bit of PFCn Register	Other Bit (Register)
	Name	I/O						
P16 (CLMER)[Note]	TOQ00 (CLMER)[Note]	Output	P16 = Setting not required	PM16 = Setting not required	PMC16 = 1	–	PFC16 = 0	
	TIP20	Input	P16 = Setting not required	PM16 = Setting not required	PMC16 = 1	–	PFC16 = 1	
P17	TOP21	Output	P17 = Setting not required	PM17 = Setting not required	PMC17 = 1	–	PFC17 = 0	
	TIP21	Input	P17 = Setting not required	PM17 = Setting not required	PMC17 = 1	–	PFC17 = 1	
P20	TOQ1T1	Output	P20 = Setting not required	PM20 = Setting not required	PMC20 = 1	–	–	
P21	TOQ1B1	Output	P21 = Setting not required	PM21 = Setting not required	PMC21 = 1	–	–	
P22	TOQ1T2	Output	P22 = Setting not required	PM22 = Setting not required	PMC22 = 1	–	–	
P23	TOQ1B2	Output	P23 = Setting not required	PM23 = Setting not required	PMC23 = 1	–	–	
P24	TOQ1T3	Output	P24 = Setting not required	PM24 = Setting not required	PMC24 = 1	–	–	
P25	TOQ1B3	Output	P25 = Setting not required	PM25 = Setting not required	PMC25 = 1	–	–	
P26	TOQ10	Output	P26 = Setting not required	PM26 = Setting not required	PMC26 = 1	–	–	
P27	TOP31	Output	P27 = Setting not required	PM27 = Setting not required	PMC27 = 1	–	–	
P30	RXDA0	Input	P30 = Setting not required	PM30 = Setting not required	PMC30 = 1	–	–	
P31	TXDA0	Output	P31 = Setting not required	PM31 = Setting not required	PMC31 = 1	–	–	
P32	RXDA1	Input	P32 = Setting not required	PM32 = Setting not required	PMC32 = 1	–	PFC32 = 1	
P33	TXDA1	Output	P33 = Setting not required	PM33 = Setting not required	PMC33 = 1	–	PFC33 = 1	
P40	SIB0	Input	P40 = Setting not required	PM40 = Setting not required	PMC40 = 1	–	–	
P41	SOB0	Output	P41 = Setting not required	PM41 = Setting not required	PMC41 = 1	–	–	
P42	$\overline{\text{SCKB0}}$	I/O	P42 = Setting not required	PM42 = Setting not required	PMC42 = 1	–	–	

Note When P16 is set as the output port or TOQ00 output function, if an error (oscillator stop) is detected by the clock monitor, the CLMER signal (low level) is output from P16. Low-level output is released by reset signal. For details, see **Table 4-5 Alternate-Function Pins of Port 1**.

When the TPkCE bit is set to 1, the value of the 16-bit counter is cleared from FFFFH to 0000H. The counter counts each time the valid edge of external event count input is detected. Additionally, the set value of the TPkCCR0 register is transferred to the CCR0 buffer register.

When the count value of the 16-bit counter matches the value of the CCR0 buffer register, the 16-bit counter is cleared to 0000H, and a compare match interrupt request signal (INTTPkCC0) is generated.

The INTTPkCC0 signal is generated for the first time when the valid edge of the external event count input has been detected "value set to TPkCCR0 register" times. After that, the INTTPkCC0 signal is generated each time the valid edge of the external event count has been detected "value set to TPkCCR0 register + 1" times.

Figure 6-18. Register Setting for Operation in External Event Count Mode (1/2)

(a) TMPk control register 0 (TPkCTL0)

	TPkCE					TPkCKS2	TPkCKS1	TPkCKS0
TPkCTL0	0/1	0	0	0	0	0	0	0

0: Stop counting
1: Enable counting

(b) TMPk control register 1 (TPkCTL1)

		TPkEST	TPkEEE			TPkMD2	TPkMD1	TPkMD0
TPkCTL1	0	0	0	0	0	0	0	1

0, 0, 1:
External event count mode

(c) TMPk I/O control register 2 (TPkIOC2)

					TPkEES1	TPkEES0	TPkETS1	TPkETS0
TPkIOC2	0	0	0	0	0/1	0/1	0	0

Select valid edge
of external event
count input (TIPk0 pin)

(d) TMPk counter read buffer register (TPkCNT)

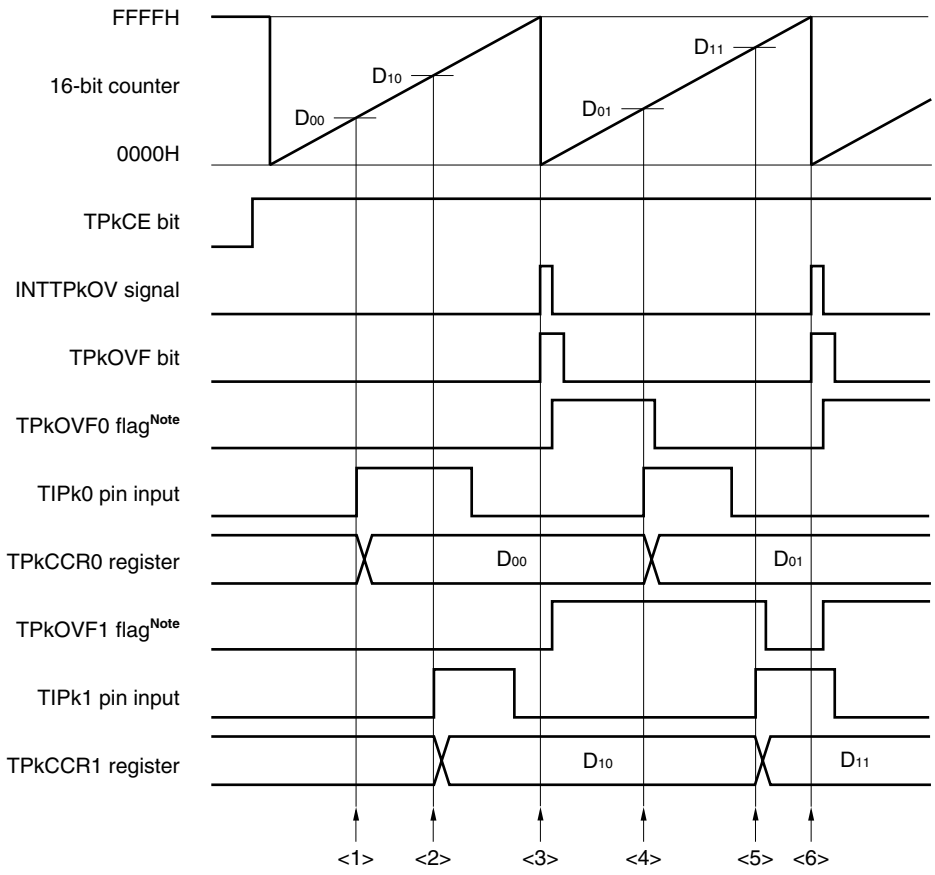
The count value of the 16-bit counter can be read by reading the TPkCNT register.

(e) TMPk capture/compare register 0 (TPkCCR0)

If the TPkCCR0 register is set to D_0, the count is cleared when the number of external event counts has reached (D_0) and the first compare match interrupt request signal (INTTPkCC0) is generated. The second compare match interrupt request signal (INTTPkCC0) is generated when the number of external event counts has reached (D_0 + 1).

(1/2)

Example when two capture registers are used (using overflow interrupt)



Note The TPkOVF0 and TPkOVF1 flags are set on the internal RAM by software.

<1> Read the TPkCCR0 register (setting of the default value of the TIk0 pin input).
<2> Read the TPkCCR1 register (setting of the default value of the TIPk1 pin input).
<3> An overflow occurs. Set the TPkOVF0 and TPkOVF1 flags to 1 in the overflow interrupt servicing, and clear the overflow flag to 0.
<4> Read the TPkCCR0 register.
Read the TPkOVF0 flag. If the TPkOVF0 flag is 1, clear it to 0.
Because the TPkOVF0 flag is 1, the pulse width can be calculated by (10000H + $D_{01} - D_{00}$).
<5> Read the TPkCCR1 register.
Read the TPkOVF1 flag. If the TPkOVF1 flag is 1, clear it to 0 (the TPkOVF0 flag is cleared in <4>, and the TPkOVF1 flag remains 1).
Because the TPkOVF1 flag is 1, the pulse width can be calculated by (10000H + $D_{11} - D_{10}$) (correct).
<6> Same as <3>

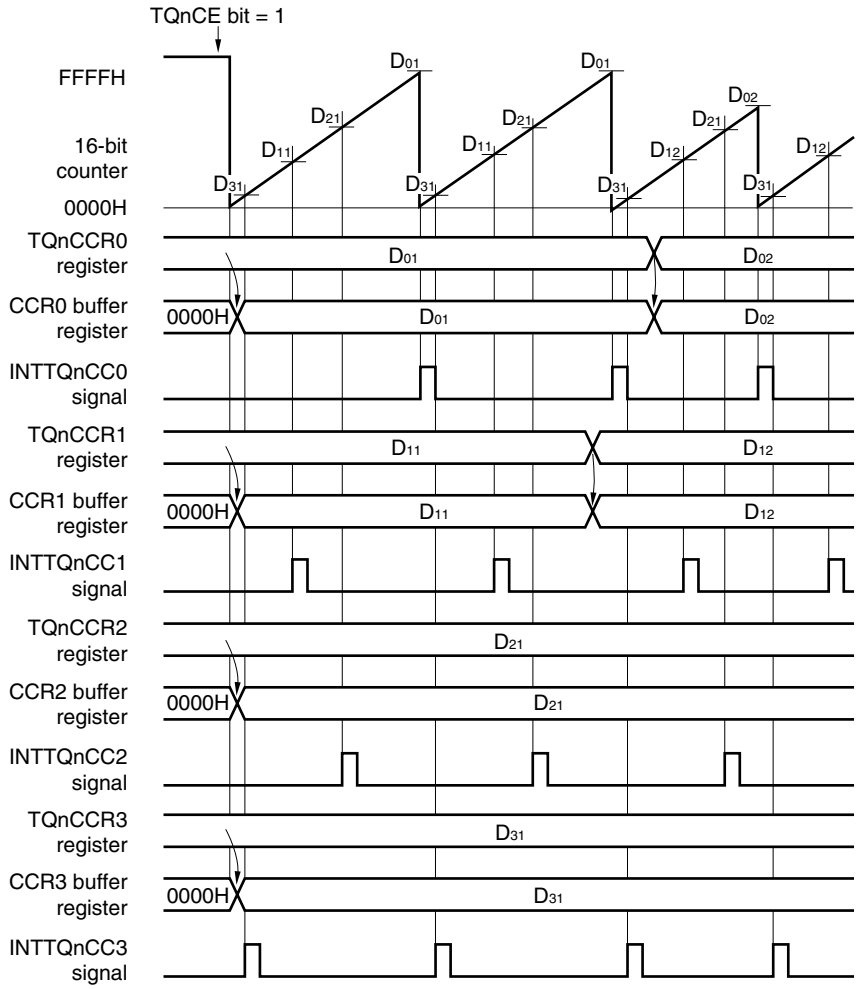
Remark k = 0, 2

(e) Interrupt operation

TMQn generates the following five interrupt request signals.

- INTTQnCC0 interrupt: This signal functions as a match interrupt request signal of the CCR0 buffer register and as a capture interrupt request signal to the TQnCCR0 register.
- INTTQnCC1 interrupt: This signal functions as a match interrupt request signal of the CCR1 buffer register and as a capture interrupt request signal to the TQnCCR1 register.
- INTTQnCC2 interrupt: This signal functions as a match interrupt request signal of the CCR2 buffer register and as a capture interrupt request signal to the TQnCCR2 register.
- INTTQnCC3 interrupt: This signal functions as a match interrupt request signal of the CCR3 buffer register and as a capture interrupt request signal to the TQnCCR3 register.
- INTTQnOV interrupt: This signal functions as an overflow interrupt request signal.

Figure 7-5. Timing of Anytime Write



Remarks 1. D_{01}, D_{02}: Setting values of TQnCCR0 register

D_{11}, D_{12}: Setting values of TQnCCR1 register

D_{21}: Setting value of TQnCCR2 register

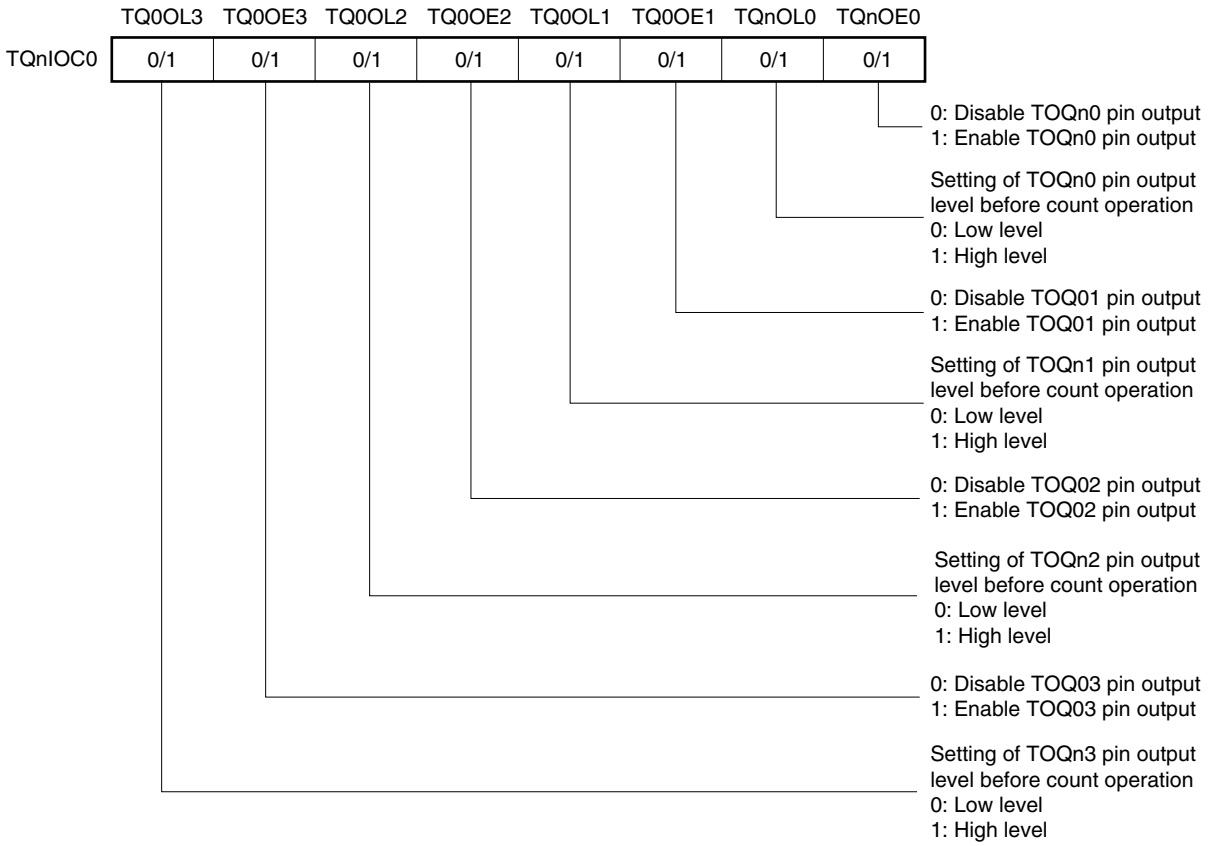
D_{31}: Setting value of TQnCCR3 register

2. The above timing chart illustrates an example of the operation in the interval timer mode.

3. n = 0, 1

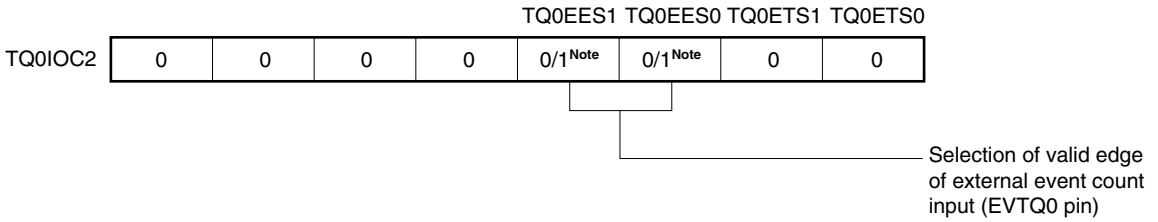
Figure 7-10. Register Setting for Interval Timer Mode Operation (2/3)

(c) TMQn I/O control register 0 (TQnIOC0)



<R>

(d) TMQ0 I/O control register 2 (TQ0IOC2)



Note Enable setting of the TQ0EES1 and TQ0EES0 bits only when timer output (TOQ00 to TOQ03) is used. In this case, set the TQ0CCR0 to TQ0CCR3 registers to the same value.

(e) TMQn counter read buffer register (TQnCNT)

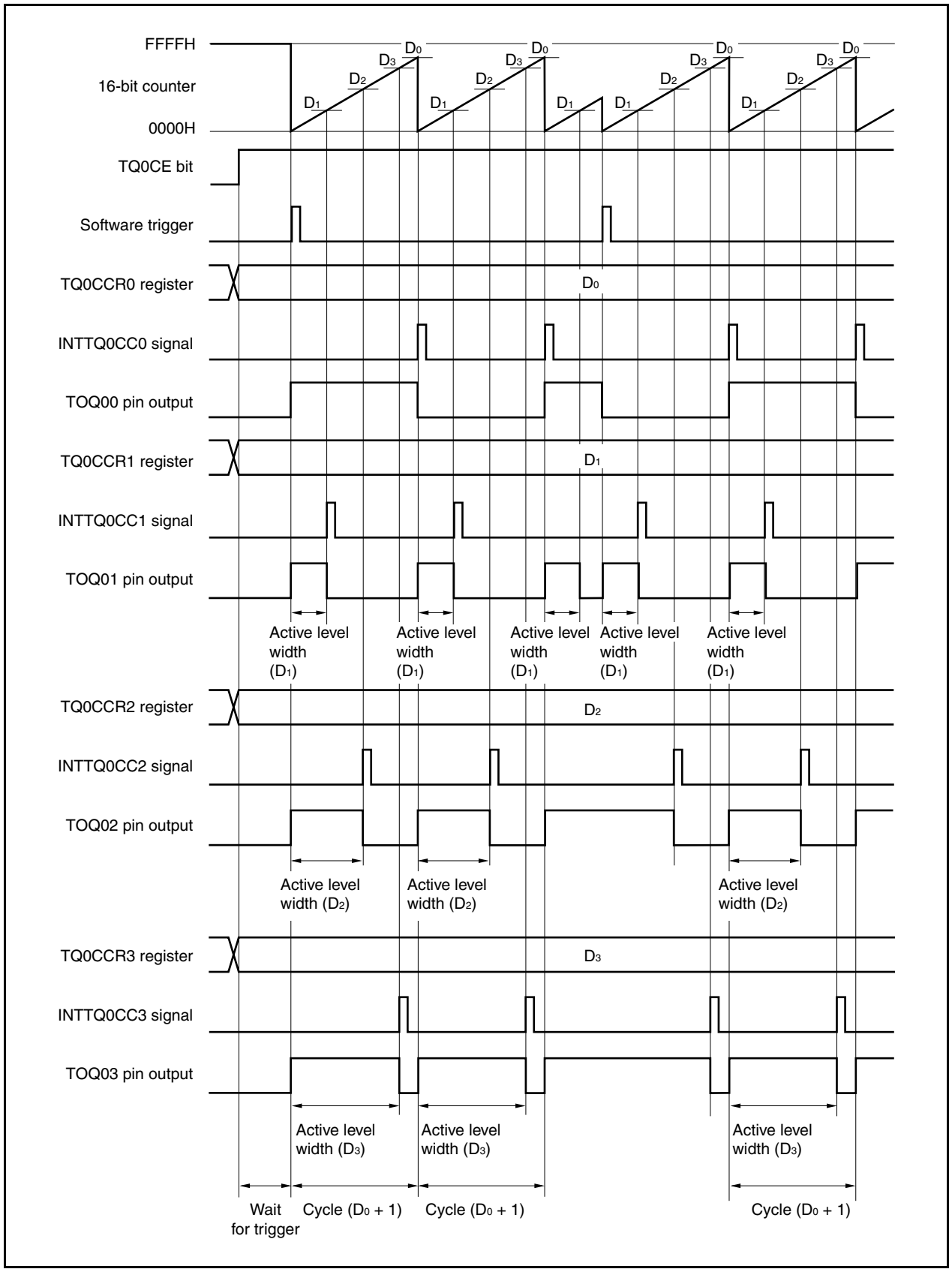
By reading the TQnCNT register, the count value of the 16-bit counter can be read.

(f) TMQn capture/compare register 0 (TQnCCR0)

If the TQnCCR0 register is set to D_0, the interval is as follows.

Interval = $(D_0 + 1) \times$ Count clock cycle

Figure 7-23. Basic Timing in External Trigger Pulse Output Mode



(3) TMQ1 option register 2 (TQ1OPT2)

The TQ1OPT2 register is an 8-bit register that controls the timer Q1 option function.

This register can be rewritten when the TQ1CTL0.TQ1CE bit is 1. However, rewriting the TQ1DTM bit is prohibited when the TQ1CE bit is 1. The same value can be rewritten.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

(1/2)

After reset: 00H R/W Address: FFFFF621H

	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TQ1OPT2	TQ1RDE	TQ1DTM	TQ1ATM03	TQ1ATM02	TQ1AT03	TQ1AT02	TQ1AT01	TQ1AT00

TQ1RDE	Transfer culling enable
0	Do not cull transfer (transfer timing is generated every time at crest and valley).
1	Cull transfer at the same interval as interrupt culling set by the TQ1OPT1 register.

TQ1DTM	Dead-time counter operation mode selection
0	Dead-time counter counts up normally and, if TOQ1m output of TMQ1 is at a narrow interval (TOQ1m output width < dead-time width), the dead-time counter is cleared and counts up again.
1	Dead-time counter counts up normally and, if TOQ1m output of TMQ1 is at a narrow interval (TOQ1m output width < dead-time width), the dead-time counter counts down and the dead-time control width is automatically narrowed.
Rewriting the TQ1DTM bit is disabled during timer operation. If it is rewritten by mistake, stop the timer operation by clearing the TQ1CE bit to 0, and re-set the TQ1DTM bit.	

Cautions 1. When using interrupt culling (the TQ1OPT1.TQ1ID4 to TQ1OPT1.TQ1ID0 bits are set to other than 00000), be sure to set the TQ1RDE bit to 1.

Therefore, the interrupt **and transfer are generated at the same timing. The interrupt and transfer cannot be set** separately**. If the interrupt and transfer are set separately (TQ1RDE bit = 0), transfer is not performed normally.**

<R> **2. To generate the dead-time period, set the TQ1DTC register to 1 or more.**

When the operation is stopped (TQ1CTL0.TQ1CE bit = 0), the dead-time period is not generated and the output level of the TOQ1T1 to TOQ1T3 pins and TOQ1B1 to TOQ1B3 pins will be in the initial status. For the system protection, therefore, before operation is being stopped, set the TOQ1T1 to TOQ1T3 and TOQ1B1 to TOQ1B3 pins to the high impedance state, or set the output level of pins and switch them to the port mode.

If a dead time period is not needed, set the TQ1DTC register to 0.

Remark m = 1 to 3

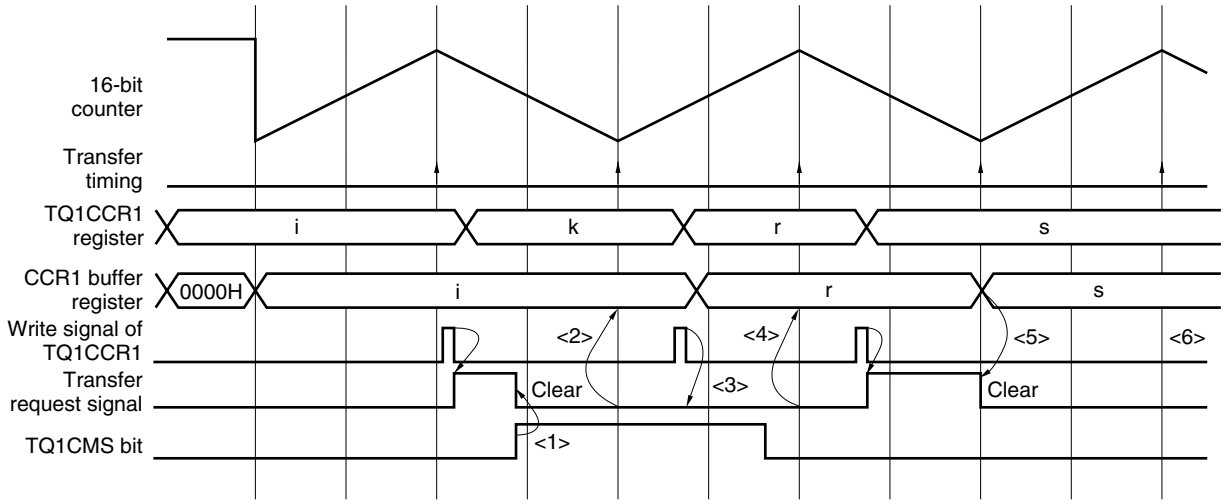
(4) Rewriting TQ1OPT0.TQ1CMS bit

The TQ1CMS bit can select the anytime rewrite mode and batch rewrite mode. This bit can be rewritten during timer operation (when TQ1CTL0.TQ1CE bit = 1). However, the operation and caution illustrated in Figure 9-31 are necessary.

If the TQ1CCR1 register is written when the TQ1CMS bit is cleared to 0, a transfer request signal (internal signal) is set.

When the transfer request signal is set, the register is transferred at the next transfer timing, and the transfer request signal is cleared. This transfer request signal is also cleared when the TQ1CMS bit is set to 1.

Figure 9-36. Rewriting TQ1CMS Bit



<1> If the TQ1CCR1 register is rewritten when the TQ1CMS bit is 0, the transfer request signal is set.
If the TQ1CMS bit is set to 1 in this status, the transfer request signal is cleared.

<2> The register is not transferred because the TQ1CMS bit is set to 1 and the transfer request signal is cleared.

<3> The transfer request signal is not set even if the TQ1CCR1 register is written when the TQ1CMS bit is 1.

<4> The transfer request signal is not set even if the TQ1CCR1 register is written when the TQ1CMS bit is 1, so even if the TQ1CMS bit is cleared to 0, transfer does not occur at the subsequent transfer timing.

<5> The transfer request signal is set if the TQ1CCR1 register is written when the TQ1CMS bit is 0.
Transfer is performed at the subsequent transfer timing and the transfer request signal is cleared.

<6> Once transfer has been performed, the transfer request signal is cleared. Therefore, transfer is not performed at the next transfer timing.

(5) Successive approximation register (SAR)

The SAR is a 10-bit register that sets voltage tap data whose values from the array match the voltage values of the analog input pins, 1 bit at a time starting from the most significant bit (MSB).

If data is set in the SAR all the way to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR (conversion results) are held in A/Dn conversion result registers 0 to 3 (ADAnCR0 to ADAnCR3) (n = 0, 1). When all the specified A/D conversion operations have ended, an A/Dn conversion end interrupt request signal (INTADn) is generated.

(6) A/Dn conversion result registers 0 to 3 (ADAnCR0 to ADAnCR3), A/Dn conversion result registers 0H to 3H (ADAnCR0H to ADAnCR3H) (n = 0, 1)

The ADAnCR0 to ADAnCR3 and ADAnCR0H to ADAnCR3H registers are registers that hold the A/D conversion results. Each time A/D conversion ends, the conversion result is loaded from the successive approximation register (SAR) and stored in the higher 10 bits of the ADAnCR0 to ADAnCR3 registers. The lower 6 bits of these registers are always 0 when read.

The higher 8 bits of the result of A/D conversion are read from the ADAnCR0H to ADAnCR3H registers. To read the result of A/D conversion in 16-bit units, specify the ADAnCR0 to ADAnCR3 registers. To read the higher 8 bits, specify the ADAnCR0H to ADAnCR3H registers.

(7) A/D converter n mode register 0 (ADAnM0) (n = 0, 1)

This register is used to specify the operation mode and controls the conversion operation.

(8) A/D converter n mode register 1 (ADAnM1) (n = 0, 1)

This register is used to set the number of conversion clocks of the analog input to be A/D converted.

(9) A/D converter n channel specification register (ADAnS) (n = 0, 1)

This register is used to specify the analog input pin to be A/D converted.

(10) A/D converter n mode register 2 (ADA2M2) (n = 0, 1)

This register is used to specify the buffer mode and specify the mode in the hardware trigger mode.

(11) ANIn0 to ANIn3 pins (n = 0, 1)

The ANIn0 to ANIn3 pins are analog input pins for A/D converters 0 and 1. They input the analog signals to be A/D converted.

Caution Make sure that the voltages input to ANIn0 to ANIn3 do not exceed the rated values. If a voltage higher than or equal to AV_{REFn} or lower than or equal to AV_{SSn} (even within the range of the absolute maximum ratings) is input to a channel, the conversion value of the channel is undefined, and the conversion values of the other channels may also be affected.

(12) AV_{REF0} and AV_{REF1} pins

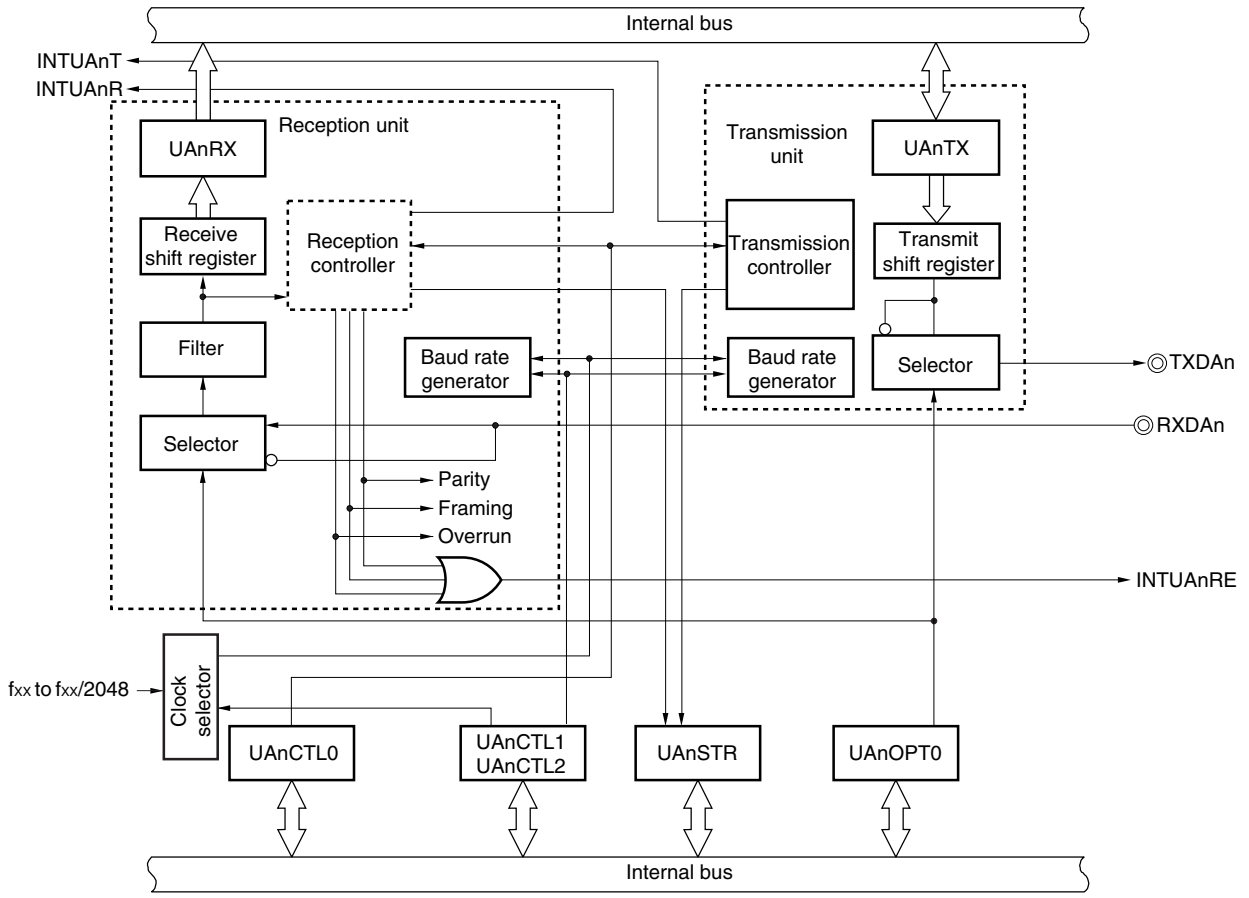
This is the pin for inputting the reference voltage of A/D converters 0 and 1. It converts signals input to the ANIn0 to ANIn3 pins to digital signals based on the voltage applied between AV_{REFn} and AV_{SSn} (n= 0, 1). Always make the potential at the AV_{REFn} pin the same as that at the EV_{DD} pin even when A/D converters 0 and 1 are not used.

The operating voltage range of the AV_{REFn} pin is $V_{DD} = EV_{DD} = AV_{DDn} = AV_{REFn}$ = 4.5 to 5.5 V.

12.2 Configuration

The block diagram of the UARTAn is shown below.

<R> **Figure 12-1. Block Diagram of UARTAn**



Remarks 1. n = 0, 1

2. For the configuration of the baud rate generator, see **Figure 12-9**.

UARTAn includes the following hardware units.

Table 12-1. Configuration of UARTAn

Item	Configuration
Registers	UARTAn control register 0 (UAnCTL0) UARTAn control register 1 (UAnCTL1) UARTAn control register 2 (UAnCTL2) UARTAn option control register 0 (UAnOPT0) UARTAn status register (UAnSTR) UARTAn receive shift register UARTAn receive data register (UAnRX) UARTAn transmit shift register UARTAn transmit data register (UAnTX)

12.5.6 Parity types and operations

The parity bit is used to detect bit errors in the communication data. Normally the same parity is used on the transmission side and the reception side.

In the case of even parity and odd parity, it is possible to detect odd-count bit errors. In the case of 0 parity and no parity, errors cannot be detected.

(a) Even parity

(i) During transmission

The number of bits whose value is “1” among the transmit data, including the parity bit, is controlled so as to be an even number. The parity bit values are as follows.

- Odd number of bits whose value is “1” among transmit data: 1
- Even number of bits whose value is “1” among transmit data: 0

(ii) During reception

The number of bits whose value is “1” among the reception data, including the parity bit, is counted, and if it is an odd number, a parity error is output.

(b) Odd parity

(i) During transmission

Opposite to even parity, the number of bits whose value is “1” among the transmit data, including the parity bit, is controlled so that it is an odd number. The parity bit values are as follows.

- Odd number of bits whose value is “1” among transmit data: 0
- Even number of bits whose value is “1” among transmit data: 1

(ii) During reception

The number of bits whose value is “1” among the receive data, including the parity bit, is counted, and if it is an even number, a parity error is output.

(c) 0 parity

During transmission, the parity bit is always made 0, regardless of the transmit data.

During reception, parity bit check is not performed. Therefore, no parity error occurs, regardless of whether the parity bit is 0 or 1.

(d) No parity

No parity bit is added to the transmit data.

Reception is performed assuming that there is no parity bit. No parity error occurs since there is no parity bit.

(2/2)

CB0DIR[Note 1]	Specification of transfer direction mode (MSB/LSB)
0	MSB first
1	LSB first

CB0TMS[Note 1]	Transfer mode specification
0	Single transfer mode
1	Continuous transfer mode

- When using single transmission or transmission/reception mode with communication type 2 or 4 (CB0CTL1.CB0DAP bit = 1), write the transfer data to the CB0TX register after checking that the CB0STR.CB0TSF bit is 0.

CB0SCE	Specification of start transfer disable/enable
0	Communication start trigger invalid
1	Communication start trigger valid

- In master mode
  This bit enables or disables the communication start trigger.
  (a) In single reception mode
  Clear the CB0SCE bit to 0 before reading the receive data (CB0RX register)[Note 2].
  (b) In continuous reception mode
  Clear the CB0SCE bit to 0 one communication clock before reception of the last data is ended[Note 3].
- In slave mode
  This bit enables or disables the communication start trigger.
  (a) In single reception mode or continuous reception mode
  Set the CB0SCE bit to 1[Note 4].
- In single transmission or transmission/reception mode, or continuous transmission or transmission/reception mode
  The function of the CB0SCE bit is invalid. It is recommended to set this bit to 1.

Notes 1. These bits can only be rewritten when the CB0PWR bit = 0. However, the CB0PWR can be set to 1 at the same time as these bits are rewritten.

2. If the CB0SCE bit is read while it is 1, the next communication operation is started.

3. The CB0SCE bit is not cleared to 0 one communication clock before the end of the last data reception, the next communication operation is automatically started.

To start communication operation again after reading the last data, set the CB0SCE bit to 1 and perform a dummy read of the CB0RX register.

4. To start the reception, a dummy read is necessary.

14.3.6 In-service priority register (ISPR)

The ISPR register holds the priority level of the maskable interrupt currently acknowledged. When an interrupt request signal is acknowledged, the bit of this register corresponding to the priority level of that interrupt signal request is set to 1 and remains set while the interrupt is serviced.

When the RETI instruction is executed, the bit corresponding to the interrupt request signal having the highest priority is automatically cleared to 0 by hardware. However, it is not cleared to 0 when execution is returned from non-maskable interrupt servicing or exception processing.

This register is read-only, in 8-bit or 1-bit units.

Reset sets this register to 00H.

Caution In the interrupt enabled (EI) state, if an interrupt is acknowledged during the reading of the ISPR register, the value of the ISPR register may be read after the bit is set (1) by this interrupt acknowledgment. To read the value of the ISPR register properly before interrupt acknowledgment, read it in the interrupt disabled (DI) state.

After reset: 00H R Address: FFFFF1FAH

	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
ISPR	ISPR7	ISPR6	ISPR5	ISPR4	ISPR3	ISPR2	ISPR1	ISPR0

ISPRn	Priority of interrupt currently being acknowledged
0	Interrupt request signal with priority n is not acknowledged
1	Interrupt request signal with priority n is being acknowledged

Remark n: 0 to 7 (priority level)

(2) Generation of exception in servicing program

Servicing program of maskable interrupt or exception

... ... • EIPC saved to memory or register • EIPSW saved to memory or register ... • TRAP instruction ... • Saved value restored to EIPSW • Saved value restored to EIPC • RETI instruction	← Exception such as TRAP instruction acknowledged.

The priority order for multiple interrupt servicing control has 8 levels, from 0 to 7 for each maskable interrupt request signal (0 is the highest priority), but it can be set as desired via software. The priority order is set using the xxPRn0 to xxPRn2 bits of the interrupt control request register (xxICn), provided for each maskable interrupt request signal. After system reset, an interrupt request signal is masked by the xxMKn bit and the priority order is set to level 7 by the xxPRn0 to xxPRn2 bits.

The priority order of maskable interrupts is as follows.

(High) Level 0 > Level 1 > Level 2 > Level 3 > Level 4 > Level 5 > Level 6 > Level 7 (Low)

Interrupt servicing that has been suspended as a result of multiple servicing control is resumed after the servicing of the higher priority interrupt has been completed and the RETI instruction has been executed.
A pending interrupt request signal is acknowledged after the current interrupt servicing has been completed and the RETI instruction has been executed.

Caution In a non-maskable interrupt servicing routine (time until the RETI instruction is executed), maskable interrupts are suspended and not acknowledged.

Remark xx: Identification name of each peripheral unit (see **Table 14-2**)
n: Peripheral unit number (see **Table 14-2**)

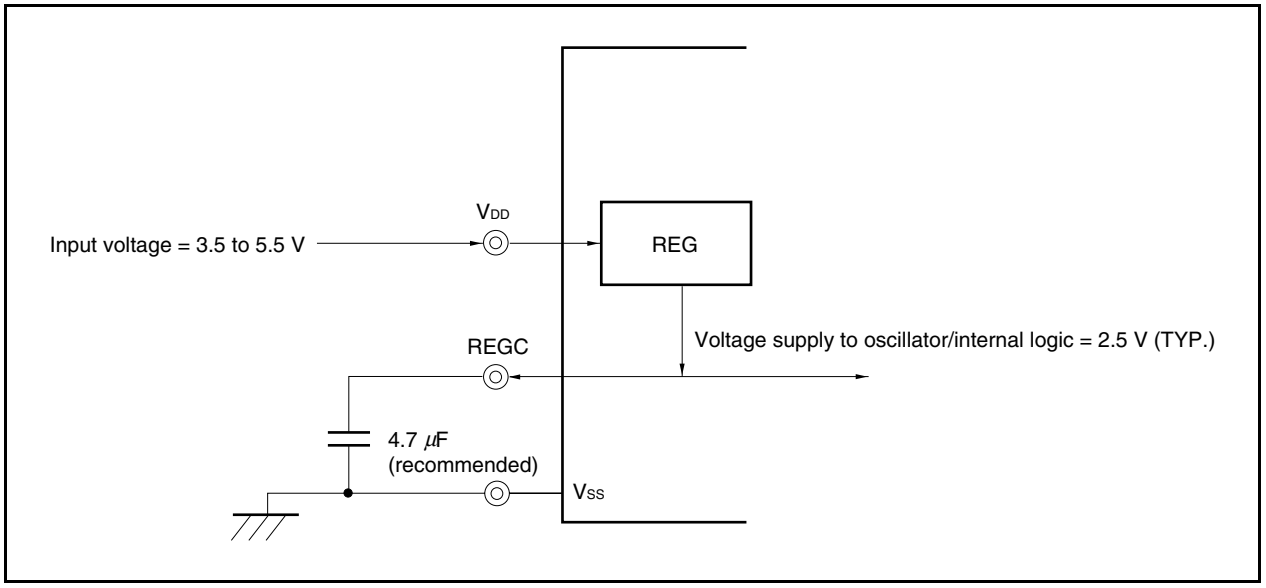
17.2 Operation

The regulator of this product always operates in any mode (normal operation mode, HALT mode, IDLE mode, STOP mode, or during reset).

Be sure to connect a capacitor (4.7 μF (recommended value)) to the REGC pin to stabilize the regulator output.

A diagram of the regulator pin connection method is shown below.

Figure 17-2. REGC Pin Connection

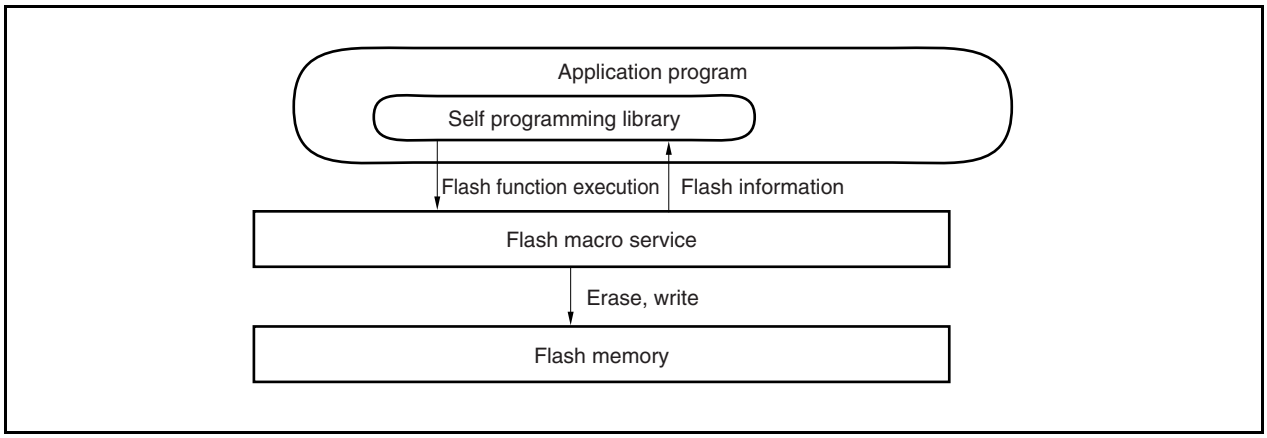


18.5 Rewriting by Self Programming (μPD70F3714 only)

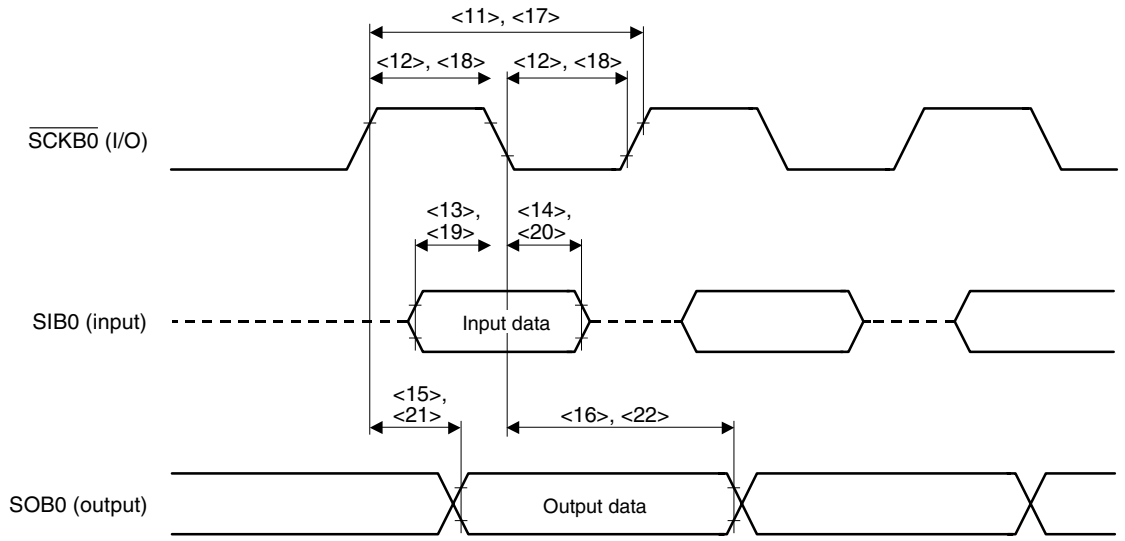
18.5.1 Overview

The V850ES/IE2 supports a flash macro service that allows the user program to rewrite the internal flash memory by itself. By using this interface and a self programming library that is used to rewrite the flash memory with a user application program, the flash memory can be rewritten by a user application transferred in advance to the internal RAM or external memory. Consequently, the user program can be upgraded and constant data can be rewritten in the field.

Figure 18-15. Concept of Self Programming

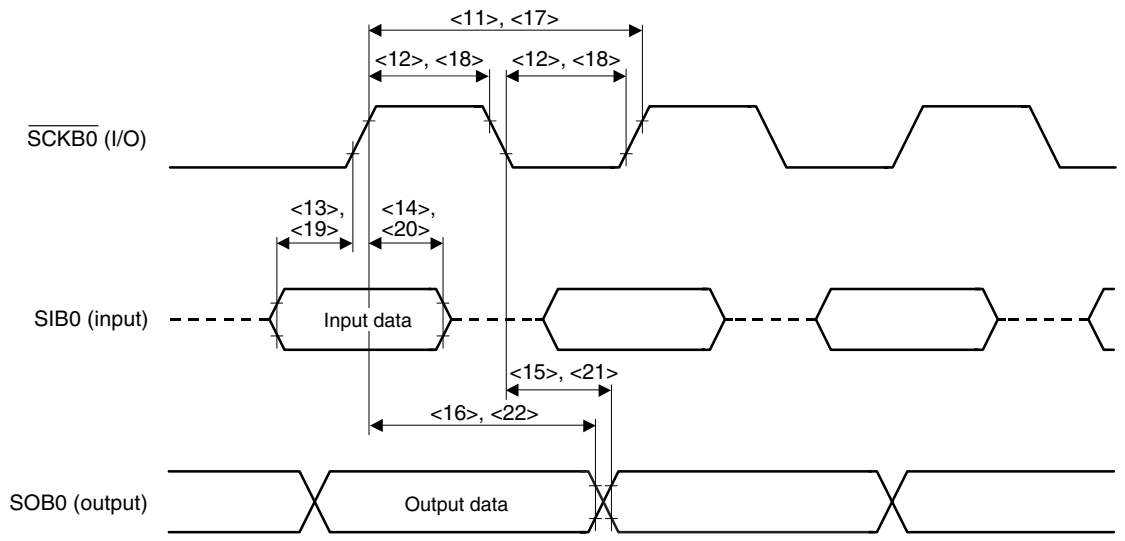


CSIB Timing: CB0CTL1.CB0CKP, CB0CTL1.CB0DAP Bits = 10



Remark The broken lines indicate high impedance.

CSIB Timing: CB0CTL1.CB0CKP, CB0CTL1.CB0DAP Bits = 11



Remark The broken lines indicate high impedance.

(2/3)

Page	Description
p. 213	Modification of description in **6.6.5 (2) (b) 0%/100% output of PWM waveform**
p. 232	Modification of description in **Figure 6-41 Configuration in Pulse Width Measurement Mode**
p. 233	Modification of description in **6.6.7 Pulse width measurement mode (TPkMD2 to TPkMD0 bits = 110)**
pp. 234, 235	Modification of description in **Figure 6-43 Register Setting in Pulse Width Measurement Mode**
p. 236	Deletion of description from **Figure 6-44 Software Processing Flow in Pulse Width Measurement Mode**
p. 238	Addition of description to **Table 7-1 TMQn Overview**
p. 246	Modification of description in **7.4 (3) TMQn I/O control register 0 (TQnIOC0)**
p. 262	Modification of description in **7.6 (1) (a) Counter start operation**
pp. 270 to 272	Modification of description in **Figure 7-10 Register Setting for Interval Timer Mode Operation**
p. 273	Addition of description to **Figure 7-11 Software Processing Flow in Interval Timer Mode**
p. 278	Modification of description in **7.6.1 (2) (d) Operation of TQnCCR1 to TQnCCR3 registers**
p. 280	Addition of **7.6.1 (3) Operation by external event count input (EVTQ0)**
p. 281	Addition of description to **7.6.2 External event count mode (TQ0MD2 to TQ0MD0 bits = 001)**
p. 284	Addition of description to **Figure 7-17 Register Setting for Operation in External Event Count Mode**
p. 286	Addition of description to **7.6.2 (2) Operation timing in external event count mode**
p. 292	Modification of figure description in **Figure 7-23 Basic Timing in External Trigger Pulse Output Mode**
p. 293	Addition of description to **7.6.3 External trigger pulse output mode (TQ0MD2 to TQ0MD0 bits = 010)**
p. 301	Modification of description in **7.6.3 (2) (b) 0%/100% output of PWM waveform**
p. 309	Modification of description in **Figure 7-28 Register Setting in One-Shot Pulse Output Mode**
pp. 310, 311	Modification of description in **Figure 7-29 Software Processing Flow in One-Shot Pulse Output Mode**
p. 323	Modification of description in **7.6.5 (2) (b) 0%/100% output of PWM waveform**
p. 346	Modification of description in **7.6.7 Pulse width measurement mode (TQ0MD2 to TQ0MD0 bits = 110)**
p. 363	Addition of description to **9.2 (1) TMQ1 dead-time compare register (TQ1DTC)**
p. 365	Addition of description to **9.3 (2) TMQ1 option register 1 (TQ1OPT1)**
p. 366	Addition of description to **9.3 (3) TMQ1 option register 2 (TQ1OPT2)**
p. 370	Addition of description to **Figure 9-3 Output Control of TOQ1Tm and TOQ1Bm Pins (Without Dead Time)**
p. 378	Modification of **Figure 9-5 Outline of 6-Phase PWM Output Mode**
p. 383	Modification of **Figure 9-9 0% PWM Output Waveform (with Dead Time)**
p. 384	Modification of **Figure 9-10 100% PWM Output Waveform (with Dead Time)**
p. 385	Modification of **Figure 9-11 PWM Output Waveform from 0% to 100% and from 100% to 0% (with Dead Time)**
p. 389	Addition of description to **9.4.3 Interrupt culling function**
p. 438	Modification of description in **11.4.1 Basic operation**
p. 475	Modification of **Figure 12-1 Block Diagram of UARTAn**
p. 476	Modification of description in **12.2 (5) UARTAn status register (UAnSTR)**
p. 477	Modification of description in **12.3 (1) UARTAn control register 0 (UAnCTL0)**
p. 487	Modification of **Figure 12-5 Continuous Transmission Operation Timing**
p. 523	Modification of figure description in **13.4.7 (2) Operation timing**
p. 559	Addition of description to **14.3.4 Interrupt control registers (xxICn)**
p. 572	Addition of description to **14.6.1 (2) Restore**