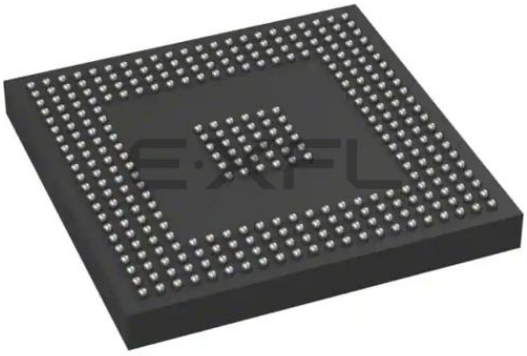
Renesas Electronics America Inc - R7S721011VCBG#AC0 Datasheet



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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

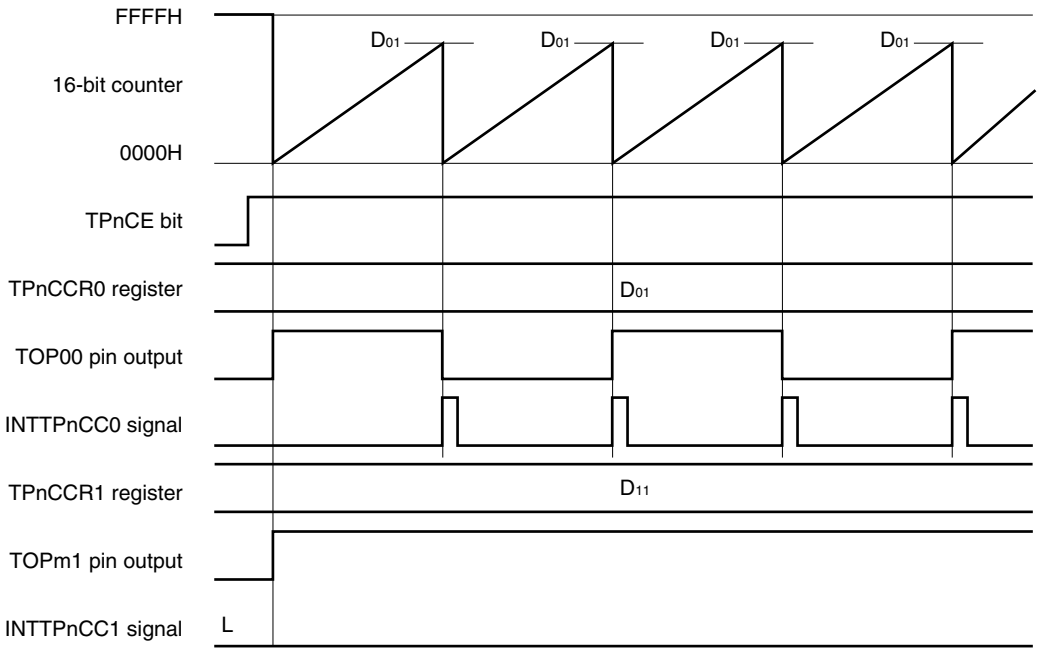
Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DVD, VDC
Ethernet	10/100Mbps (1), 100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.2V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	324-FBGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s721011vcbg-ac0

If the set value of the TPnCCR1 register is greater than the set value of the TPnCCR0 register, the count value of the 16-bit counter does not match the value of the TPnCCR1 register. Consequently, the INTTPnCC1 signal is not generated, nor is the output of the TOPm1 pin changed.

When the TPnCCR1 register is not used, it is recommended to set its value to FFFFH.

Figure 6-15. Timing Chart When $D_{01} < D_{11}$



Remark n = 0 to 3
m = 0, 2, 3

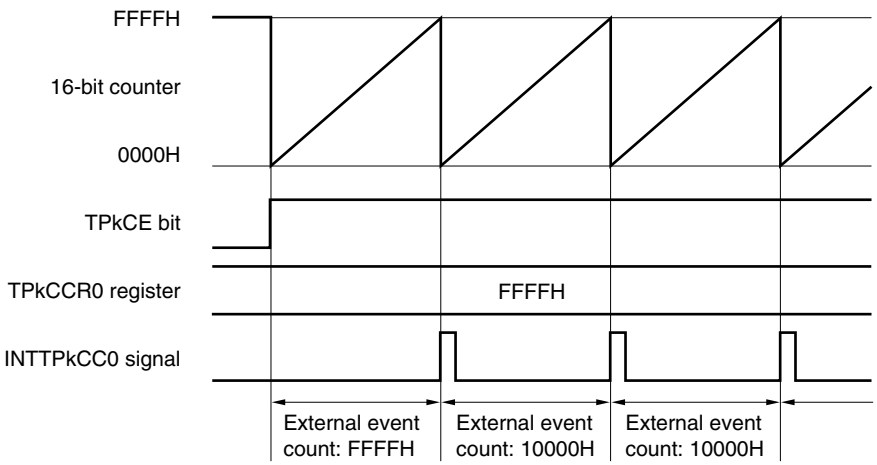
(2) Operation timing in external event count mode

Cautions 1. In the external event count mode, the TPkCCR0 and TPkCCR1 registers must not be cleared to 0000H.

<R> **2. In the external event count mode, use of the timer output (TOP00, TOPk1) is disabled. If using timer output (TOPk1) with external event count input (TIPk0), set the interval timer mode, and enable the count clock operation with the external event count input (TPkCTL1.TPkEEE bit = 1) (see 6.6.1 (3) Operation by external event count input (TIPk0)).**

(a) Operation if TPkCCR0 register is set to FFFFH

If the TPkCCR0 register is set to FFFFH, the 16-bit counter counts to FFFFH each time the valid edge of the external event count signal has been detected. The 16-bit counter is cleared to 0000H in synchronization with the next count-up timing, and the INTTPkCC0 signal is generated. At this time, the TPkOPT0.TPkOVF bit is not set.



Remark k = 0, 2

Figure 6-33. Register Setting in PWM Output Mode (1/2)

(a) TMPm control register 0 (TPmCTL0)

	TPmCE					TPmCKS2	TPmCKS1	TPmCKS0
TPmCTL0	0/1	0	0	0	0	0/1	0/1	0/1

Select count clock[Note]

0: Stop counting
1: Enable counting

Note The setting is invalid when the TPmCTL1.TPkEEE bit = 1.

(b) TMPm control register 1 (TPmCTL1)

		TPmEST	TPkEEE			TPmMD2	TPmMD1	TPmMD0
TPmCTL1	0	0	0/1	0	0	1	0	0

1, 0, 0:
PWM output mode

0: Operate on count clock selected by TPkCKS0 to TPkCKS2 bits
1: Count with external event count input signal

(c) TMPm I/O control register 0 (TPmIOC0)

<R>

					TPmOL1	TPmOE1	TP0OL0	TP0OE0
TPmIOC0	0	0	0	0	0/1	0/1	0/1	0/1[Note]

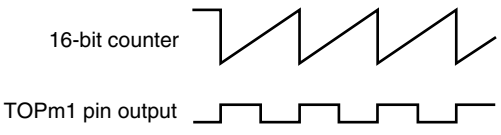
0: Disable TOP00 pin output
1: Enable TOP00 pin output

Setting of TOP00 pin output level before count operation
0: Low level
1: High level

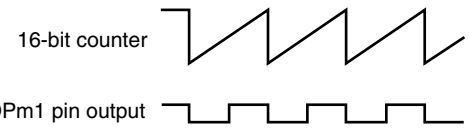
0: Disable TOPm1 pin output
1: Enable TOPm1 pin output

Setting of TOPm1 pin output level before count operation
0: Low level
1: High level

- When TPmOL1 bit = 0



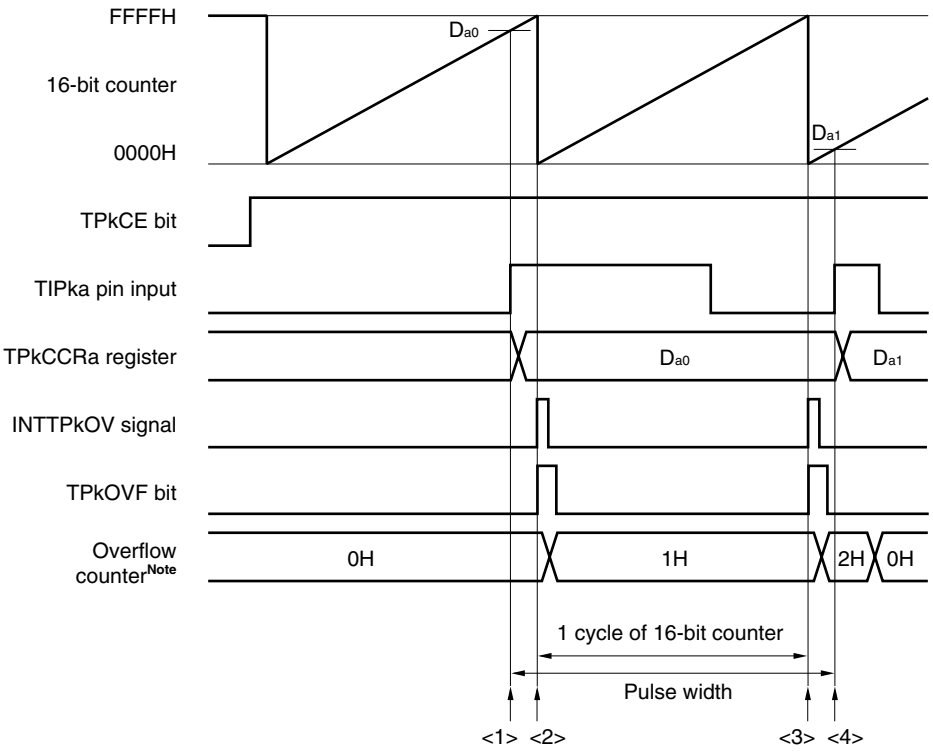
- When TPmOL1 bit = 1



<R>

Note Clear this bit to 0 when the TOP00 pin is not used in the PWM output mode.

Example when capture trigger interval is long



Note The overflow counter is set arbitrarily by software on the internal RAM.

<1> Read the TPkCCRa register (setting of the default value of the TIPka pin input).

<2> An overflow occurs. Increment the overflow counter and clear the overflow flag to 0 in the overflow interrupt servicing.

<3> An overflow occurs a second time. Increment (+1) the overflow counter and clear the overflow flag to 0 in the overflow interrupt servicing.

<4> Read the TPkCCRa register.

Read the overflow counter.

→ When the overflow counter is “N”, the pulse width can be calculated by (N × 10000H + D_{a1} – D_{a0}).

In this example, the pulse width is (20000H + D_{a1} – D_{a0}) because an overflow occurs twice.

Clear the overflow counter (0H).

Remark k = 0, 2

a = 0, 1

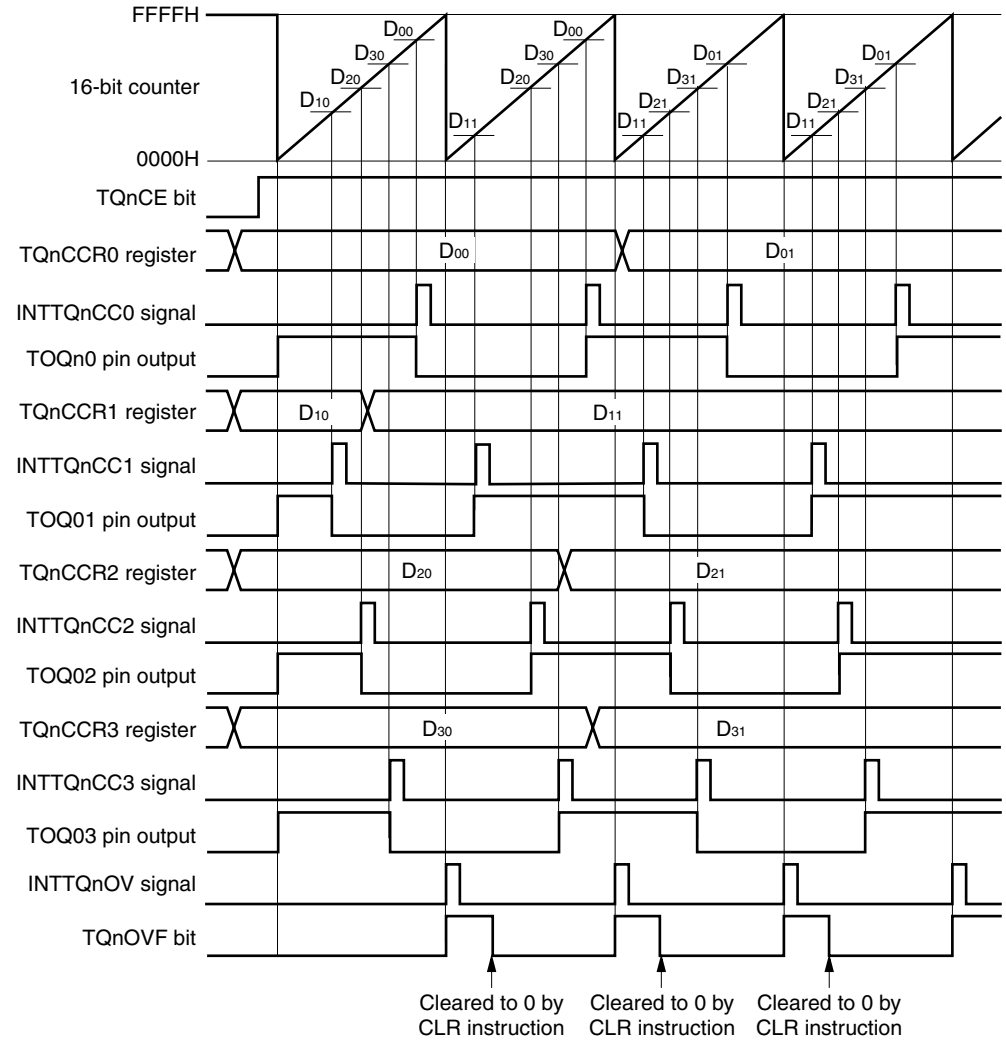
- Compare operation

  When the TQnCE bit is set to 1, 16-bit timer/event counter Q starts counting, and the output signals of the TOQ00 to TOQ03 and TOQ10 pins are inverted. When the count value of the 16-bit counter later matches the set value of the TQnCCRa register, a compare match interrupt request signal (INTTQnCCa) is generated, and the output signals of the TOQ00 to TOQ03 and TOQ10 pins are inverted.

  The 16-bit counter continues counting in synchronization with the count clock. When it counts up to FFFFH, it generates an overflow interrupt request signal (INTTQnOV) at the next clock, is cleared to 0000H, and continues counting. At this time, the overflow flag (TQnOPT0.TQnOVF bit) is also set to 1. Confirm that the overflow flag is set to 1 and then clear it to 0 by executing the CLR instruction via software.

  The TQnCCRa register can be rewritten while the counter is operating. If it is rewritten, the new value is reflected at that time by anytime write, and compared with the count value.

Figure 7-35. Basic Timing in Free-Running Timer Mode (Compare Function)

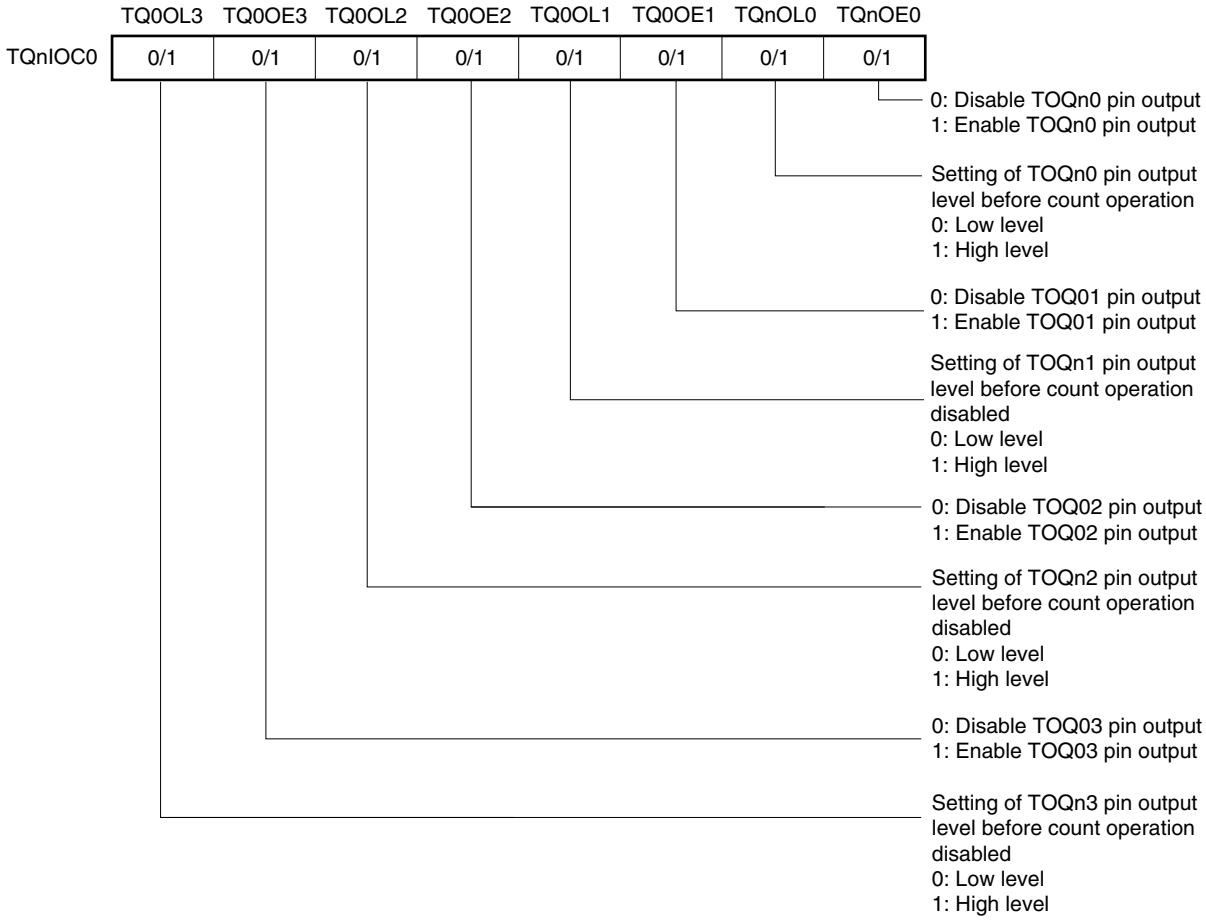


Remark n = 0, 1

a = 0 to 3

Figure 7-37. Register Setting in Free-Running Timer Mode (2/3)

(c) TMQn I/O control register 0 (TQnIOC0)



(d) TMQ0 I/O control register 1 (TQ0IOC1)

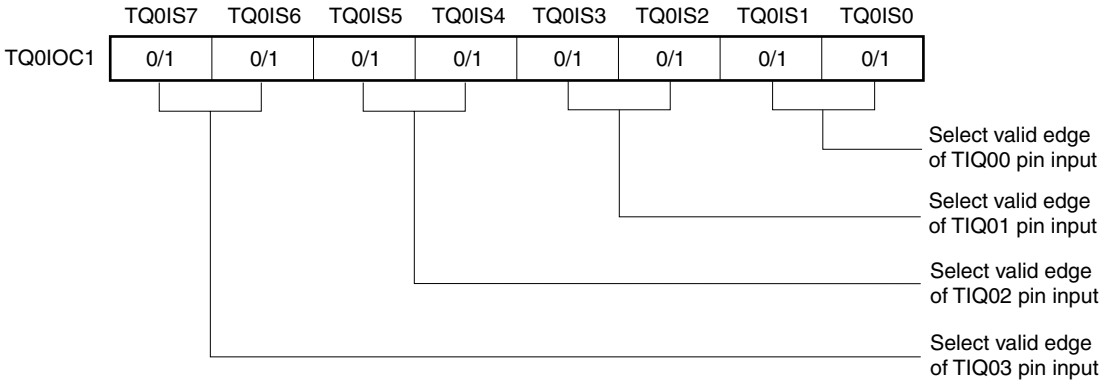
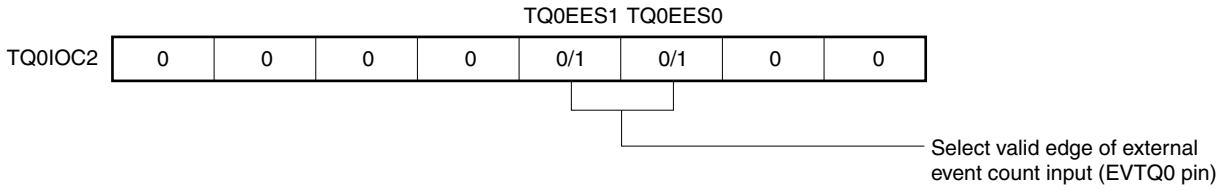
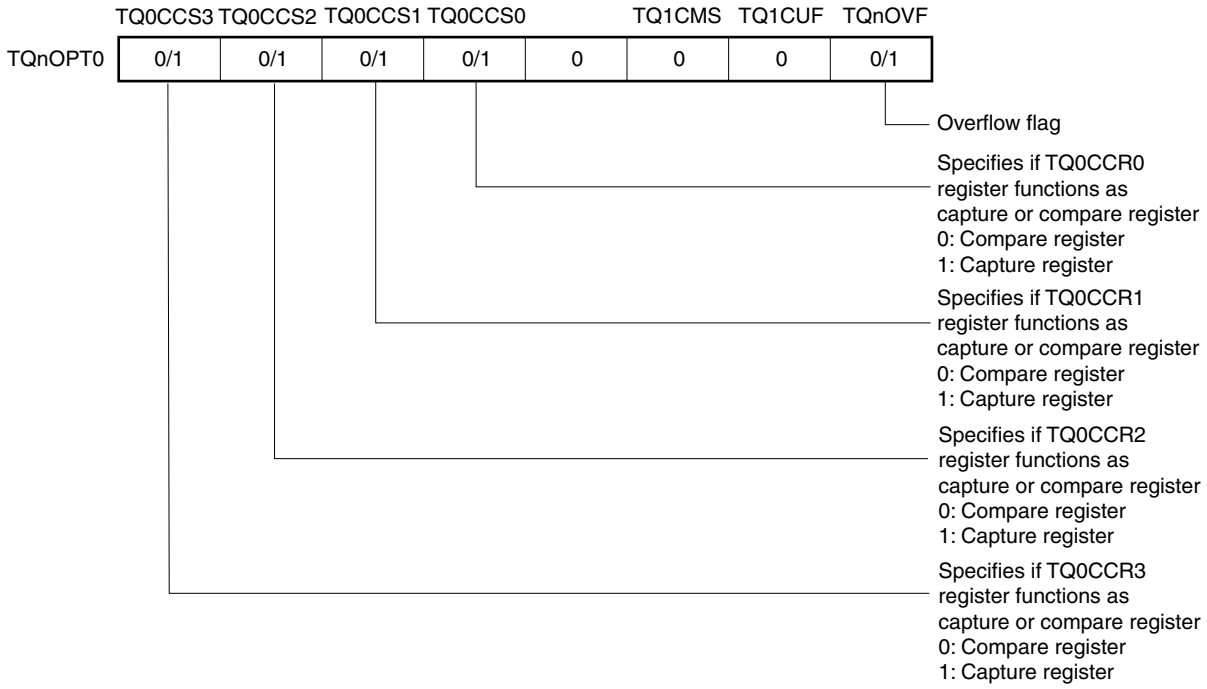


Figure 7-37. Register Setting in Free-Running Timer Mode (3/3)

(e) TMQ0 I/O control register 2 (TQ0IOC2)



(f) TMQn option register 0 (TQnOPT0)



(g) TMQn counter read buffer register (TQnCNT)

The value of the 16-bit counter can be read by reading the TQnCNT register.

(h) TMQn capture/compare registers 0 to 3 (TQnCCR0 to TQnCCR3)

These registers function as capture registers or compare registers depending on the setting of the TQ0OPT0.TQ0CCSa bit.

When the registers function as capture registers, they store the count value of the 16-bit counter when the valid edge input to the TIQ0a pin is detected.

When the registers function as compare registers and when D_a is set to the TQnCCRa register, the INTTQnCCa signal is generated when the counter reaches (D_a + 1), and the output signals of the TOQ00 to TOQ03 and TOQ10 pins are inverted.

Remark a = 0 to 3

(1/2)

After reset: 00H R/W Address: HZA0CTL0 FFFFF5F0H, HZA0CTL1 FFFFF5F1H, HZA1CTL0 FFFFF630H, HZA1CTL1 FFFFF631H

HZAyCTLn (n = 0, 1; y = 0, 1)

<7>	<6>	5	4	<3>	<2>	1	<0>
HZAyDCEn	HZAyDCMn	HZAyDCNn	HZAyDCPn	HZAyDCTn	HZAyDCCn	0	HZAyDCFn

HZAyDCEn	High-impedance output control
0	Disable high-impedance output control operation. Pins can function as output pins.
1	Enable high-impedance output control operation.

HZAyDCMn	Condition of clearing high-impedance state by HZAyDCCn bit
0	Setting of the HZAyDCCn bit is valid regardless of the external pin[Note] input.
1	Setting of the HZAyDCCn bit is invalid while the external pin[Note] input holds a level detected as abnormal (active level).
Rewrite the HZAyDCMn bit when the HZAyDCEn bit = 0.	

HZAyDCNn	HZAyDCPn	External pin[Note] input edge specification
0	0	No valid edge (setting the HZAyDCFn bit by external pin[Note] input is prohibited).
0	1	Rising edge of the external pin[Note] input is valid (abnormality is detected by rising edge input).
1	0	Falling edge of the external pin[Note] input is valid (abnormality is detected by falling edge input).
1	1	Setting prohibited

- Rewrite the HZAyDCNn and HZAyDCPn bits when the HZAyDCEn bit is 0.
- For the edge specification of the INTP0 to INTP3 pins, see **14.4.2 (1) External interrupt rising edge specification register 0 (INTR0), external interrupt falling edge specification register 0 (INTF0)**.
- High-impedance output control is performed when the valid edge is input after the operation is enabled (by setting HZAyDCEn bit to 1). If the external pin[Note] is at the active level when the operation is enabled, therefore, high-impedance output control is not performed.

HZAyDCTn	High-impedance output trigger bit
0	No operation
1	Pins are made to go into a high-impedance state by software and the HZAyDCFn bit is set to 1.

- If an edge indicating abnormality is input to the external pin[Note] (which is detected according to the setting of the HZAyDCNn and HZAyDCPn bits), the HZAyDCTn bit is invalid even if it is set to 1.
- The HZAyDCTn bit is always 0 when it is read because it is a software-triggered bit.
- The HZAyDCTn bit is invalid even if it is set to 1 when the HZAyDCEn bit = 0.
- Simultaneously setting the HZAyDCTn and HZAyDCCn bits to 1 is prohibited.

Note HZA0CTL0: TOQH0OFF pin, HZA0CTL1: TOP2OFF pin, HZA1CTL0: TOQ1OFF pin, HZA1CTL1: TOP3OFF pin

(2/2)

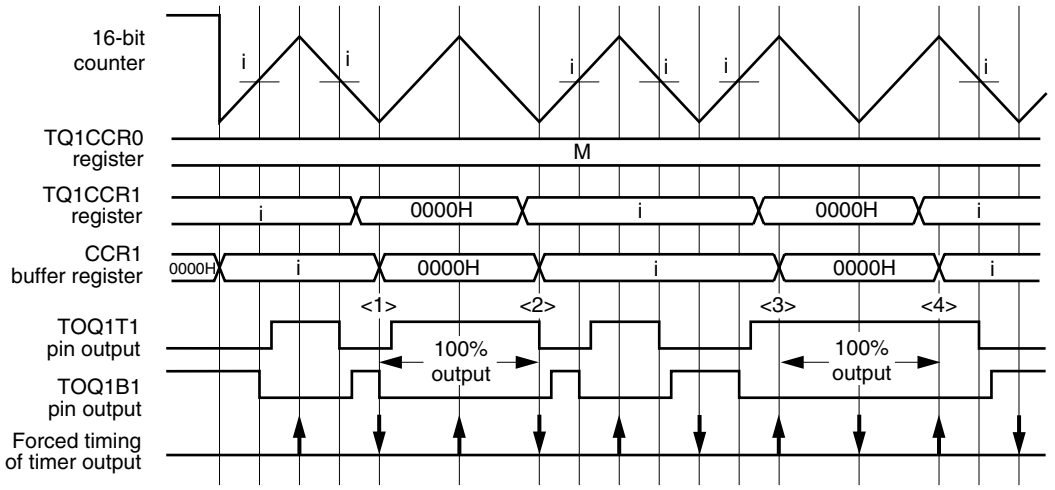
HZAyDCCn	High-impedance output control clear bit
0	No operation
1	Pins that have gone into a high-impedance state are output-enabled by software and the HZAyDCFn bit is cleared to 0.

- Pins can function as output pins when the HZAyDCM bit = 0, regardless of the status of the external pin[Note].
- If an edge indicating abnormality is input to the external pin[Note] (which is set by the HZAyDCNn and HZAyDCPn bits) when the HZAyDCM bit = 1, the HZAyDCCn bit is invalid even if it is set to 1.
- The HZAyDCCn bit is always 0 when it is read.
- The HZAyDCCn bit is invalid even if it is set to 1 when the HZAyDCEn bit = 0.
- Simultaneously setting the HZAyDCTn and HZAyDCCn bits to 1 is prohibited.

HZAyDCFn	High-impedance output status flag
0	Indicates that output of the pin is enabled. • This bit is cleared to 0 when the HZAyDCEn bit = 0. • This bit is cleared to 0 when the HZAyDCCn bit = 1.
1	Indicates that the pin goes into a high-impedance state. • This bit is set to 1 when the HZAyDCTn bit = 1. • This bit is set to 1 when an edge indicating abnormality is input to the external pin[Note] (which is detected according to the setting of the HZAyDCNn and HZAyDCPn bits).

Note HZA0CTL0: TOQH0OFF pin, HZA0CTL1: TOP2OFF pin, HZA1CTL0: TOQ1OFF pin, HZA1CTL1: TOP3OFF pin

<R> **Figure 9-10. 100% PWM Output Waveform (with Dead Time)**



<1> 100% output is selected by the valley interrupt (with a match with the 16-bit counter).
The valley interrupt forcibly lowers the timer output, but raising the timer output takes precedence when the value of the TQ1CCRm register matches the value of the 16-bit counter. As a result, the 100% output is produced.

<2> 100% output is canceled by the valley interrupt (without a match with the 16-bit counter).
The valley interrupt forcibly lowers the timer output. This cancels the 100% output.

<3> 100% output is selected by the crest interrupt (without a match with the 16-bit counter).
The crest interrupt forcibly raises the timer output. This produces the 100% output.

<4> 100% output is canceled by the crest interrupt (without a match with the 16-bit counter).
The crest interrupt forcibly raises the timer output. This cancels the 100% output.

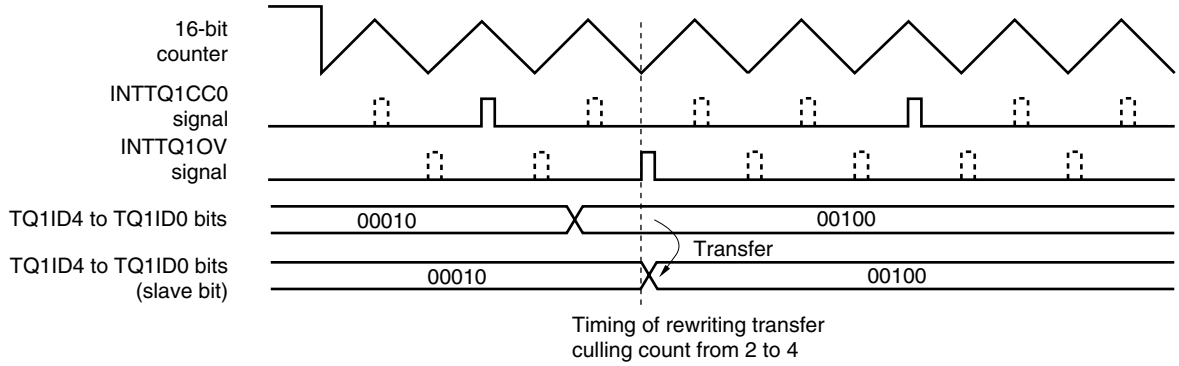
Remark ↑ means forced raising and ↓ means forced lowering.

(2) To alternately output crest interrupt (INTTQ1CC0) and valley interrupt (INTTQ1OV)

To alternately output the crest and valley interrupts, set both the TQ1OPT1.TQ1ICE and TQ1OPT1.TQ1IOE bits to 1.

Figure 9-18. Crest/Valley Interrupt Output

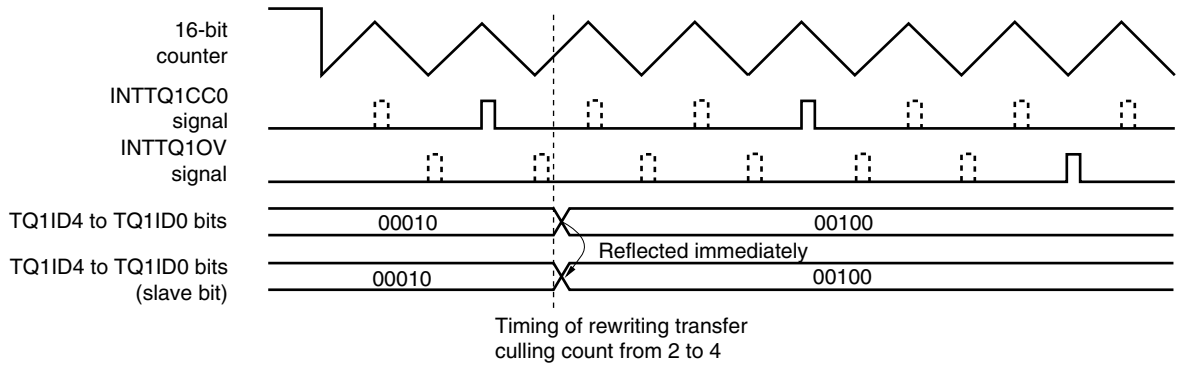
(a) TQ1OPT0.TQ1CMS bit = 0, TQ1OPT2.TQ1RDE bit = 1 (with transfer culling control)



Remarks 1. Transfer is performed at the culled interrupt output timing. The other transfer timing is ignored.

2. : Culled interrupt

(b) TQ1CMS bit = 1, TQ1RDE bit = 0 or 1 (without transfer control)



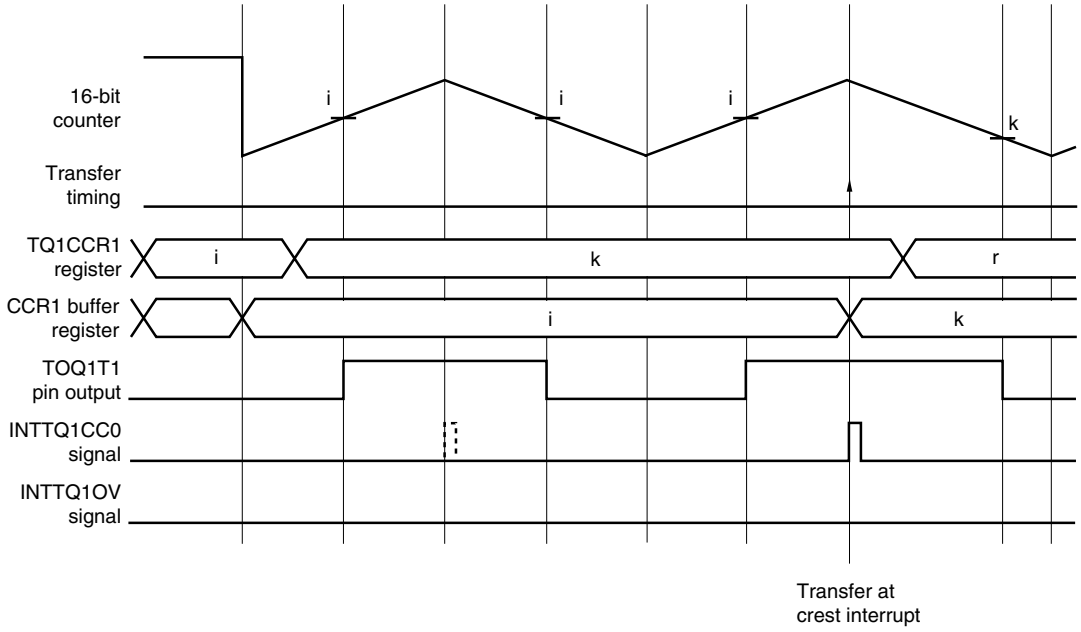
Remarks 1. Rewriting is reflected immediately. The transfer timing is ignored.

2. : Culled interrupt

(c) Rewriting TQ1CCR1 to TQ1CCR3 registers

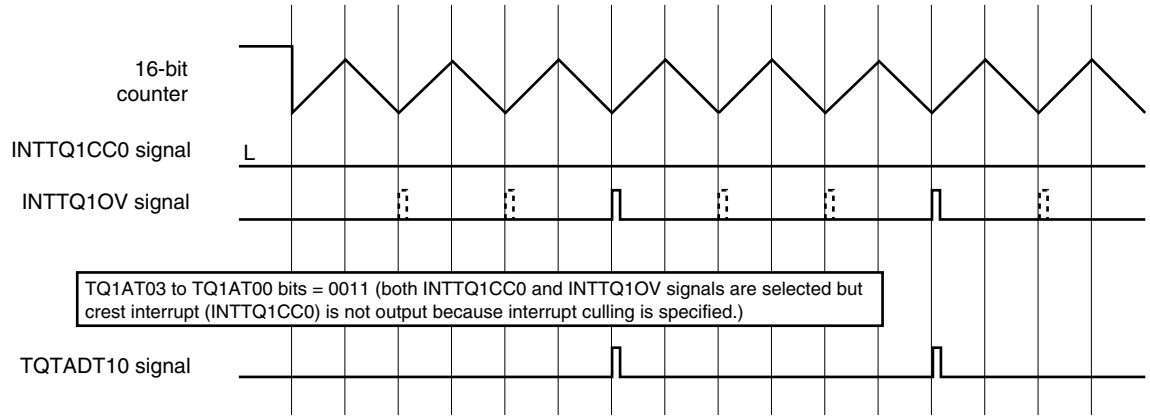
- Transfer at crest when crest interrupt is set
  Because the register is transferred at the transfer timing of the crest interrupt, an asymmetrical triangular wave is output.

Figure 9-34. Rewriting TQ1CCR1 Register
(TQ1OPT1.TQ1ICE bit = 1, TQ1OPT1.TQ1IOE bit = 0, TQ1OPT1.TQ1ID4 to TQ1OPT1.TQ1ID0 = 00001)



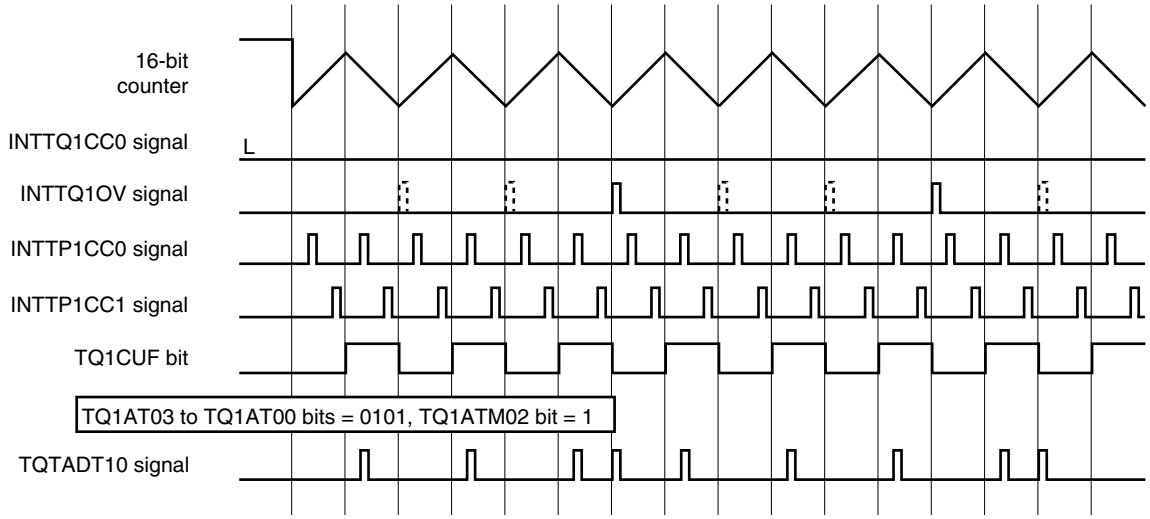
Remark : Culled interrupt

Figure 9-39. Example of A/D Conversion Start Trigger (TQTADT10) Signal Output (TQ1OPT1.TQ1ICE Bit = 0, TQ1OPT1.TQ1IOE Bit = 1, TQ1OPT1.TQ1ID4 to TQ1OPT1.Q1ID0 Bits = 00010: With Interrupt Culling) (1)



Remark : Culled interrupt

Figure 9-40. Example of A/D Conversion Start Trigger (TQTADT10) Signal Output (TQ1OPT1.TQ1ICE Bit = 0, TQ1OPT1.TQ1IOE Bit = 1, TQ1OPT1.TQ1ID4 to TQ1OPT1.TQ1ID0 Bits = 00010: With Interrupt Culling) (2)



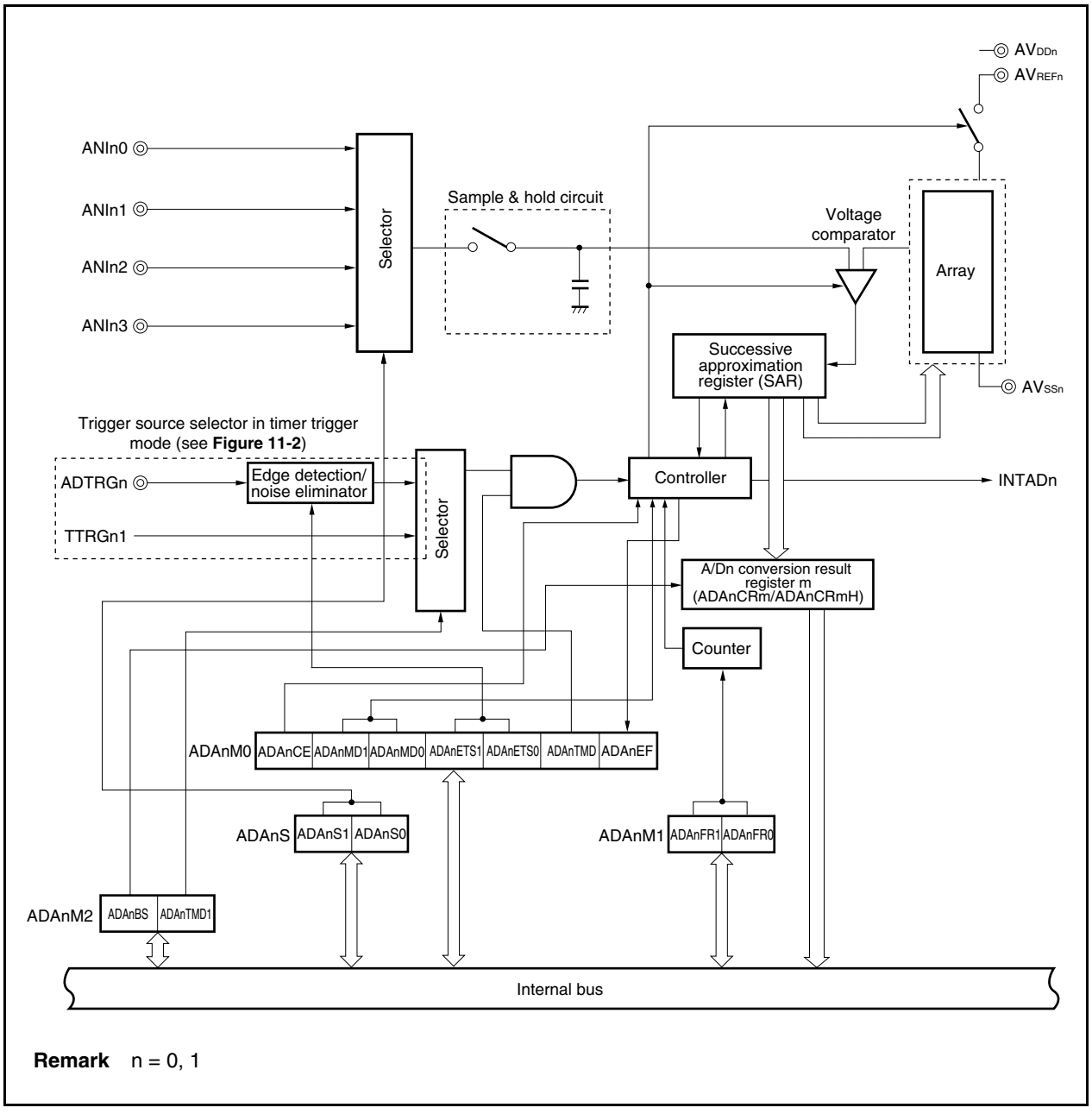
Caution The INTTQ1CC0 signal is culled but the INTTP1CC0 signal is not.

Remark : Culled interrupt

11.2 Configuration

The block diagram is shown below.

Figure 11-1. Block Diagram of A/D Converters 0 and 1



Remark n = 0, 1

11.9 Notes on Operation

11.9.1 Stopping conversion operation

When the ADAnM0.ADAnCE bit is cleared to 0 during a conversion operation, the conversion operation stops and the conversion results are not stored in A/Dn conversion result register m (ADAnCRm).

The ADAnCE bit is not cleared to 0 even after the A/Dn conversion end interrupt request signal (INTADn) has been generated in all modes.

Remark n = 0, 1, m = 0 to 3

11.9.2 Timer/external trigger interval

Make sure that the occurrence interval of the trigger in timer trigger mode or external trigger mode is longer than the total number of conversion clocks specified by the ADAnM1.ADAnFR1 and ADAnM1.ADAnFR0 bits (see **Table 11-2 Number of Conversion Clocks**).

(1) When 0 < trigger occurrence interval < total number of A/D conversion clocks

When the timer/external trigger is input during a conversion operation, the conversion operation is aborted and the conversion starts according to the last timer/external trigger input.

When conversion operations are aborted, the conversion results from the conversion operation immediately before are not stored in the ADAnCRm register. Note, therefore, that the generation of the INTADn signal and storing of the result in the ADAnCRm register are not guaranteed.

Remark n = 0, 1, m = 0 to 3

(2) When trigger occurrence interval ≥ total number of A/D conversion clocks

The INTADn signal is generated, and the value at the end of conversion is correctly stored in the ADAnCRm register. Design so that the trigger occurrence interval is equal or greater than the total number of A/D conversion clocks.

Remark n = 0, 1, m = 0 to 3

11.9.3 Operation in standby mode

(1) HALT mode

In this mode, A/D conversion continues.

(2) IDLE mode, STOP mode

As clock supply to A/D converters 0 and 1 is stopped, no conversion operations are performed.

When these modes are released by the maskable interrupt request signal input pin[Note], the ADAnM0, ADAnM1, ADAnM2, and ADAnS registers and A/Dn conversion result register m (ADAnCRm) hold their values. However, when the IDLE or STOP mode is set during a conversion operation, the conversion operation is suspended. At this time, if the mode released by the maskable interrupt request signal input pin[Note], the conversion operation resumes. At this time, the A/Dn conversion end interrupt request signal (INTADn) may be generated, but the conversion result written to the ADAnCRm register will be undefined.

Note INTP0 to INTP5

Remark n = 0, 1, m = 0 to 3

12.5.2 UART transmission

A high level is output to the TXDAn pin by setting the UAnCTL0.UAnPWR bit to 1.

Next, the transmission enabled status is set by setting the UAnCTL0.UAnTXE bit to 1, and transmission is started by writing transmit data to the UAnTX register. The start bit, parity bit, and stop bit are automatically added.

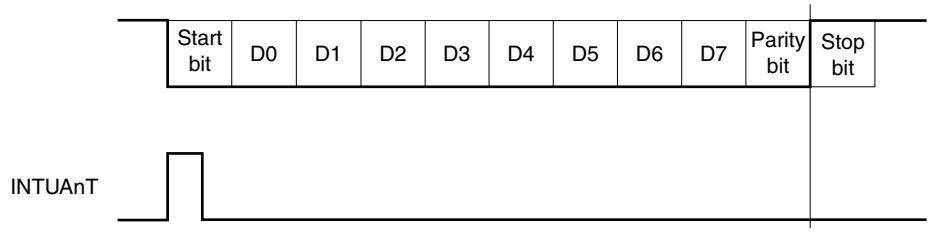
Since the CTS (transmit enable signal) input pin is not provided in UARTAn, use a port to check that reception is enabled at the transmit destination.

The data in the UAnTX register is transferred to the UARTAn transmit shift register upon the start of the transmit operation.

A transmission enable interrupt request signal (INTUAnT) is generated upon end of transmission of the data of the UAnTX register to the UARTAn transmit shift register, and thereafter the contents of the UARTAn transmit shift register are output to the TXDAn pin.

Write of the next transmit data to the UAnTX register is enabled by generating the INTUAnT signal.

Figure 12-3. UART Transmission



Remarks 1. LSB first

2. n = 0, 1

Table 14-1. Interrupt Source List (1/3)

Type	Classification	Default Priority	Name	Generating Source	Generating Unit	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Reset	Interrupt	–	RESET	$\overline{\text{RESET}}$ pin input	Pin	0000H	00000000H	Undefined	–
				WDT overflow (WDTRES)	WDT				
				Low-voltage detection (LVIRES)	POC/LVI				
Non-maskable	Interrupt	–	INTWDT	WDT overflow	WDT	0010H	00000010H	nextPC	–
Software exception	Exception	–	TRAP0n[Note 1]	TRAP instruction	–	004nH	00000040H	nextPC	–
	Exception	–	TRAP1n[Note 1]	TRAP instruction	–	005nH	00000050H	nextPC	–
Exception trap	Exception	–	ILGOP/ DBG0	Invalid instruction code/ DBTRAP instruction	–	0060H	00000060H	nextPC	–
Maskable	Interrupt	0	INTP0	INTP0 pin valid edge input	Pin	0080H	00000080H	nextPC	PIC0
	Interrupt	1	INTP1	INTP1 pin valid edge input	Pin	0090H	00000090H	nextPC	PIC1
	Interrupt	2	INTP2	INTP2 pin valid edge input	Pin	00A0H	000000A0H	nextPC	PIC2
	Interrupt	3	INTP3	INTP3 pin valid edge input	Pin	00B0H	000000B0H	nextPC	PIC3
	Interrupt	4	INTP4	INTP4 pin valid edge input	Pin	00C0H	000000C0H	nextPC	PIC4
	Interrupt	5	INTP5	INTP5 pin valid edge input	Pin	00D0H	000000D0H	nextPC	PIC5
	Interrupt	6	INTP6	INTP6 pin valid edge input	Pin	00E0H	000000E0H	nextPC	PIC6
	Interrupt	7	INTLVI	Low-voltage detection	POC/LVI	00F0H	000000F0H	nextPC	LVIIC
	Interrupt	–	–	Not used	–	–	00000100H	–	–
	Interrupt	–	–	Not used	–	–	00000110H	–	–
	Interrupt	8	INTTQ0OV	TMQ0 overflow	TMQ0	0120H	00000120H	nextPC	TQ0OVIC
	Interrupt	9	INTTQ0CC0	TQ0CCR0 capture input/ compare match	TMQ0	0130H	00000130H	nextPC	TQ0CCIC0
	Interrupt	10	INTTQ0CC1	TQ0CCR1 capture input/ compare match	TMQ0	0140H	00000140H	nextPC	TQ0CCIC1
	Interrupt	11	INTTQ0CC2	TQ0CCR2 capture input/ compare match	TMQ0	0150H	00000150H	nextPC	TQ0CCIC2
	Interrupt	12	INTTQ0CC3	TQ0CCR3 capture input/ compare match	TMQ0	0160H	00000160H	nextPC	TQ0CCIC3
	Interrupt	13	INTTQ1OV	TMQ1 overflow[Note 2]	TMQ1	0170H	00000170H	nextPC	TQ1OVIC
	Interrupt	14	INTTQ1CC0	TQ1CCR0 compare match[Note 3]	TMQ1	0180H	00000180H	nextPC	TQ1CCIC0
	Interrupt	15	INTTQ1CC1	TQ1CCR1 compare match	TMQ1	0190H	00000190H	nextPC	TQ1CCIC1
	Interrupt	16	INTTQ1CC2	TQ1CCR2 compare match	TMQ1	01A0H	000001A0H	nextPC	TQ1CCIC2
	Interrupt	17	INTTQ1CC3	TQ1CCR3 compare match	TMQ1	01B0H	000001B0H	nextPC	TQ1CCIC3
	Interrupt	–	–	Not used	–	–	000001C0H	–	–
	Interrupt	–	–	Not used	–	–	000001D0H	–	–

Notes 1. n is the value between 0 to FH.

2. When TMQ1 is used in the 6-phase PWM output mode, it functions as INTTQ1OV (valley interrupt) from the TMQ1 option (TMQOP1).

3. When TMQ1 is used in the 6-phase PWM output mode, it functions as INTTQ1CC0 (crest interrupt) from the TMQ1 option (TMQOP1).

After reset: FFFFH R/W Address: IMR3 FFFFF106H
IMR3L FFFFF106H, IMR3H FFFFF107H

	15	14	13	12	11	10	9	8
IMR3 (IMR3H[Note])	1	1	1	1	TM0EQMK0	1	AD1MK	AD0MK
	7	6	5	4	3	2	1	0
(IMR3L)	1	1	1	UA1TMK	UA1RMK	UA1REMK	CB0TMK	CB0RMK

After reset: FFFFH R/W Address: IMR2 FFFFF104H
IMR2L FFFFF104H, IMR2H FFFFF105H

	15	14	13	12	11	10	9	8
IMR2 (IMR2H[Note])	CB0REMK	UA0TMK	UA0RMK	UA0REMK	1	1	1	1
	7	6	5	4	3	2	1	0
(IMR2L)	TP3CCMK1	TP3CCMK0	TP3OVMK	TP2CCMK1	TP2CCMK0	TP2OVMK	TP1CCMK1	TP1CCMK0

After reset: FFFFH R/W Address: IMR1 FFFFF102H
IMR1L FFFFF102H, IMR1H FFFFF103H

	15	14	13	12	11	10	9	8
IMR1 (IMR1H[Note])	TP1OVMK	TP0CCMK1	TP0CCMK0	TP0OVMK	1	1	1	1
	7	6	5	4	3	2	1	0
(IMR1L)	1	1	1	1	TQ1CCMK3	TQ1CCMK2	TQ1CCMK1	TQ1CCMK0

After reset: FFFFH R/W Address: IMR0 FFFFF100H
IMR0L FFFFF100H, IMR0H FFFFF101H

	15	14	13	12	11	10	9	8
IMR0 (IMR0H[Note])	TQ1OVMK	TQ0CCMK3	TQ0CCMK2	TQ0CCMK1	TQ0CCMK0	TQ0OVMK	1	1
	7	6	5	4	3	2	1	0
(IMR0L)	LVIMK	PMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0

xxMKn	Interrupt mask flag setting
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note When reading/writing bits 15 to 8 of the IMR0 to IMR3 registers in 8-bit or 1-bit units, specify these bits as bits 7 to 0 of the IMR0H to IMR3H registers.

Caution Set bits 9 and 8 of the IMR0 register (bits 1 and 0 of the IMR0H register), bits 11 to 4 of the IMR1 register (bits 3 to 0 of the IMR1H register and bits 7 to 4 of the IMR1L register), bits 11 to 8 of the IMR2 register (bits 3 to 0 of the IMR2H register), bits 15 to 12, 10, and 7 to 5 of the IMR3 register (bits 7 to 4 and 2 of the IMR3H register and bits 7 to 5 of the IMR3L register) to 1. The operation when these settings are changed is not guaranteed.

Remark xx: Identification name of each peripheral unit (see **Table 14-2**)
n: Peripheral unit number (see **Table 14-2**)

(5/6)

Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SET1	bit#3,disp16[reg1]	00bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not (Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,1)	3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100000	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,1)	3 Note 3	3 Note 3	3 Note 3				×	
SHL	reg1,reg2	rrrrr111111RRRRR 0000000011000000	GR[reg2]←GR[reg2] logically shift left by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010110iiiii	GR[reg2]←GR[reg2] logically shift left by zero-extend(imm5)	1	1	1	×	0	×	×	
SHR	reg1,reg2	rrrrr111111RRRRR 0000000010000000	GR[reg2]←GR[reg2] logically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010100iiiii	GR[reg2]←GR[reg2] logically shift right by zero-extend(imm5)	1	1	1	×	0	×	×	
SLD.B	disp7[ep],reg2	rrrrr0110ddddddd	adr←ep+zero-extend(disp7) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.BU	disp4[ep],reg2	rrrrr0000110dddd **Note 18**	adr←ep+zero-extend(disp4) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.H	disp8[ep],reg2	rrrrr1000ddddddd **Note 19**	adr←ep+zero-extend(disp8) GR[reg2]←sign-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.HU	disp5[ep],reg2	rrrrr0000111dddd **Notes 18, 20**	adr←ep+zero-extend(disp5) GR[reg2]←zero-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.W	disp8[ep],reg2	rrrrr1010dddddd0 **Note 21**	adr←ep+zero-extend(disp8) GR[reg2]←Load-memory(adr,Word)	1	1	Note 9					
SST.B	reg2,disp7[ep]	rrrrr0111ddddddd	adr←ep+zero-extend(disp7) Store-memory(adr,GR[reg2],Byte)	1	1	1					
SST.H	reg2,disp8[ep]	rrrrr1001ddddddd **Note 19**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Halfword)	1	1	1					
SST.W	reg2,disp8[ep]	rrrrr1010ddddddd1 **Note 21**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Word)	1	1	1					
ST.B	reg2,disp16[reg1]	rrrrr111010RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Byte)	1	1	1					
ST.H	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd0 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory (adr,GR[reg2], Halfword)	1	1	1					
ST.W	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory (adr,GR[reg2], Word)	1	1	1					
STSR	regID,reg2	rrrrr111111RRRRR 0000000001000000	GR[reg2]←SR[regID]	1	1	1					

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