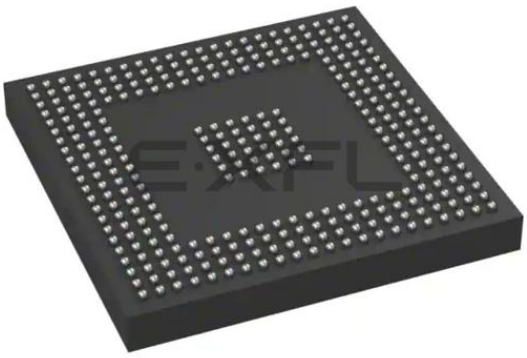
Renesas Electronics America Inc - R7S721011VLBG#AC0 Datasheet



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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DVD, VDC
Ethernet	10/100Mbps (1), 100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.2V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	324-FBGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7s721011vlbg-ac0

(2/2)

Pin Name	Pin No.	I/O	Function	Alternate Function
TIP00	37	Input	External event count input/external trigger input/capture trigger input of TMP0	TOP00/P43
TIP01	36		Capture trigger input of TMP0	TOP01/P44
TIP20	19		External event count input/external trigger input/capture trigger input of TMP2	TOQ00 (CLMER)[Note]/ P16 (CLMER)[Note]
TIP21	18		Capture trigger input of TMP2	TOP21/P17
TIQ00	21	Input	Capture trigger input of TMQ0	P13
TIQ01	24			TOQH01/TOQ01/P10
TIQ02	23			TOQ02/P11
TIQ03	22			TOQH02/TOQ03/P12
TOP00	37	Output	Pulse signal output of TMP0, TMP2	TIP00/P43
TOP01	36			TIP01/P44
TOP21	18			TIP21/P17
TOP2OFF	15	Input	High-impedance output control signal input	INTP2/P02
TOP31	45	Output	Pulse signal output of TMP3	P27
TOP3OFF	14	Input	High-impedance output control signal input	INTP3/P03
TOQ00 (CLMER)[Note]	19	Output	Pulse signal output of TMQ0	TIP20/P16 (CLMER)[Note]
TOQ01	24			TOQH01/TIQ01/P10
TOQ02	23			TIQ02/P11
TOQ03	22			TOQH02/TIQ03/P12
TOQ10	46	Output	Pulse signal output of TMQ1	P26
TOQ1B1	53	Output	Pulse signal output for 6-phase PWM	P21
TOQ1B2	51			P23
TOQ1B3	49			P25
TOQ1OFF	16	Input	High-impedance output control signal input	INTP1/P01
TOQ1T1	54	Output	Pulse signal output for 6-phase PWM	P20
TOQ1T2	52			P22
TOQ1T3	50			P24
TOQH01	24	Output	High-impedance output by TMQ0 pulse signal output and valid edge of TOQH0OFF pin input	TIQ01/TOQ01/P10
TOQH02	22			TIQ03/TOQ03/P12
TOQH03	20			EVTQ0/P14
TOQH0OFF	17	Input	High-impedance output control signal input	INTP0/P00
TXDA0	43	Output	Serial transmit data output of UARTA0, UARTA1	P31
TXDA1	41			P33
V_{DD}	9	–	Positive power supply for internal unit	–
V_{SS}	8	–	Ground potential for internal unit	–
X1	6	Input	Resonator connection pin for system clock	–
X2	7	–		–

Note The CLMER signal is enabled only when P16 is specified as an output port or the output function of TOQ00. When an error (oscillator stop) is detected by the clock monitor, a low level is forcibly output. Low-level output is released by reset signal. For details, see **Table 4-5 Alternate-Function Pins of Port 1**.

(f) Setting of alternate function of port 1

PFC17	Specification of alternate function of P17 pin
0	TOP21 output
1	TIP21 input

PFC16	Specification of alternate function of P16 pin
0	TOQ00 (CLMER) output[Note 1]
1	TIP20 input

PFC14	Specification of alternate function of P14 pin
0	TOQH03 output[Note 2]
1	EVTQ0 input

PFC13	Specification of alternate function of P13 pin
0	Setting prohibited
1	TIQ00 input

PFCE12	PFC12	Specification of alternate function of P12 pin
0	0	TOQH02 output[Note 2]
0	1	TIQ03 input
1	0	TOQ03 output
1	1	Setting prohibited

PFCE11	PFC11	Specification of alternate function of P11 pin
0	0	Setting prohibited
0	1	TIQ02 input
1	0	TOQ02 output
1	1	Setting prohibited

PFCE10	PFC10	Specification of alternate function of P10 pin
0	0	TOQH01 output[Note 2]
0	1	TIQ01 input
1	0	TOQ01 output
1	1	Setting prohibited

Notes 1. If P16 is used as the TOQ00 output pin, when an error (oscillator stop) is detected by the clock monitor, the CLMER signal (low level) is output from P16. Low-level output is released by reset signal. For details, see **Table 4-5 Alternate-Function Pins of Port 1**.

2. These are setting prohibited when TMQ0 is in other than PWM output mode.

Figure 4-6. Block Diagram of P11 Pin

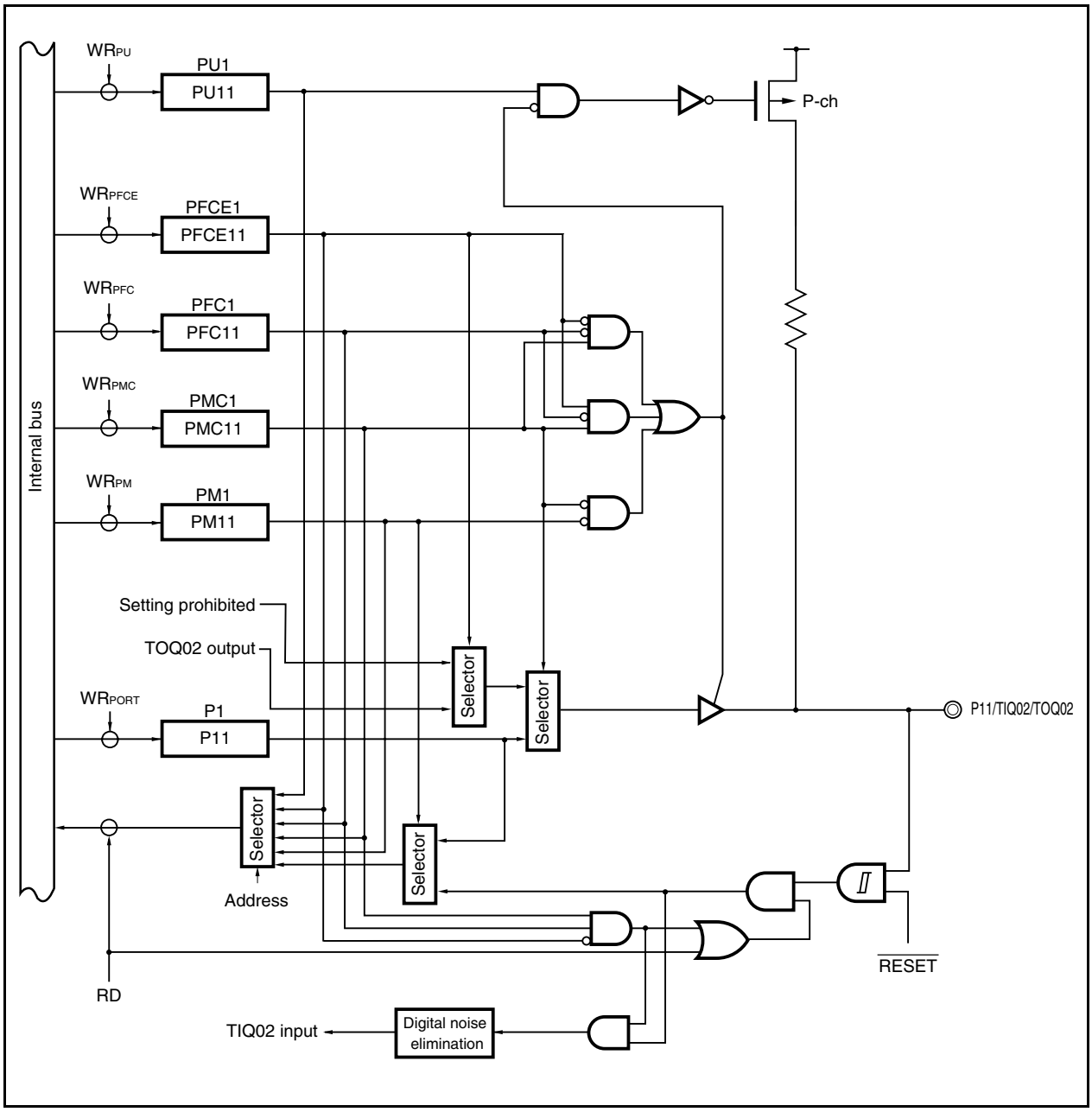
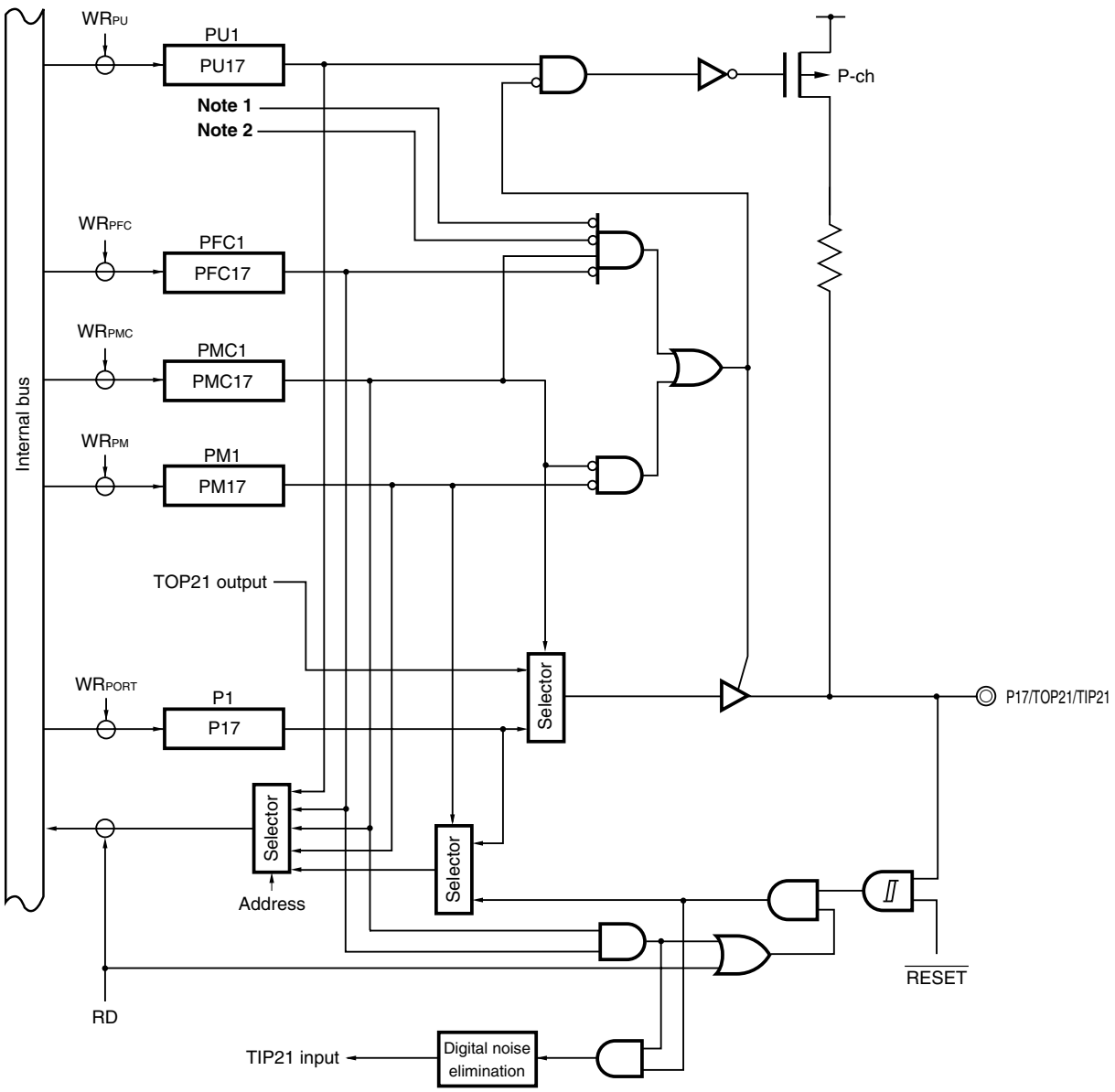


Figure 4-10. Block Diagram of P17 Pin



Notes 1. Output of high impedance setting signal from high impedance output controller

2. Output of clock stop detection signal from clock monitor

(1) Registers

(a) Port 2 register (P2)

After reset: Undefined R/W Address: FFFFF404H

	7	6	5	4	3	2	1	0
P2	P27	P26	P25	P24	P23	P22	P21	P20

P2n	Control of output data (in output mode) (n = 0 to 7)
0	Output 0.
1	Output 1.

(b) Port 2 mode register (PM2)

After reset: FFH R/W Address: FFFFF424H

	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

PM2n	Control of input/output mode (in port mode) (n = 0 to 7)
0	Output mode
1	Input mode

(e) Pull-up resistor option register 4 (PU4)

After reset: 00H R/W Address: FFFFFC48H

	7	6	5	4	3	2	1	0
PU4	0	0	0	PU44	PU43	PU42	PU41	PU40

PU4n	Control of on-chip pull-up resistor connection (n = 0 to 4)
0	Do not connect
1	Connect[Note]

Note An on-chip pull-up resistor can be connected only when the pins are in input mode in the port mode or when the pins function as input pins in the alternate-function mode (including when in the $\overline{\text{SCKB0}}$ pin slave mode). The resistor cannot be connected when the pin is in the output state.

(5) TMPk I/O control register 2 (TPkIOC2)

The TPkIOC2 register is an 8-bit register that controls the valid edge for the external event count input signal (TIPk0 pin) and external trigger input signal (TIPk0 pin).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

Remark TMP1 and TMP3 do not have the TP1IOC2 and TP3IOC2 registers.

After reset: 00H R/W Address: TP0IOC2 FFFFF644H, TP2IOC2 FFFFF684H

	7	6	5	4	3	2	1	0
TPkIOC2	0	0	0	0	TPkEES1	TPkEES0	TPkETS1	TPkETS0

(k = 0, 2)

TPkEES1	TPkEES0	External event count input signal (TIPk0 pin) valid edge setting
0	0	No edge detection (external event count invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

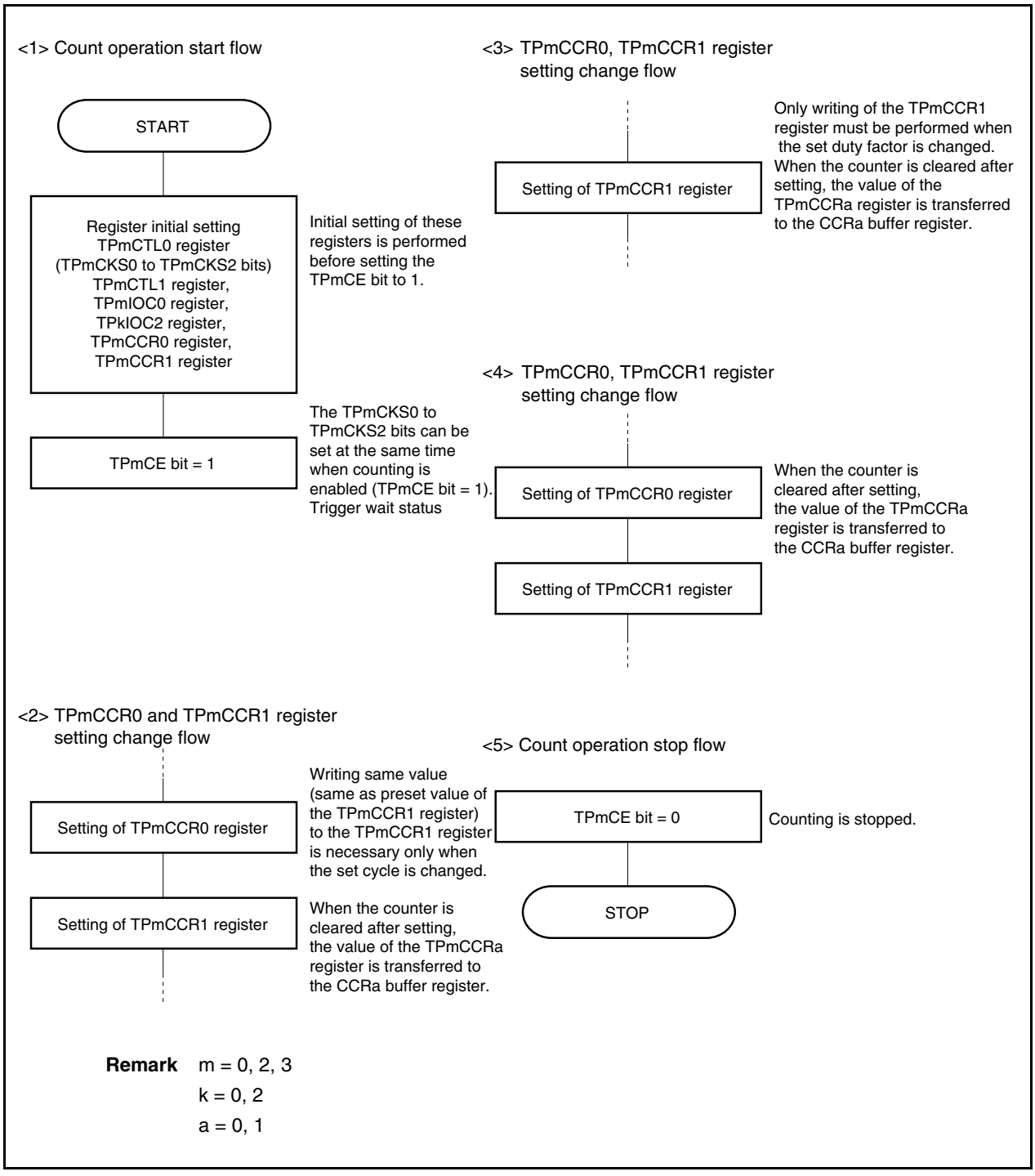
TPkETS1	TPkETS0	External trigger input signal (TIPk0 pin) valid edge setting
0	0	No edge detection (external trigger invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

Cautions 1. Rewrite the TPkEES1, TPkEES0, TPkETS1, and TPkETS0 bits when the TPkCTL0.TPkCE bit = 0. (The same value can be written when the TPkCE bit = 1.) If rewriting was mistakenly performed, clear the TPkCE bit to 0 and then set the bits again.

2. The TPkEES1 and TPkEES0 bits are valid only when the TPkCTL1.TPkEEE bit = 1 or when the external event count mode (TPkCTL1.TPkMD2 to TPkCTL1.TPkMD0 bits = 001) has been set.

3. The TPkETS1 and TPkETS0 bits are valid only in the external trigger pulse output mode or one-shot pulse output mode.

Figure 6-26. Software Processing Flow in External Trigger Pulse Output Mode (2/2)



Remark m = 0, 2, 3
k = 0, 2
a = 0, 1

(a) Function as compare register

The TQnCCR1 register can be rewritten even when the TQnCTL0.TQnCE bit = 1.

The set value of the TQnCCR1 register is transferred to the CCR1 buffer register. When the value of the 16-bit counter matches the value of the CCR1 buffer register, a compare match interrupt request signal (INTTQnCC1) is generated. If TOQ01/TOQH01 pin output is enabled at this time, the output of the TOQ01/TOQH01 pin is inverted (the TOQ11 and TOQH11 pins are not provided).

The compare register is not cleared by the TQnCTL0.TQnCE bit = 0.

(b) Function as capture register (TQ0CCR1 register only)

When the TQ0CCR1 register is used as a capture register in the free-running timer mode, the count value of the 16-bit counter is stored in the TQ0CCR1 register if the valid edge of the capture trigger input pin (TIQ01 pin) is detected. In the pulse width measurement mode, the count value of the 16-bit counter is stored in the TQ0CCR1 register and the 16-bit counter is cleared (0000H) if the valid edge of the capture trigger input pin (TIQ01 pin) is detected.

Even if the capture operation and reading the TQ0CCR1 register conflict, the correct value of the TQ0CCR1 register can be read.

The capture register is cleared by the TQ0CTL0.TQ0CE bit = 0.

The following table shows the functions of the capture/compare register in each mode, and how to write data to the compare register.

Table 7-5. Function of Capture/Compare Register in Each Mode and How to Write Compare Register

Operation Mode	Capture/Compare Register	How to Write Compare Register
Interval timer	Compare register	Anytime write
External event counter[Note 1]	Compare register	Anytime write
External trigger pulse output[Notes 1, 2]	Compare register	Batch write[Note 3]
One-shot pulse output[Notes 1, 2]	Compare register	Anytime write
PWM output[Note 1]	Compare register	Batch write[Note 3]
Free-running timer	Capture/compare register	Anytime write
Pulse width measurement[Note 1]	Capture register	None

Notes 1. TMQ0 only

2. This mode can be set only with the software trigger. No external trigger input pin is available.

3. Writing to the TQ0CCR1 register is the trigger.

Remark For anytime write and batch write, see **7.6 (2) Anytime write and batch write**.

7.5 Timer Output Operations

The following table shows the operations and output levels of the TOQ00 to TOQ03, TOQ10, and TOQH01 to TOQH03 pins.

Table 7-8. Timer Output Control in Each Mode

Operation Mode	TOQn0 Pin	TOQ01 to TOQ03 Pins	TOQH01 to TOQH03 Pins
Interval timer mode	PWM output		None
External event count mode	None		
External trigger pulse output mode	PWM output[Note]	External trigger pulse output	None
One-shot pulse output mode		One-shot pulse output	
PWM output mode		PWM output	
Free-running timer mode	PWM output (only when compare function is used)		None
Pulse width measurement mode	None		

Note TOQ00 pin only

Remark n = 0, 1

Table 7-9. Truth Table of TOQ00 to TOQ03, TOQ10, and TOQH01 to TOQH03 Pins Under Control of Timer Output Control Bits

TQnIOC0.TQnOLa Bit	TQnIOC0.TQnOEa Bit	TQnCTL0.TQnCE Bit	Level of TOQna and TOQH1b Pins
0	0	×	Low-level output
	1	0	Low-level output
		1	Low level immediately before counting, high level after counting is started
1	0	×	High-level output
	1	0	High-level output
		1	High level immediately before counting, low level after counting is started

Remark a = 0 to 3 when n = 0
a = 0 when n = 1
b = 1 to 3

16-bit timer/event counter Q waits for a trigger when the TQ0CE bit is set to 1. When the trigger is generated, the 16-bit counter is cleared from FFFFH to 0000H, starts counting at the same time, and outputs a PWM waveform from the TOQ0b pin. If the trigger is generated again while the counter is operating, the counter is cleared to 0000H and <R> restarted. (The output of the TOQ00 pin is inverted. The TOQ0b pin outputs high level regardless of the status (high/low) when a trigger occurs.)

The active level width, cycle, and duty factor of the PWM waveform can be calculated as follows.

Active level width = (Set value of TQ0CCRb register) × Count clock cycle
Cycle = (Set value of TQ0CCR0 register + 1) × Count clock cycle
Duty factor = (Set value of TQ0CCRb register)/(Set value of TQ0CCR0 register + 1)

The compare match interrupt request signal INTTQ0CC0 is generated when the 16-bit counter counts next time after its count value matches the value of the CCR0 buffer register, and the 16-bit counter is cleared to 0000H. The compare match interrupt request signal INTTQ0CCb is generated when the count value of the 16-bit counter matches the value of the CCRb buffer register.

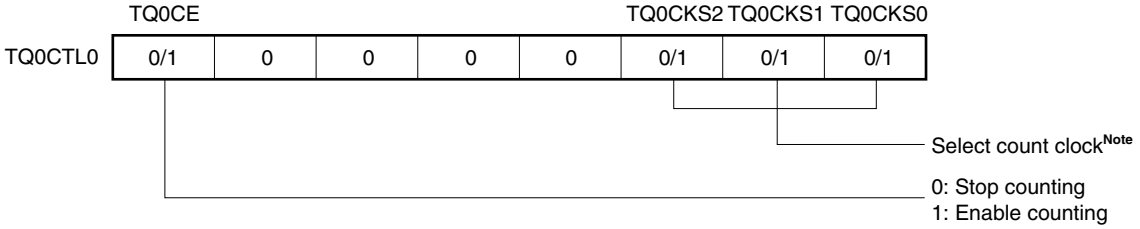
The value set to the TQ0CCRa register is transferred to the CCRa buffer register when the count value of the 16-bit counter matches the value of the CCRa buffer register and the 16-bit counter is cleared to 0000H.

Only setting the software trigger (TQ0CTL1.TQ0EST bit) to 1 is used as the trigger.

Remark a = 0 to 3
b = 1 to 3

Figure 7-24. Setting of Registers in External Trigger Pulse Output Mode (1/3)

(a) TMQ0 control register 0 (TQ0CTL0)



Note The setting is invalid when the TQ0CTL1.TQ0EEE bit = 1.

To transfer data from the TQ0CCRa register to the CCRa buffer register, the TQ0CCR1 register must be written.

To change both the cycle and active level of the PWM waveform at this time, first set the cycle to the TQ0CCR0 register, set the active level width to the TQ0CCR2 and TQ0CCR3 registers, and then set an active level width to the TQ0CCR1 register.

To change only the cycle of the PWM waveform, first set a cycle to the TQ0CCR0 register, and then write the same value (same as preset value of the TQ0CCR1 register) to the TQ0CCR1 register.

To change only the active level width (duty factor) of PWM wave, first set the active level to the TQ0CCR2 and TQ0CCR3 registers, and then set an active level to the TQ0CCR1 register.

To change only the active level width (duty factor) of the PWM waveform output by the TOQ01 (TOQH01) pin, only the TQ0CCR1 register has to be set.

To change only the active level width (duty factor) of the PWM waveform output by the TOQ02 (TOQH02) and TOQ03 (TOQH03) pins, first set an active level width to the TQ0CCR2 and TQ0CCR3 registers, and then write the same value (same as preset value of the TQ0CCR1 register) to the TQ0CCR1 register.

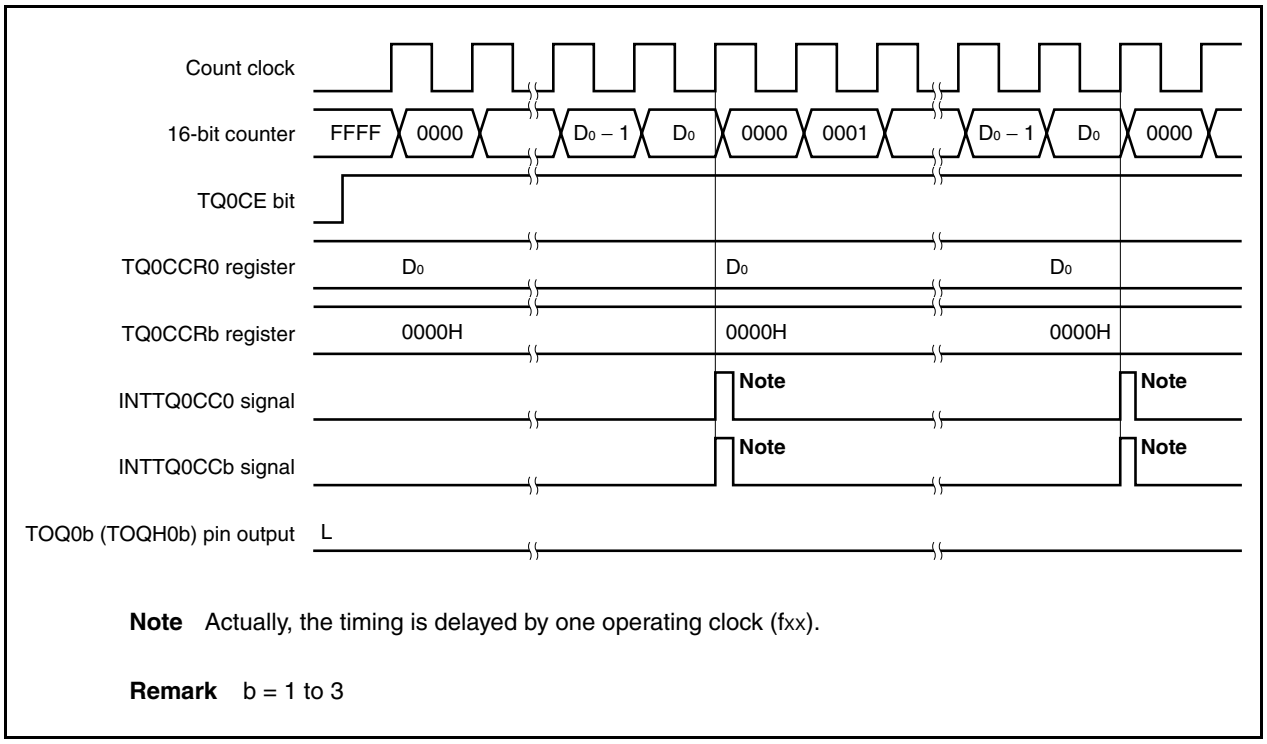
After the TQ0CCR1 register is written, the value written to the TQ0CCRa register is transferred to the CCRa buffer register in synchronization with the timing of clearing the 16-bit counter, and is used as a value to be compared with the value of the 16-bit counter.

To write the TQ0CCR0 to TQ0CCR3 registers again after writing the TQ0CCR1 register once, do so after the INTTQ0CC0 signal is generated. Otherwise, the value of the CCRa buffer register may become undefined because the timing of transferring data from the TQ0CCRa register to the CCRa buffer register conflicts with writing the TQ0CCRa register.

Remark a = 0 to 3

(b) 0%/100% output of PWM waveform

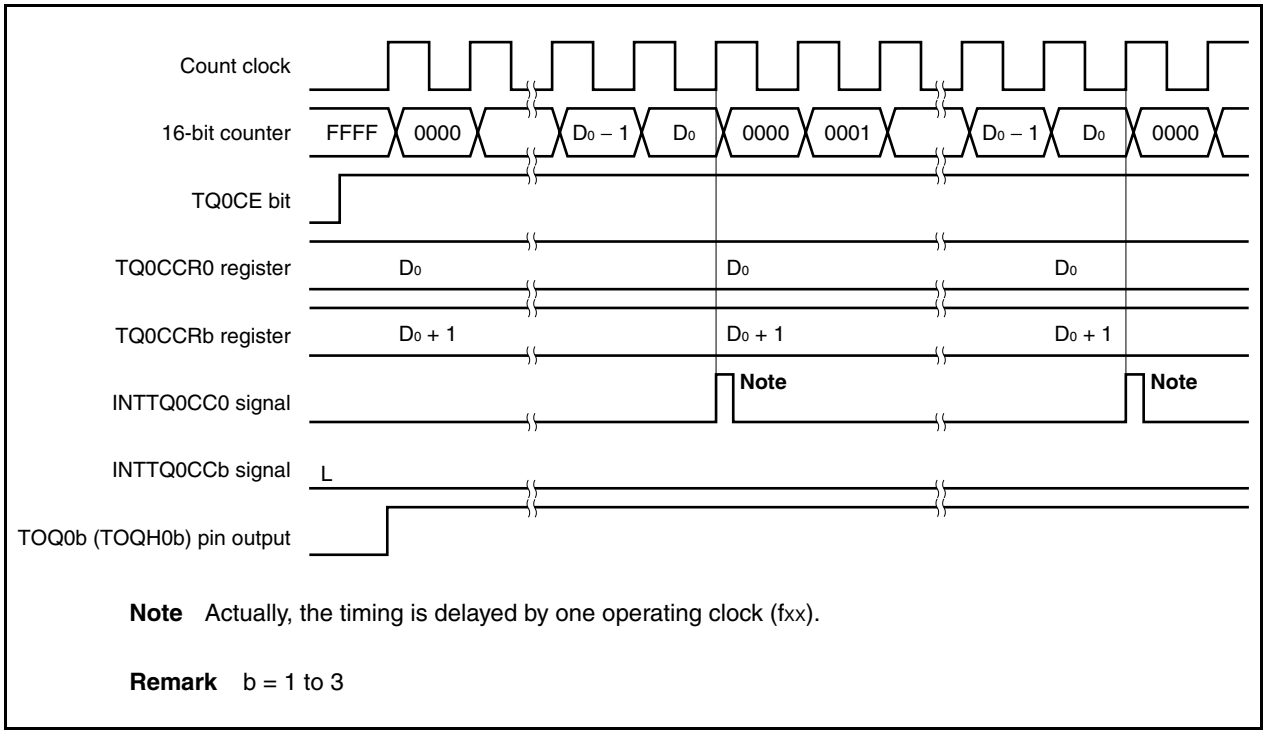
To output a 0% waveform, set the TQ0CCRb register to 0000H. The 16-bit counter is cleared to 0000H and the INTTQ0CC0 and INTTQ0CCb signals are generated at the next timing after a match between the count value of the 16-bit counter and the value of the CCR0 buffer register.



Note Actually, the timing is delayed by one operating clock (fxx).

Remark b = 1 to 3

To output a 100% waveform, set a value of (set value of TQ0CCR0 register + 1) to the TQ0CCRb register. If the set value of the TQ0CCR0 register is FFFFH, 100% output cannot be produced.



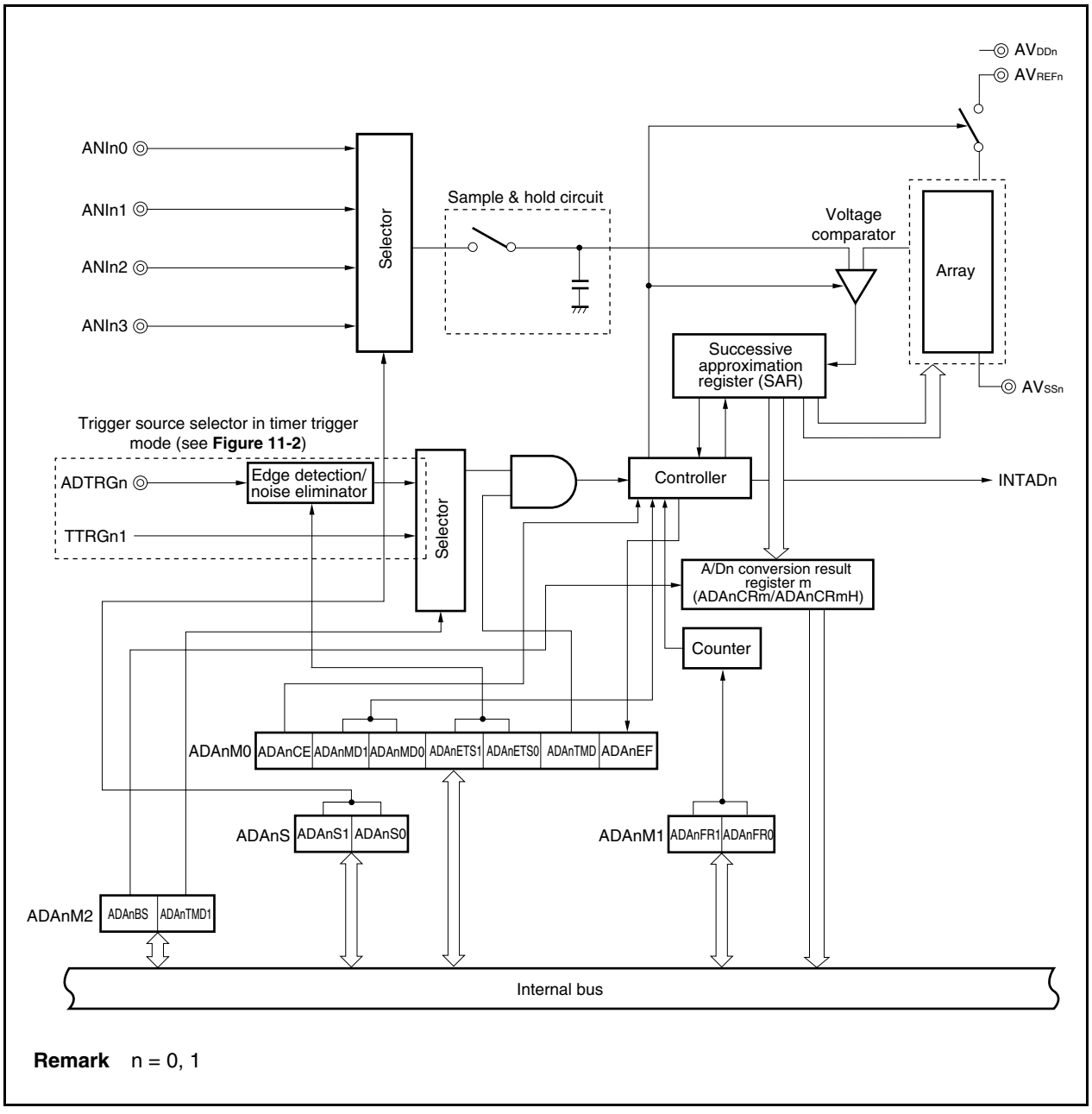
Note Actually, the timing is delayed by one operating clock (fxx).

Remark b = 1 to 3

11.2 Configuration

The block diagram is shown below.

Figure 11-1. Block Diagram of A/D Converters 0 and 1



Remark n = 0, 1

(5) Successive approximation register (SAR)

The SAR is a 10-bit register that sets voltage tap data whose values from the array match the voltage values of the analog input pins, 1 bit at a time starting from the most significant bit (MSB).

If data is set in the SAR all the way to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR (conversion results) are held in A/Dn conversion result registers 0 to 3 (ADAnCR0 to ADAnCR3) (n = 0, 1). When all the specified A/D conversion operations have ended, an A/Dn conversion end interrupt request signal (INTADn) is generated.

(6) A/Dn conversion result registers 0 to 3 (ADAnCR0 to ADAnCR3), A/Dn conversion result registers 0H to 3H (ADAnCR0H to ADAnCR3H) (n = 0, 1)

The ADAnCR0 to ADAnCR3 and ADAnCR0H to ADAnCR3H registers are registers that hold the A/D conversion results. Each time A/D conversion ends, the conversion result is loaded from the successive approximation register (SAR) and stored in the higher 10 bits of the ADAnCR0 to ADAnCR3 registers. The lower 6 bits of these registers are always 0 when read.

The higher 8 bits of the result of A/D conversion are read from the ADAnCR0H to ADAnCR3H registers. To read the result of A/D conversion in 16-bit units, specify the ADAnCR0 to ADAnCR3 registers. To read the higher 8 bits, specify the ADAnCR0H to ADAnCR3H registers.

(7) A/D converter n mode register 0 (ADAnM0) (n = 0, 1)

This register is used to specify the operation mode and controls the conversion operation.

(8) A/D converter n mode register 1 (ADAnM1) (n = 0, 1)

This register is used to set the number of conversion clocks of the analog input to be A/D converted.

(9) A/D converter n channel specification register (ADAnS) (n = 0, 1)

This register is used to specify the analog input pin to be A/D converted.

(10) A/D converter n mode register 2 (ADA2M2) (n = 0, 1)

This register is used to specify the buffer mode and specify the mode in the hardware trigger mode.

(11) ANIn0 to ANIn3 pins (n = 0, 1)

The ANIn0 to ANIn3 pins are analog input pins for A/D converters 0 and 1. They input the analog signals to be A/D converted.

Caution Make sure that the voltages input to ANIn0 to ANIn3 do not exceed the rated values. If a voltage higher than or equal to AV_{REFn} or lower than or equal to AV_{SSn} (even within the range of the absolute maximum ratings) is input to a channel, the conversion value of the channel is undefined, and the conversion values of the other channels may also be affected.

(12) AV_{REF0} and AV_{REF1} pins

This is the pin for inputting the reference voltage of A/D converters 0 and 1. It converts signals input to the ANIn0 to ANIn3 pins to digital signals based on the voltage applied between AV_{REFn} and AV_{SSn} (n= 0, 1). Always make the potential at the AV_{REFn} pin the same as that at the EV_{DD} pin even when A/D converters 0 and 1 are not used.

The operating voltage range of the AV_{REFn} pin is $V_{DD} = EV_{DD} = AV_{DDn} = AV_{REFn}$ = 4.5 to 5.5 V.

(2) 4-buffer mode (4 buffers of continuous select/one-shot select by external trigger)

In this mode, the voltage of one analog input pin (ANInm) is A/D converted four times using the ADTRGn signal as a trigger and the results are stored in the ADAnCRm register (n = 0, 1, m = 0 to 3).

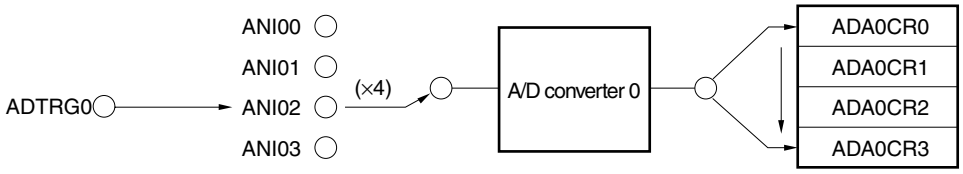
The A/Dn conversion end interrupt request signal (INTADn) is generated when the four A/D conversions end. After the end of A/D conversion, the A/D converter waits for a trigger.

This mode is suitable for applications in which the average of the A/D conversion results is calculated.

Analog Input Pin	A/D Conversion Result Register
ANInm	ADAnCR0
ANInm	ADAnCR1
ANInm	ADAnCR2
ANInm	ADAnCR3

Remark n = 0, 1
m = 0 to 3

Figure 11-20. Example of 4-Buffer Mode Operation (4 Buffers of Continuous Select/One-Shot Select by External Trigger)



(1) The ADA0CE bit = 1 (enable)
(2) The external trigger signal (ADTRG0) is generated
(3) The ANI02 pin is A/D converted
(4) The conversion result is stored in the ADA0CR0 register
(5) The ANI02 pin is A/D converted
(6) The conversion result is stored in the ADA0CR1 register
(7) The ANI02 pin is A/D converted
(8) The conversion result is stored in the ADA0CR2 register
(9) The ANI02 pin is A/D converted
(10) The conversion result is stored in the ADA0CR3 register
(11) The ADA0M0.ADA0EF bit = 0
(12) The INTAD0 interrupt request signal is generated
(13) If next trigger is input, return to (3)
(14) To end the conversion, the ADA0CE bit = 0 (stop)

Remark This is an operation example with the following setting.
ADA0M0.ADA0MD1 and ADA0M0.ADA0MD0 bits = 00 or 10, ADA0M0.ADA0TMD bit = 1,
ADA0M2.ADA0BS bit = 1, ADA0M2.ADA0TMD1 bit = 0,
ADA0S.ADA0S1 and ADA0S.ADA0S0 bit = 10

12.5.2 UART transmission

A high level is output to the TXDAn pin by setting the UAnCTL0.UAnPWR bit to 1.

Next, the transmission enabled status is set by setting the UAnCTL0.UAnTXE bit to 1, and transmission is started by writing transmit data to the UAnTX register. The start bit, parity bit, and stop bit are automatically added.

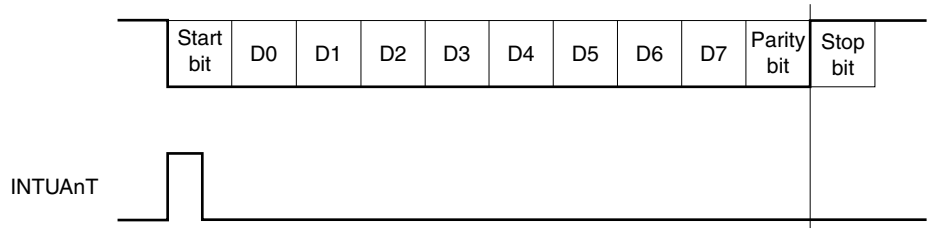
Since the CTS (transmit enable signal) input pin is not provided in UARTAn, use a port to check that reception is enabled at the transmit destination.

The data in the UAnTX register is transferred to the UARTAn transmit shift register upon the start of the transmit operation.

A transmission enable interrupt request signal (INTUAnT) is generated upon end of transmission of the data of the UAnTX register to the UARTAn transmit shift register, and thereafter the contents of the UARTAn transmit shift register are output to the TXDAn pin.

Write of the next transmit data to the UAnTX register is enabled by generating the INTUAnT signal.

Figure 12-3. UART Transmission

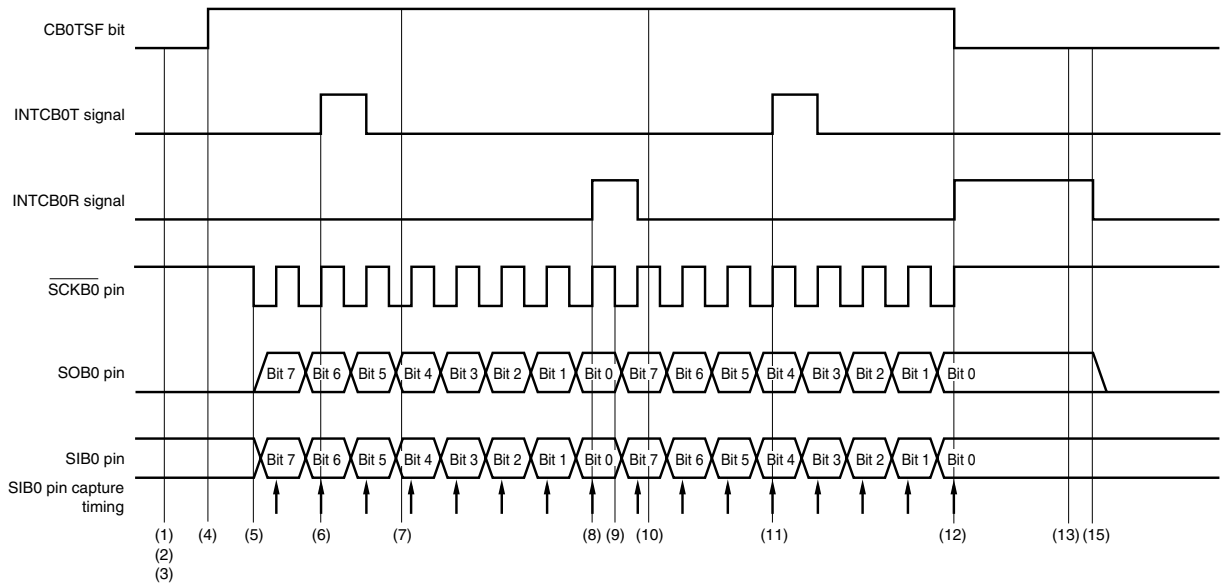


Remarks 1. LSB first

2. n = 0, 1

(2) Operation timing

(1/2)



(1) Write 07H to the CB0CTL1 register, and select communication type 1, communication clock (f_{CCLK}) = external clock ($\overline{SCKB0}$), and slave mode.

(2) Write 00H to the CB0CTL2 register, and set the transfer data length to 8 bits.

(3) Write E3H to the CB0CTL0 register, and select the transmission/reception mode, MSB first, and continuous transfer mode at the same time as enabling the operation of the communication clock (f_{CCLK}).

(4) The CB0STR.CB0TSF bit is set to 1 by writing the transmit data to the CB0TX register, and the device waits for a serial clock input.

(5) When a serial clock is input, output the transmit data to the SOB0 pin in synchronization with the serial clock, and capture the receive data of the SIB0 pin.

(6) When transfer of the transmit data from the CB0TX register to the shift register is completed and writing to the CB0TX register is enabled, the transmission enable interrupt request signal (INTCB0T) is generated.

(7) To continue transmission, write the transmit data to the CB0TX register again after the INTCB0T signal is generated.

(8) When reception of the transfer data length set with the CB0CTL2 register is completed, the reception end interrupt request signal (INTCB0R) is generated, and reading of the CB0RX register is enabled.

(9) When a serial clock is input continuously, continuous transmission/reception is started.

(10) Read the CB0RX register.

(11) When transfer of the transmit data from the CB0TX register to the shift register is completed and writing to the CB0TX register is enabled, the INTCB0T signal is generated. To end continuous transmission/reception with the current transmission/reception, do not write to the CB0TX register.

15.5 STOP Mode

15.5.1 Setting and operation status

The STOP mode is set by setting (1) the PSMR.PSM0 bit and setting (1) the PSC.STB bit in the normal operation mode.

In the STOP mode, the clock generator stops operation. Clock supply to the CPU and the on-chip peripheral functions is stopped.

As a result, program execution is stopped, and the contents of the internal RAM before the STOP mode was set <R> are retained. The CPU and other on-chip peripheral functions stop operating. The on-chip peripheral functions that can operate with an external clock continue operating.

Table 15-7 shows the operation status in the STOP mode.

Because the STOP mode stops operation of the clock generator, it reduces the power consumption to a level lower than the IDLE mode. The power consumption is therefore minimized with only leakage current flowing if the external clock is not used.

Caution Insert five or more NOP instructions after the instruction that stores data in the PSC register to set the STOP mode.

15.5.2 Releasing STOP mode

The STOP mode is released by an unmasked external interrupt request signal (INTP0 to INTP5 pin input), unmasked internal interrupt request signal (INTLVI), unmasked internal interrupt request signal from the peripheral functions operable in the STOP mode (interrupt request signal related to CSIB in the slave mode), or reset signal ($\overline{\text{RESET}}$ pin input, reset signal generation by low-voltage detection (LVIRES), and reset signal generation by power-on clear (POCRES)).

After the STOP mode has been released, the normal operation mode is restored after the oscillation stabilization time has been secured.

(1) Releasing STOP mode by unmasked maskable interrupt request signal

The STOP mode is released by an unmasked maskable interrupt request signal, regardless of the priority of the interrupt request. If the STOP mode is set in an interrupt servicing routine, however, an interrupt request that is issued later is serviced as follows.

Caution When the PSC.INTM bit is set to 1, the STOP mode cannot be released by an unmasked maskable interrupt request signal.

(a) If an interrupt request signal with a priority lower than or same as the interrupt request signal currently being serviced is generated, the STOP mode is released, but the newly generated interrupt request signal is not acknowledged. The interrupt request signal itself is retained. Therefore, execution starts at the next instruction after the STOP instruction.

(b) If an interrupt request signal with a priority higher than that of the interrupt request signal currently being serviced is issued, the STOP mode is released and that interrupt request signal is acknowledged. Therefore, the execution branches to the handler address.

Table 18-6. Wiring of V850ES/IE2 Flash Writing Adapters (FA-64GC-8BS-A)

<R>

Flash Memory Programmer (PG-FP4 and PG-FP5) Connection Pin			Name of FA Board Pin	CSIB0 + HS Used		CSIB0 Used		UARTA0 Used	
Signal Name	I/O	Pin Function		Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SI/RxD	Input	Receive signal	SI	P41/SOB0	39	P41/SOB0	39	P31/TXDA0	43
SO/TxD	Output	Transmit signal	SO	P40/SIB0	40	P40/SIB0	40	P30/RXDA0	44
SCK	Output	Transfer clock	SCK	P42/$\overline{\text{SCKB0}}$	38	P42/$\overline{\text{SCKB0}}$	38	Not needed	–
CLK[Note]	Output	Clock to V850ES/IE2	X1[Note]	X1[Note]	6	X1[Note]	6	X1[Note]	6
			X2[Note]	X2[Note]	7	X2[Note]	7	X2[Note]	7
/RESET	Output	Reset signal	/RESET	$\overline{\text{RESET}}$	5	$\overline{\text{RESET}}$	5	$\overline{\text{RESET}}$	5
FLMD0	Input	Write voltage	FLMD0	FLMD0	25	FLMD0	25	FLMD0	25
FLMD1	Input	Write voltage	FLMD1	PDL5/FLMD1	30	PDL5/FLMD1	30	PDL5/FLMD1	30
HS	Input	Handshake signal for CSI0 + HS	RESERVE/ HS	P43/TOP00/ TIP00	37	Not needed	–	Not needed	–
VDD	–	VDD voltage generation/ voltage monitor	VDD	V_{DD}	9	V_{DD}	9	V_{DD}	9
				EV_{DD}	26, 47	EV_{DD}	26, 47	EV_{DD}	26, 47
				AV_{REF0}	64	AV_{REF0}	64	AV_{REF0}	64
				AV_{REF1}	59	AV_{REF1}	59	AV_{REF1}	59
				AV_{DD0}	63	AV_{DD0}	63	AV_{DD0}	63
				AV_{DD1}	60	AV_{DD1}	60	AV_{DD1}	60
GND	–	Ground	GND	V_{SS}	8	V_{SS}	8	V_{SS}	8
				EV_{SS}	27, 48	EV_{SS}	27, 48	EV_{SS}	27, 48
				AV_{SS0}	62	AV_{SS0}	62	AV_{SS0}	62
				AV_{SS1}	61	AV_{SS1}	61	AV_{SS1}	61

Note The clock cannot be supplied from the CLK pin of the flash memory programmer. Create an oscillator on the board and supply the clock via that oscillator.

Caution Be sure to connect the REGC pin in either of the following ways.

- **Connect to GND via 4.7 μF capacitor**
- **Connect directly to V_{DD}**