Renesas Electronics America Inc - UPD70F3714GC-8BS-A Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, UART/USART
Peripherals	LVD, PWM, WDT
Number of I/O	39
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3714gc-8bs-a

3.2.2 System register set

System registers control the status of the CPU and hold interrupt information.

Read from and write to system registers are performed by setting the system register numbers shown below with the system register load/store instructions (LDSR, STSR instructions).

Table 3-2. System Register Numbers

System Register No.	System Register Name	Operand Specification Enabled	
		LDSR Instruction	STSR Instruction
0	Interrupt status saving register (EIPC)[Note 1]	Yes	Yes
1	Interrupt status saving register (EIPSW)[Note 1]	Yes	Yes
2	NMI status saving register (FEPC)	Yes	Yes
3	NMI status saving register (FEPSW)	Yes	Yes
4	Interrupt source register (ECR)	No	Yes
5	Program status word (PSW)	Yes	Yes
6 to 15	Reserved numbers for future function expansion (The operation is not guaranteed if accessed.)	No	No
16	CALLT execution status saving register (CTPC)	Yes	Yes
17	CALLT execution status saving register (CTPSW)	Yes	Yes
18	Exception/debug trap status saving register (DBPC)	Yes[Note 2]	Yes[Note 2]
19	Exception/debug trap status saving register (DBPSW)	Yes[Note 2]	Yes[Note 2]
20	CALLT base pointer (CTBP)	Yes	Yes
21 to 31	Reserved numbers for future function expansion (The operation is not guaranteed if accessed.)	No	No

Notes 1. Since only one set of these registers is available, the contents of this register must be saved by the program when multiple interrupt servicing is enabled.

2. Can be accessed only after the DBTRAP instruction or illegal opcode is executed and before the DBRET instruction is executed.

Caution Even if bit 0 of EIPC, FEPC, or CTPC is set (1) by the LDSR instruction, bit 0 is ignored during return with the RETI instruction following interrupt servicing (because bit 0 of PC is fixed to 0). When setting a value to EIPC, FEPC, and CTPC, set an even number (bit 0 = 0).

(2) Internal RAM area

An area of 60 KB maximum from 3FF0000H to 3FFEFFFH is reserved for the internal RAM area.

A 6 KB area from 3FFD800H to 3FFEFFFH is provided as physical internal RAM for the V850ES/IE2.

Addresses 3FF0000H to 3FFD7FFH are an access-prohibited area.

Figure 3-6. Internal RAM Area (6 KB)

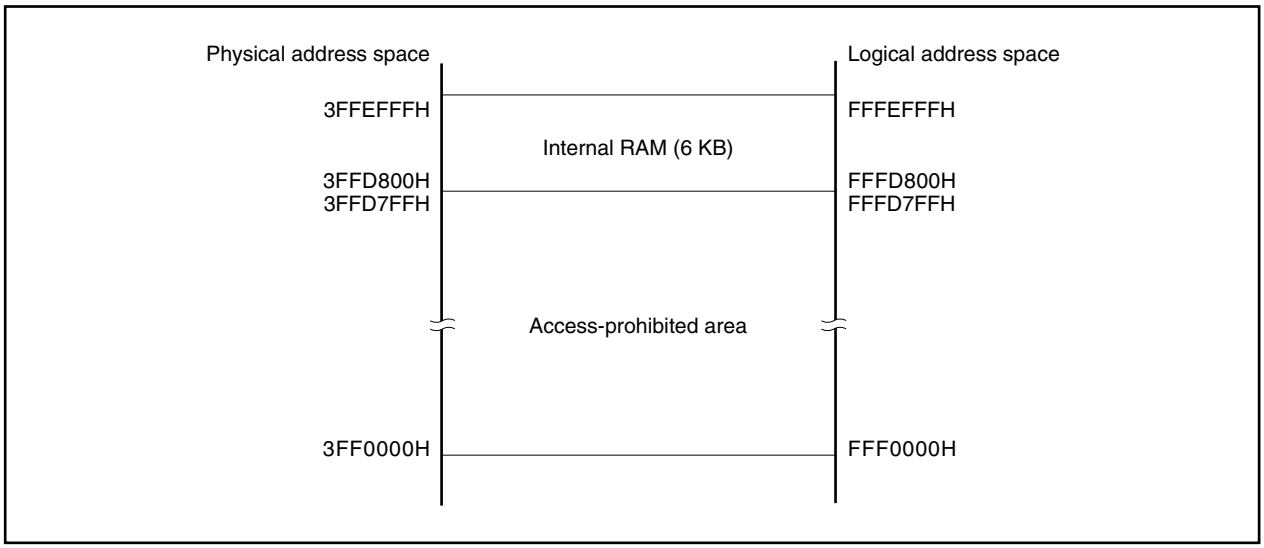


Table 4-10. Output Data and Port Read Value for Each Setting (2/4)

Port Name	Function	PMCmn	PFCEmn	PFCmn	PMmn	Output Data	Pmn Read Value	Remark
P14	Output port	0	None	×	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	TOQH03	1	None	0	0	Alternate output (timer output)	Port latch	
					1		Pin level	
	EVTQ0	1	None	1	0	–	Port latch	Alternate input (timer input)
					1		Pin level	
P16 (CLMER)[Note], P17	Output port[Note]	0	None	×	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	TOQ00 (CLMER)[Note], TOP21	1	None	0	0	Alternate output (timer output)	Port latch	
					1		Pin level	
	TIP20, TIP21	1	None	1	0	–	Port latch	Alternate input (timer input)
					1		Pin level	
P20 to P27	Output port	0	None	None	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	TOQ1T1 to TOQ1T3, TOQ1B1 to TOQ1B3, TOQ10, TOP31	1	None	None	0	Alternate output (timer output)	Port latch	
					1		Pin level	
P30	Output port	0	None	None	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	RXDA0	1	None	None	0	–	Port latch	Alternate input (serial input)
					1		Pin level	
P31	Output port	0	None	None	0	Port latch	Port latch	
	Input port				1	–	Pin level	
	TXDA0	1	None	None	0	Alternate output (serial output)	Port latch	
					1		Pin level	

Note When P16 is set as the output port or TOQ00 output function, if an error (oscillator stop) is detected by the clock monitor, the CLMER signal (low level) is output from P16. Low-level output is released by reset signal. For details, see **Table 4-5 Alternate-Function Pins of Port 1**.

Remark ×: Don't care

Table 4-11. Using Port Pin as Alternate-Function Pin (3/3)

Pin Name	Alternate Pin		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCEnx Bit of PFCEn Register	PFCnx Bit of PFCn Register	Other Bit (Register)
	Name	I/O						
P43	TOP00	Output	P43 = Setting not required	PM43 = Setting not required	PMC43 = 1	–	PFC43 = 0	
	TIP00	Input	P43 = Setting not required	PM43 = Setting not required	PMC43 = 1	–	PFC43 = 1	
P44	TOP01	Output	P44 = Setting not required	PM44 = Setting not required	PMC44 = 1	–	PFC44 = 0	
	TIP01	Input	P44 = Setting not required	PM44 = Setting not required	PMC44 = 1	–	PFC44 = 1	
PDL0	–	–	PDL0 = Setting not required	PMDL0 = Setting not required	–	–	–	
PDL1	–	–	PDL1 = Setting not required	PMDL1 = Setting not required	–	–	–	
PDL2	–	–	PDL2 = Setting not required	PMDL2 = Setting not required	–	–	–	
PDL3	–	–	PDL3 = Setting not required	PMDL3 = Setting not required	–	–	–	
PDL4	–	–	PDL4 = Setting not required	PMDL4 = Setting not required	–	–	–	
PDL5[Note]	FLMD1[Note]	Input	PDL5 = Setting not required	PMDL5 = Setting not required	–	–	–	
PDL6	–	–	PDL6 = Setting not required	PMDL6 = Setting not required	–	–	–	
PDL7	–	–	PDL7 = Setting not required	PMDL7 = Setting not required	–	–	–	

Note The PDL5 pin also functions as a pin to be set in the flash programming mode (FLMD1). This pin does not need to be manipulated using the port control register. For details, see **CHAPTER 18 FLASH MEMORY**.

(6) TMPn option register 0 (TPnOPT0)

The TPnOPT0 register is an 8-bit register that sets the capture/compare operation and detects overflow.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: TP0OPT0 FFFFF645H, TP1OPT0 FFFFF665H, TP2OPT0 FFFFF685H, TP3OPT0 FFFFF6A5H

TPnOPT0 (n = 0 to 3, k = 0, 2)

7	6	5	4	3	2	1	<0>
0	0	TPkCCS1[Note]	TPkCCS0[Note]	0	0	0	TPnOVF

TPkCCS1[Note]	TPkCCR1 register capture/compare selection
0	Compare register selected
1	Capture register selected (cleared by TPkCTL0.TPkCE bit = 0)
The TPkCCS1 bit setting is valid only in the free-running timer mode.	

TPkCCS0[Note]	TPkCCR0 register capture/compare selection
0	Compare register selected
1	Capture register selected (cleared by TPkCTL0.TPkCE bit = 0)
The TPkCCS0 bit setting is valid only in the free-running timer mode.	

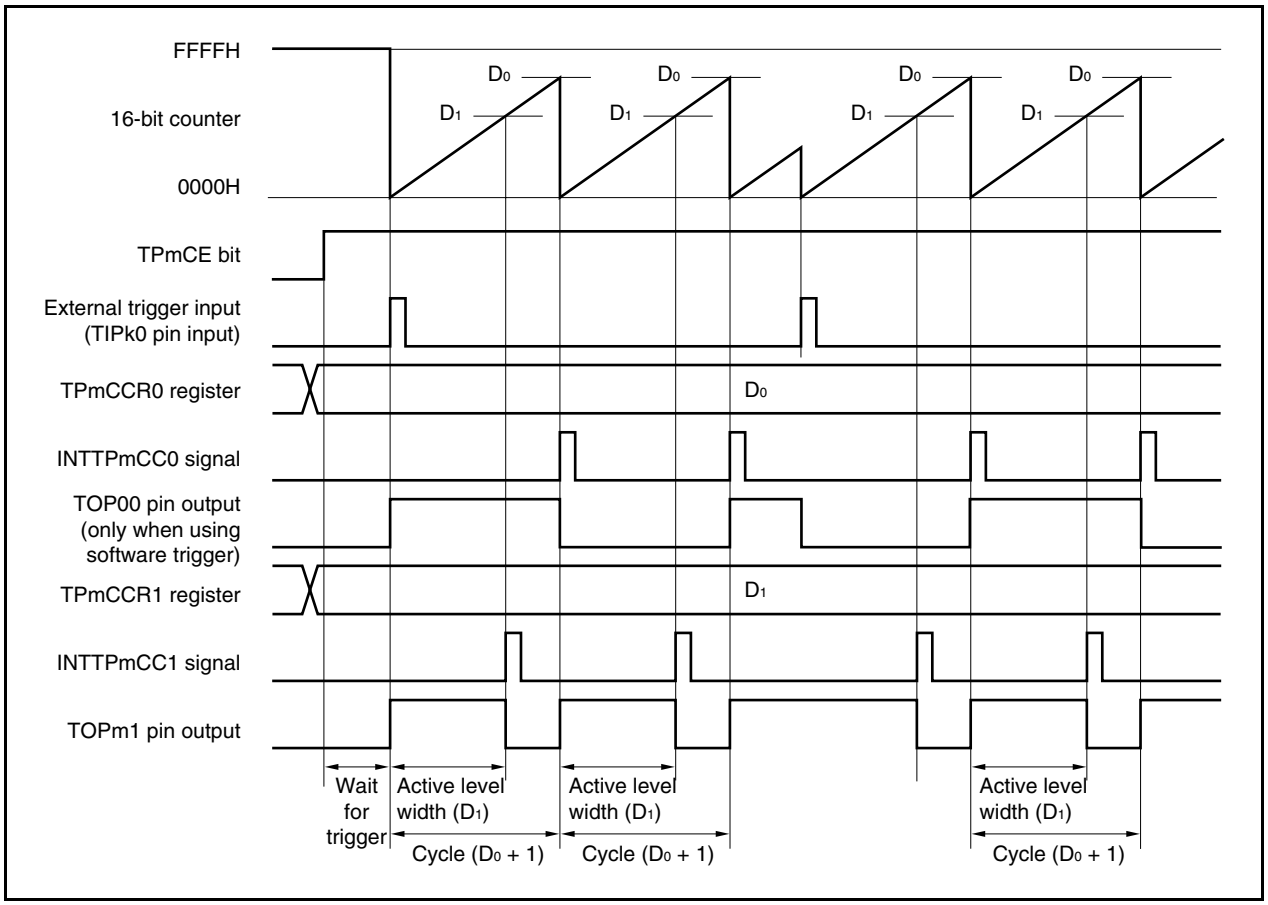
TPnOVF	TMPn overflow detection flag
Set (1)	Overflow occurred
Reset (0)	0 written to TPnOVF bit or TPnCTL0.TPnCE bit = 0
• The TPnOVF bit is set to 1 when the 16-bit counter value overflows from FFFFH to 0000H in the free-running timer mode or the pulse width measurement mode. • An overflow interrupt request signal (INTTPnOV) is generated at the same time that the TPnOVF bit is set to 1. The INTTPnOV signal is not generated in modes other than the free-running timer mode and the pulse width measurement mode. • The TPnOVF bit is not cleared to 0 even when the TPnOVF bit or the TPnOPT0 register is read when the TPnOVF bit = 1. • Before clearing the TPnOVF bit to 0 after generation of the INTTPnOV signal, be sure to confirm (by reading) that the TPnOVF bit is set to 1. • The TPnOVF bit can be both read and written, but the TPnOVF bit cannot be set to 1 by software. Writing 1 has no effect on the operation of TMPn.	

Note Valid only for TMP0 and TMP2. Be sure to clear bits 5 and 4 of TMP1 and TMP3 to 0.

Cautions 1. Rewrite the TPkCCS1 and TPkCCS0 bits when the TPkCE bit = 0. (The same value can be written when the TPkCE bit = 1.) If rewriting was mistakenly performed, clear the TPkCE bit to 0 and then set the bits again.

2. Be sure to clear bits 1 to 3, 6, and 7 to "0".

Figure 6-24. Basic Timing in External Trigger Pulse Output Mode



16-bit timer/event counter P waits for a trigger when the TPmCE bit is set to 1. When the trigger is generated, the 16-bit counter is cleared from FFFFH to 0000H, starts counting at the same time, and outputs a PWM waveform from the TOPm1 pin. If the trigger is generated again while the counter is operating, the counter is cleared to 0000H and <R> restarted. (The output of the TOP00 pin is inverted. The TOPm1 pin outputs high level regardless of the status (high/low) when a trigger occurs.)

The active level width, cycle, and duty factor of the PWM waveform can be calculated as follows.

Active level width = (Set value of TPmCCR1 register) × Count clock cycle
Cycle = (Set value of TPmCCR0 register + 1) × Count clock cycle
Duty factor = (Set value of TPmCCR1 register)/(Set value of TPmCCR0 register + 1)

The compare match interrupt request signal INTTPmCC0 is generated when the 16-bit counter counts next time after its count value matches the value of the CCR0 buffer register, and the 16-bit counter is cleared to 0000H. The compare match interrupt request signal INTTPmCC1 is generated when the count value of the 16-bit counter matches the value of the CCR1 buffer register.

The value set to the TPmCCRa register is transferred to the CCRa buffer register when the count value of the 16-bit counter matches the value of the CCRa buffer register and the 16-bit counter is cleared to 0000H.

The valid edge of an external trigger input (TIPk0) or setting the software trigger (TPmCTL1.TPmEST bit) to 1 is used as the trigger.

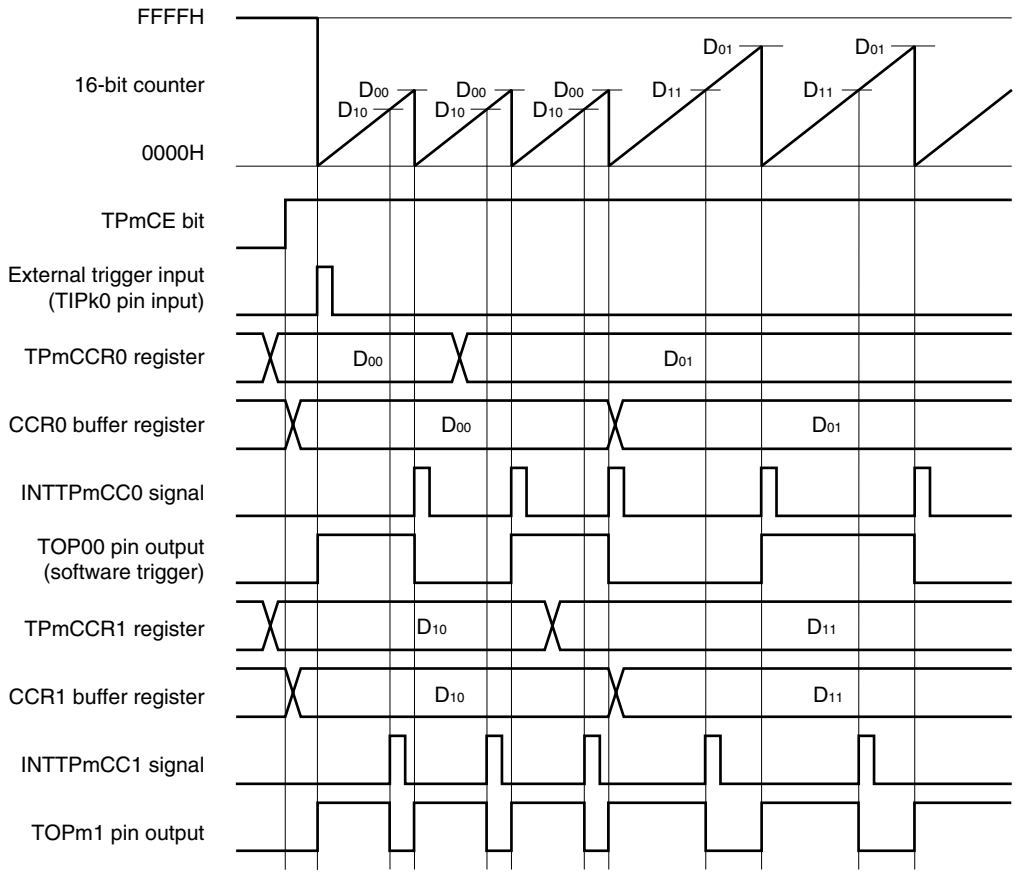
Remark m = 0, 2, 3
k = 0, 2
a = 0, 1

(2) External trigger pulse output mode operation timing

(a) Note on changing pulse width during operation

To change the PWM waveform while the counter is operating, write the TPmCCR1 register last.

Rewrite the TPmCCRa register after writing the TPmCCR1 register after the INTTPmCC0 signal is detected.



Remark m = 0, 2, 3
k = 0, 2

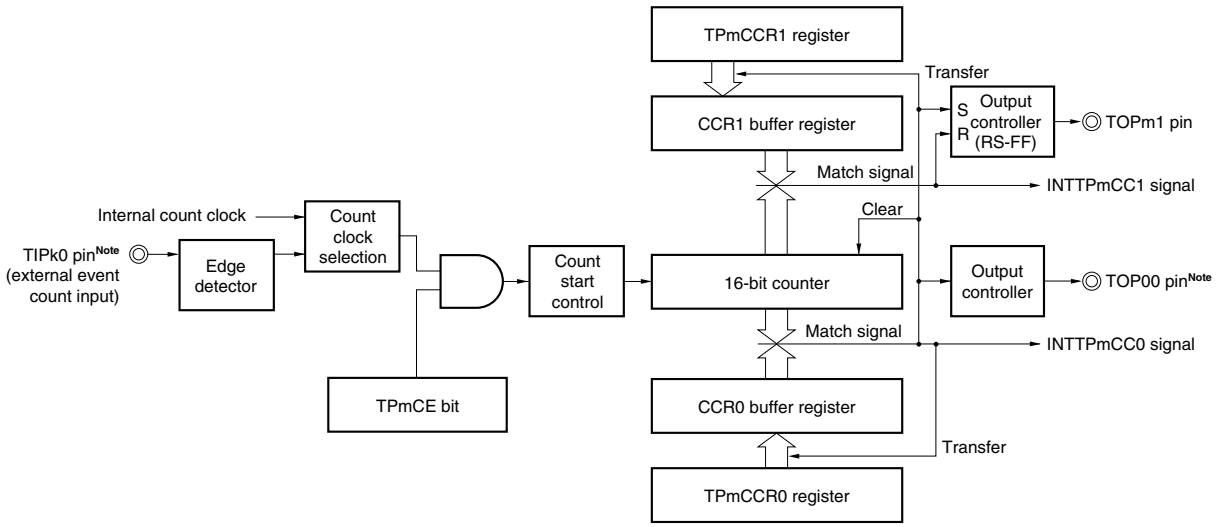
6.6.5 PWM output mode (TPmMD2 to TPmMD0 bits = 100)

This mode is valid only in TMP0, TMP2, and TMP3.

In the PWM output mode, a PWM waveform is output from the TOPm1 pin when the TPmCTL0.TPmCE bit is set to 1.

In addition, a PWM waveform with a duty factor of 50% with the set value of the TPmCCR0 register + 1 as half its cycle is output from the TOP00 pin.

Figure 6-31. Configuration in PWM Output Mode

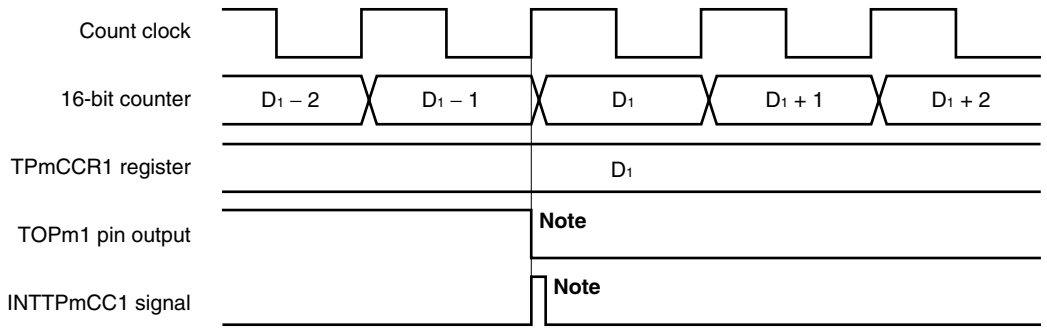


Note Because the external event count input pin (TIP00) and timer output pin (TOP00) share the same alternate-function pin, two functions cannot be used at the same time.

Remark m = 0, 2, 3
k = 0, 2

(c) Generation timing of compare match interrupt request signal (INTTPmCC1)

The timing of generation of the INTTPmCC1 signal in the PWM output mode differs from the timing of INTTPmCC1 signals in other modes; the INTTPmCC1 signal is generated when the count value of the 16-bit counter matches the value of the TPmCCR1 register.



Note Actually, the timing is delayed by one operating clock (fxx).

Remark m = 0, 2, 3

Usually, the INTTPmCC1 signal is generated in synchronization with the next counting up after the count value of the 16-bit counter matches the value of the TPmCCR1 register.

In the PWM output mode, however, it is generated one clock earlier. This is because the timing is changed to match the change timing of the output signal of the TOPm1 pin.

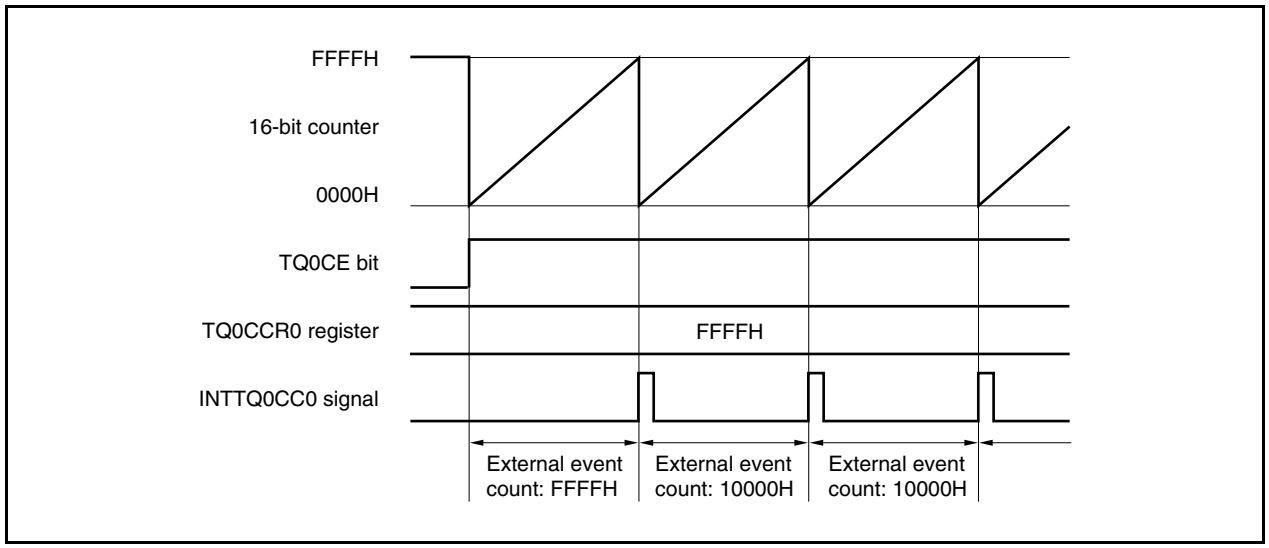
(2) Operation timing in external event count mode

Cautions 1. In the external event count mode, the TQ0CCR0 to TQ0CCR3 registers must not be cleared to 0000H.

<R> **2. In the external event count mode, use of the timer output (TOQ00 to TOQ03) is disabled. If using timer output (TOQ00 to TOQ03) with external event count input (EVTQ0), set the interval timer mode, and enable the count clock operation with the external event count input (TQ0CTL1.TQ0EEE bit = 1) (see 7.6.1 (3) Operation by external event count input (EVTQ0)).**

(a) Operation if TQ0CCR0 register is set to FFFFH

If the TQ0CCR0 register is set to FFFFH, the 16-bit counter counts to FFFFH each time the valid edge of the external event count signal has been detected. The 16-bit counter is cleared to 0000H in synchronization with the next count-up timing, and the INTTQ0CC0 signal is generated. At this time, the TQ0OPT0.TQ0OVF bit is not set.



16-bit timer/event counter Q waits for a trigger when the TQ0CE bit is set to 1. When the trigger is generated, the 16-bit counter is cleared from FFFFH to 0000H, starts counting at the same time, and outputs a PWM waveform from the TOQ0b pin. If the trigger is generated again while the counter is operating, the counter is cleared to 0000H and <R> restarted. (The output of the TOQ00 pin is inverted. The TOQ0b pin outputs high level regardless of the status (high/low) when a trigger occurs.)

The active level width, cycle, and duty factor of the PWM waveform can be calculated as follows.

Active level width = (Set value of TQ0CCRb register) × Count clock cycle
Cycle = (Set value of TQ0CCR0 register + 1) × Count clock cycle
Duty factor = (Set value of TQ0CCRb register)/(Set value of TQ0CCR0 register + 1)

The compare match interrupt request signal INTTQ0CC0 is generated when the 16-bit counter counts next time after its count value matches the value of the CCR0 buffer register, and the 16-bit counter is cleared to 0000H. The compare match interrupt request signal INTTQ0CCb is generated when the count value of the 16-bit counter matches the value of the CCRb buffer register.

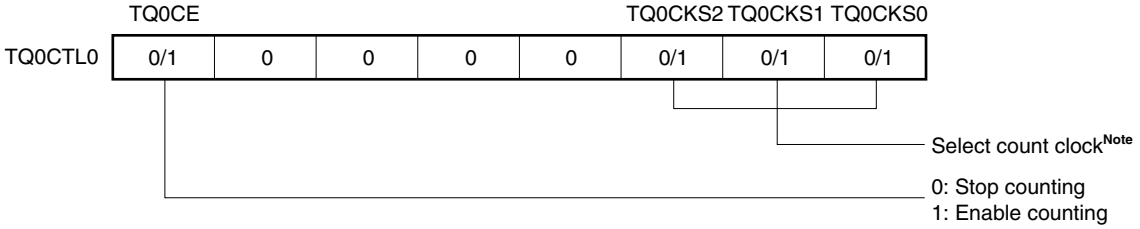
The value set to the TQ0CCRa register is transferred to the CCRa buffer register when the count value of the 16-bit counter matches the value of the CCRa buffer register and the 16-bit counter is cleared to 0000H.

Only setting the software trigger (TQ0CTL1.TQ0EST bit) to 1 is used as the trigger.

Remark a = 0 to 3
b = 1 to 3

Figure 7-24. Setting of Registers in External Trigger Pulse Output Mode (1/3)

(a) TMQ0 control register 0 (TQ0CTL0)



Note The setting is invalid when the TQ0CTL1.TQ0EEE bit = 1.

When the TQ0CE bit is set to 1, the 16-bit counter is cleared from FFFFH to 0000H, starts counting, and outputs PWM waveform from the TOQ0b pin (TOQH0b).

The active level width, cycle, and duty factor of the PWM waveform can be calculated as follows.

Active level width = (Set value of TQ0CCRb register) × Count clock cycle
Cycle = (Set value of TQ0CCR0 register + 1) × Count clock cycle
Duty factor = (Set value of TQ0CCRb register)/(Set value of TQ0CCR0 register + 1)

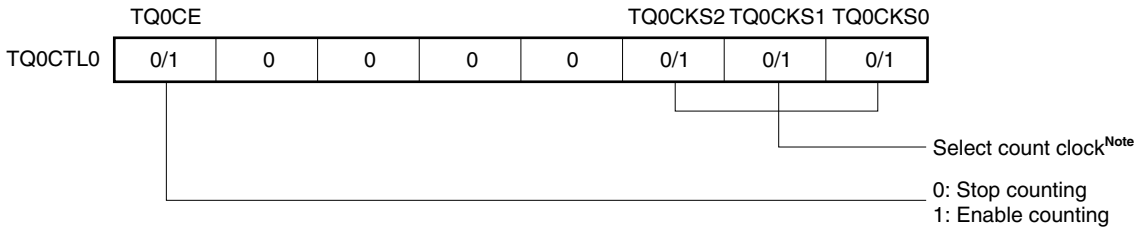
The PWM waveform can be changed by rewriting the TQ0CCRa register while the counter is operating. The newly written value is reflected when the count value of the 16-bit counter matches the value of the CCR0 buffer register and the 16-bit counter is cleared to 0000H.

The compare match interrupt request signal INTTQ0CC0 is generated when the 16-bit counter counts next time after its count value matches the value of the CCR0 buffer register, and the 16-bit counter is cleared to 0000H. The compare match interrupt request signal INTTQ0CCb is generated when the count value of the 16-bit counter matches the value of the CCRb buffer register.

Remark a = 0 to 3
b = 1 to 3

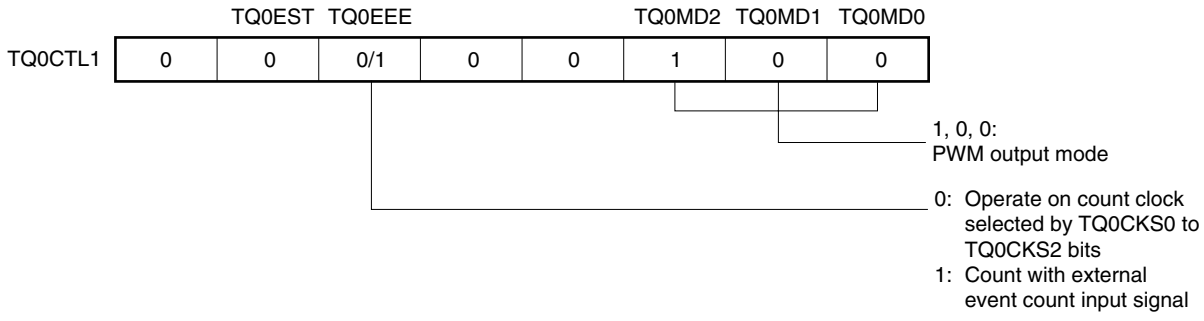
Figure 7-32. Register Setting in PWM Output Mode (1/3)

(a) TMQ0 control register 0 (TQ0CTL0)



Note The setting is invalid when the TQ0CTL1.TQ0EEE bit = 1.

(b) TMQ0 control register 1 (TQ0CTL1)



When performing an interval operation in the free-running timer mode, two intervals can be set with one channel.

To perform the interval operation, the value of the corresponding TQnCCRa register must be re-set in the interrupt servicing that is executed when the INTTQnCCa signal is detected.

The set value for re-setting the TQnCCRa register can be calculated by the following expression, where "D_a" is the interval period.

Compare register default value: $D_a - 1$

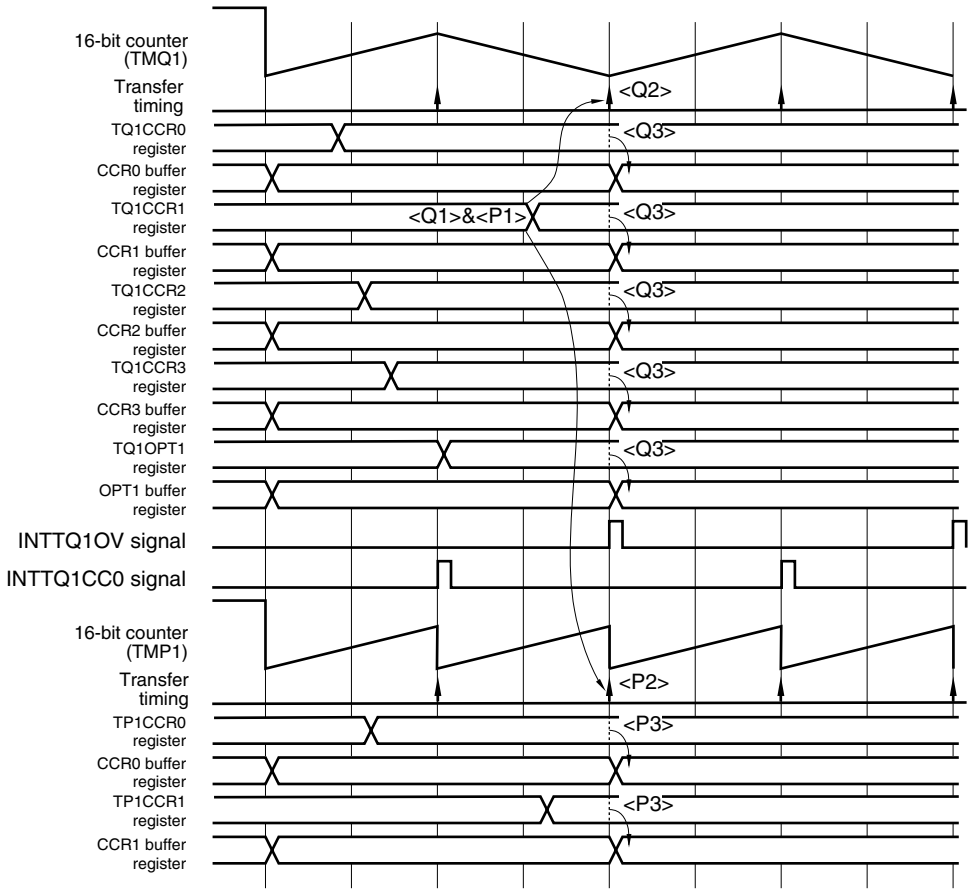
Value set to compare register second and subsequent time: Previous set value + D_a

(If the calculation result is greater than FFFFH, subtract 10000H from the result and set this value to the register.)

Remark n = 0, 1

a = 0 to 3

Figure 9-26. Basic Operation in Batch Mode



[Operation of TMQ1]

<Q1> Write the TQ1CCR1 register

<Q2> The target timing is the first transfer timing after a write to the TQ1CCR1 register.

<Q3> The values are transferred all at once at the transfer timing.

[Operation of TMP1]

<P1> Write the TQ1CCR1 register

<P2> The target timing is the first transfer timing after a write to the TQ1CCR1 register.

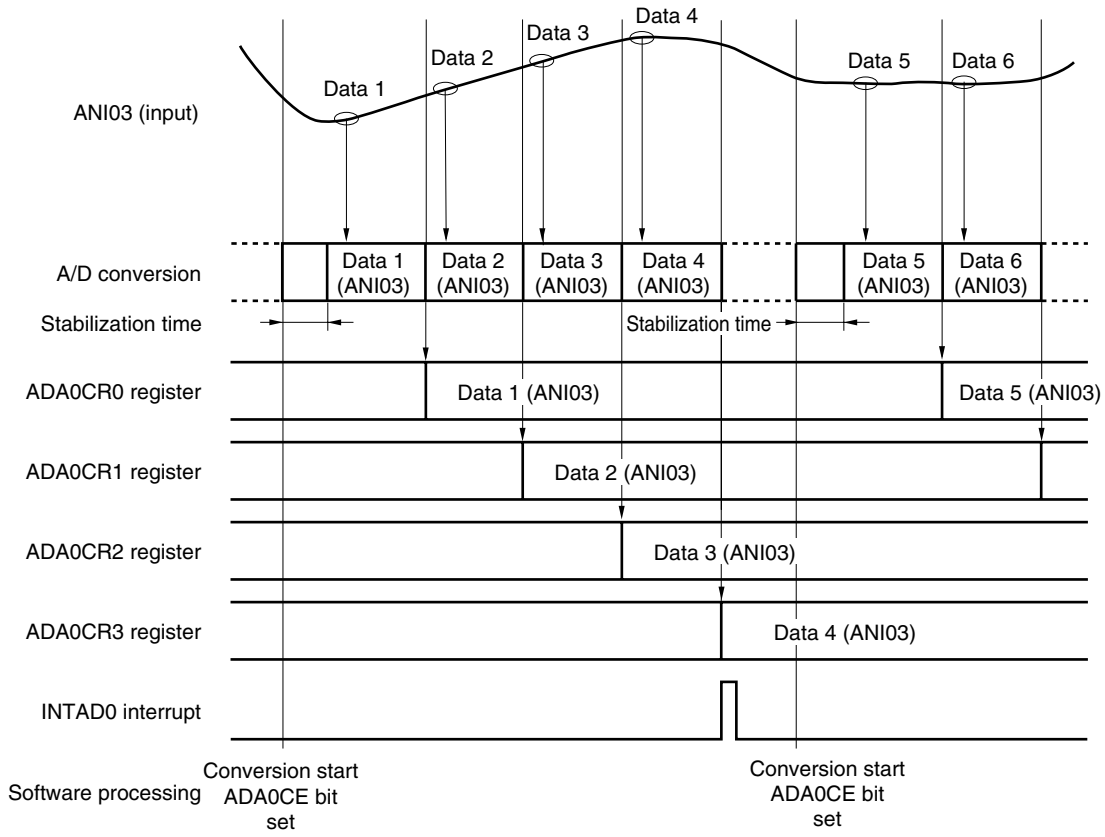
<P3> The values are transferred all at once at the transfer timing.

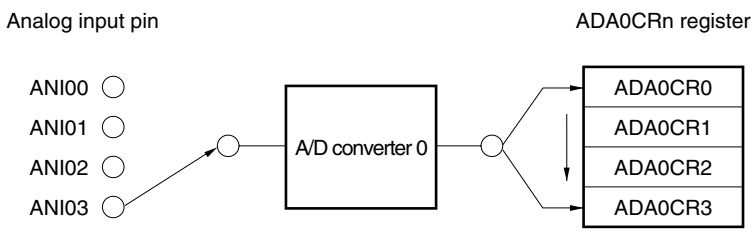
- **4-buffer mode**

  In this mode the voltage of one analog input pin (ANInm) is A/D converted four times and the results are stored in the ADAnCRm register. The A/Dn conversion end interrupt request signal (INTADn) is generated when the four A/D conversions end. After end of A/D conversion, the conversion operation is stopped.

Remark n = 0, 1, m = 0 to 3

Figure 11-8. One-Shot Select 4-Buffer Mode Operation Timing (When ADA0M0.ADA0MD1 and ADA0M0.ADA0MD0 Bits = 10, ADA0M2.ADA0BS Bit = 1, ADA0S.ADA0S1 and ADA0S.ADA0S0 Bits = 11)





Caution The A/D conversion results are stored in the order of ADA0CR0 → ADA0CR1 → ADA0CR2 → ADA0CR3 regardless of the selected analog input pin.

(6) UARTAn receive data register (UAnRX)

The UAnRX register is an 8-bit buffer register that stores parallel data converted by the UARTAn receive shift register.

The data stored in the UARTAn receive shift register is transferred to the UAnRX register upon end of reception of 1 byte of data. A reception end interrupt request signal (INTUAnR) is generated at this timing.

During LSB-first reception when the data length has been specified as 7 bits, the receive data is transferred to bits 6 to 0 of the UAnRX register and the MSB always becomes 0. During MSB-first reception, the receive data is transferred to bits 7 to 1 of the UAnRX register and the LSB always becomes 0.

When an overrun error occurs (UAnSTR.UAnOVE bit = 1), the receive data at this time is not transferred to the UAnRX register and is discarded.

This register is read-only, in 8-bit units.

In addition to reset, the UAnRX register can be set to FFH by clearing the UAnCTL0.UAnPWR bit to 0.

After reset: FFH R Address: UA0RX FFFFFA06H, UA1RX FFFFFA16H

	7	6	5	4	3	2	1	0
UAnRX								

(n = 0, 1)

(7) UARTAn transmit data register (UAnTX)

The UAnTX register is an 8-bit register used to set transmit data.

Transmission starts when transmit data is written to the UAnTX register in the transmission enabled status (UAnCTL0.UAnTXE bit = 1). When the data of the UAnTX register has been transferred to the UARTAn transmit shift register, the transmission enable interrupt request signal (INTUAnT) is generated.

This register can be read or written in 8-bit units.

Reset sets this register to FFH.

After reset: FFH R/W Address: UA0TX FFFFFA07H, UA1TX FFFFFA17H

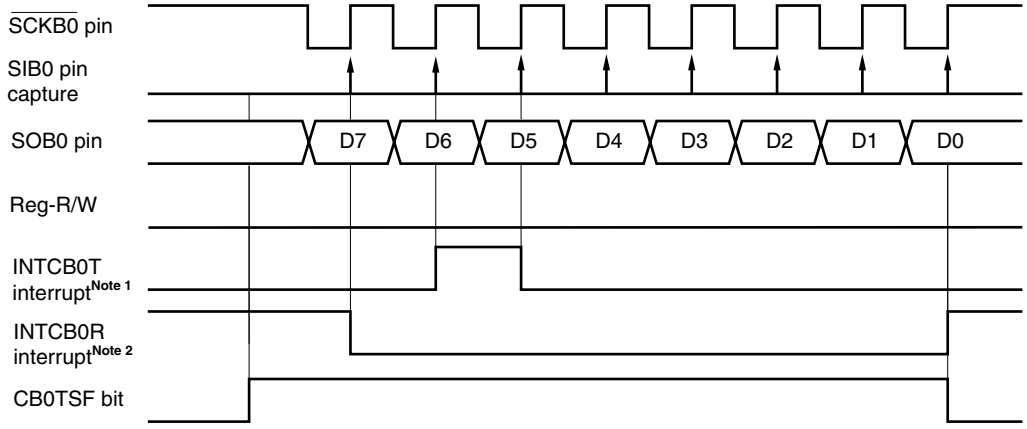
	7	6	5	4	3	2	1	0
UAnTX								

(n = 0, 1)

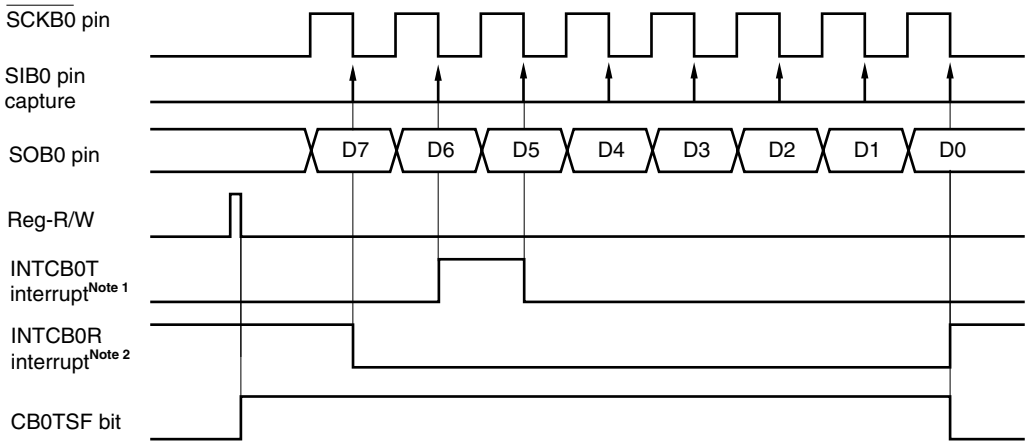
13.4.14 Clock timing

(1/2)

(i) Communication type 1 (CB0CKP and CB0DAP bits = 00)



(ii) Communication type 3 (CB0CKP and CB0DAP bits = 10)



Notes 1. The INTCB0T interrupt is set when the data written to the CB0TX register is transferred to the data shift register in the continuous transmission or continuous transmission/reception mode. In the single transmission or single transmission/reception mode, the INTCB0T interrupt request signal is not generated, but the INTCB0R interrupt request signal is generated upon end of communication.

2. The INTCB0R interrupt occurs if reception is correctly ended and receive data is ready in the CB0RX register while reception is enabled. In the single mode, the INTCB0R interrupt request signal is generated even in the transmission mode, upon end of communication.

Caution In single transfer mode, writing to the CB0TX register with the CB0TSF bit set to 1 is ignored. This has no influence on the operation during transfer.
Use the continuous transfer mode, not the single transfer mode.

16.3.4 Power-on-clear circuit (POC)

(1) Overview

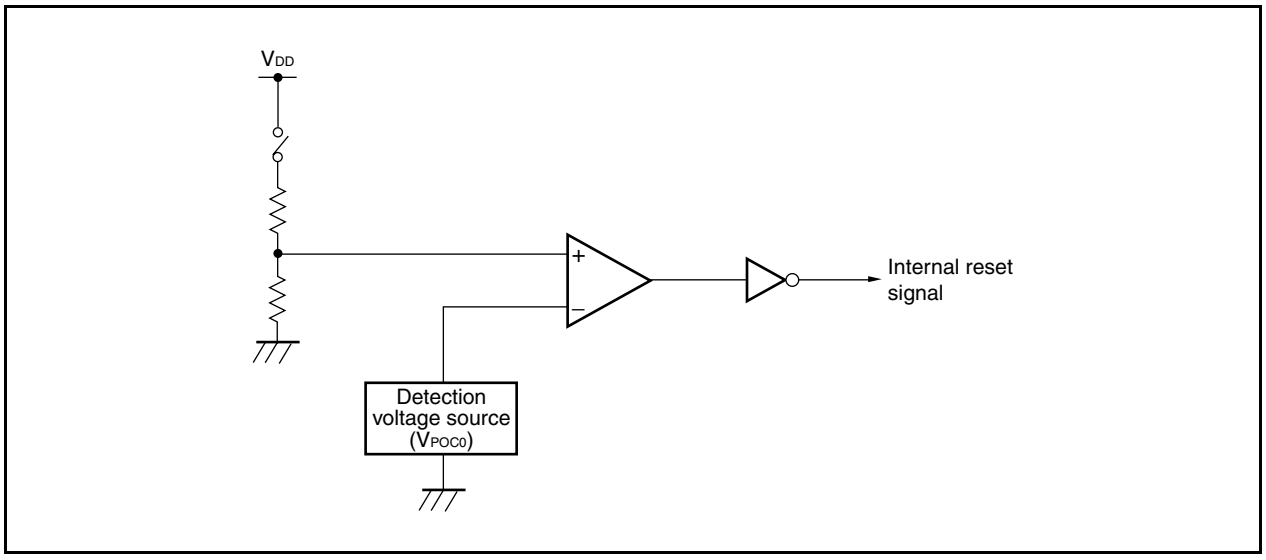
An overview of the power-on-clear (POC) circuit is shown below.

- Generates a reset signal upon power application.
- Compares the supply voltage (V_{DD}) and detection voltage (V_{POC0}), and generates a reset signal when $V_{DD} < V_{POC0}$.

(2) Configuration

The block diagram is shown below.

Figure 16-8. Block Diagram of Power-on-Clear Circuit



18.4.6 Pin connection

When performing on-board writing, mount a connector on the target system to connect to the dedicated flash memory programmer. Also, incorporate a function on-board to switch from the normal operation mode to the flash memory programming mode.

In the flash memory programming mode, all the pins not used for flash memory programming become the same status as that immediately after reset. Therefore, pin handling is required when the external device does not acknowledge the status immediately after a reset.

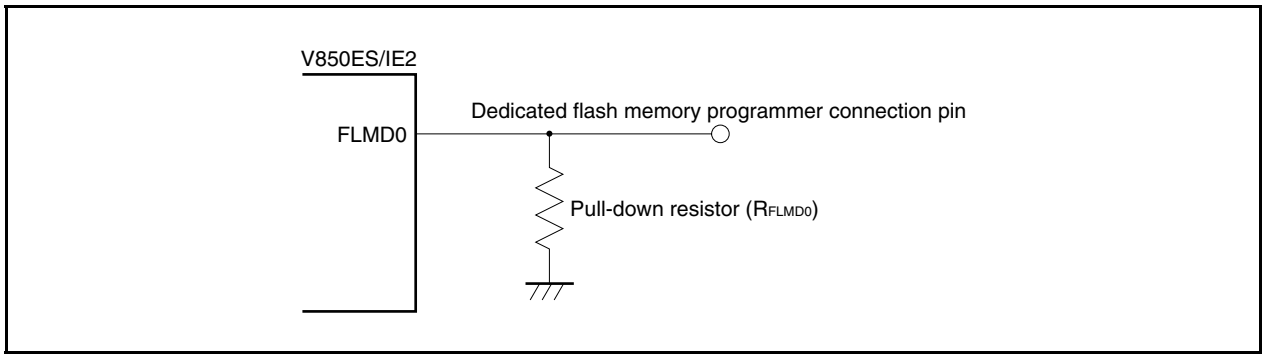
(1) FLMD0 pin

In the normal operation mode, input a voltage of V_{SS} level to the FLMD0 pin. In the flash memory programming mode, supply a write voltage of V_{DD} level to the FLMD0 pin.

Because the FLMD0 pin serves as a write protection pin in the self programming mode (μPD70F3714 only), a voltage of V_{DD} level must be supplied to the FLMD0 pin via port control, etc., before writing to the flash memory.

For details, see **18.5.5 (1) FLMD0 pin**.

Figure 18-10. FLMD0 Pin Connection Example



Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, EV_{DD}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = EV_{DD} = EV_{SS} = AV_{DD0} = AV_{SS0} = AV_{DD1} = AV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_c = 1 MHz Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Operating Conditions (T_A = –40 to +85°C, V_{SS} = EV_{SS} = AV_{SS0} = AV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{XX}	PLL mode	20		20	MHz
		Clock through mode	2.5		2.5	MHz
CPU clock frequency	f_{CPU}	PLL mode	2.5		20	MHz
		Clock through mode	0.3125		2.5	MHz
V_{DD}, EV_{DD} voltage	V_{DD}, EV_{DD}		3.5		5.5	V
AV_{DD0}, AV_{DD1} voltage	AV_{DD}	Operation is not guaranteed when EV_{DD} is 4.5 V or less.	4.5		EV_{DD}	V